FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22114-1E

Communication Control

ASSP

IP PACKET FORWARDING ENGINE

MB86977

■ DESCRIPTION

The MB86977 is an LSI that enables processes that previously were handled through software, such as packet-destination transferring and filtering, to be handled through hardware, thereby achieving a full wire speed bi-directional LAN-WAN throughput of 100 Mbps. The IP forwarding can be applied to both IPv4 and IPv6 packets at full wire speed.The Layer 3/4 filtering capabilities enables application of basic security policies, and also makes it possible to build Demilitarized Zones (D.M.Z.) for servers to be accessed directly from the WWW without intervention of software. Out of a total of four MAC interfaces, two are used for internal segments (i.e. LAN0,LAN1), one as a D.M.Z. port, and the remaining as a WAN port. The D.M.Z.interface may be configured as an extra internal segment (i.e. LAN2)if desired. The Layer 2 switch can switch packets from internal segments (LAN0, LAN1 and LAN2) based on their MAC addresses.

In addition, real-time applications such as streaming media flows and VoIP streams can be prioritized by the priority control function. The MB86977 offers the ideal solution for superior performance required by network appliances such as broadband routers.

■ FEATURES

1. Built-in high performance IP Forwarding Engine “Fujitsu/FLS Express Forwarding (FEF)” Engine

• IP packet forwarding

- Routing operations such as Ethernet MAC Address replacement, TTL reduction and checksum generation done in hardware
- Supports both IPv4 and IPv6
- Supports PPPoE Tunneling and IPv6 over IPv4 Tunneling at WAN Interface

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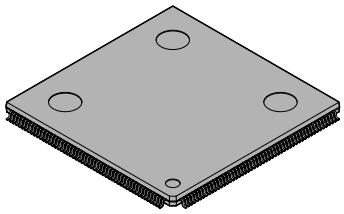
■ PACKAGE

208-pin plastic LQFP



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- **NAT (NAPT)**
  - NAT operations such as IP Address replacement, Transport layer port number replacement, and checksum generation done in hardware
  - Supports PPPoE Tunneling and IPv6 over IPv4 Tunneling at WAN Interface
  - Supports IPv4 only.

- **Layer 3/4 Filtering**
  - Filtering based on IP Address (Dst and/or Src, supports both IPv4/IPv6)
  - Filtering based on TCP/UDP port number (supports TCP and ACK flag)
  - Filtering based on combinations of IP address and TCP port number in TCP connections for both IPv4 and IPv6.
  - Filtering based on ICMP Type
  - Filtering based on Protocol Type (Type field in Ethernet)
  - Supports PPPoE discovery stage /session stage filtering
  - Supports AH (Authentication Header) Type VPN packet filtering by Layer 3/4 information
  - Supports ESP (Encapsulating Security Payload) type VPN packets filtering by IP Address
  - Filtering can be applied independently per each port (LAN,D.M.Z., WAN)
  - Supports Max 64x2 (Inbound and Outbound) Filter Table Entries
  - Supports filter logging

- Packet Prioritizing Function
  - Prioritization based on combination of IPv4 address and UDP port number
  - Prioritization based on combination of IPv4 address and ToS field
  - Prioritization based on combination of IPv4 address, ToS field and UDP port number
  - Prioritization based on combination of IPv6 address, Traffic Class and Flow Label
  - Supports QoS mapping ToS field

Note: The FEF supports only DIX type Ethernet Frames, and does not support IEEE802.1 LLC type frames and IEEE802.1Q VLAN tagged frames (These frames, when received, will be sent to the host).
Achieving a full wire rate bi-directional throughput of 100 Mbps at 50 MHz operation.

2. Layer 2 (MAC) Functions

- Four integrated IEEE802.3 compliant 10/100BaseT/TX MAC ports
- Port selectable RMII/MII interface (Supports both full duplex and half duplex)
- SMI Interface for PHY device configuration
- Supports Auto Negotiation
- Supports IEEE802.3x Flow control
- Supports back pressure for half duplex mode
- Integrated SRAM for packet buffering (PRAM)
- Store-and-Forward switching method
- MAC Address table up to 50 entries
- MAC Address auto learning and aging

3. Host Interface

- 32 bit-width SRAM host interface
- BigEndian/LittleEndian configurable

4. Other features

- 208-pin Plastic LQFP Package

■ PIN ASSIGNMENT

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TDOUT	36	DQ18	71	COL_0	106	VSS
2	SDO1	37	DQ19	72	TX_CLK_0	107	TX_EN_D
3	SDO2	38	DQ20	73	VSS	108	TXD_D [0]
4	SDO3	39	VDDE	74	RX_DV_0	109	TXD_D [1]
5	SDO4	40	VSS	75	RXD_0 [0]	110	TXD_D [2]
6	SDO5	41	VDDI	76	RXD_0 [1]	111	TXD_D [3]
7	SDO6	42	DQ21	77	RXD_0 [2]	112	VDDE
8	INT_	43	DQ22	78	RXD_0 [3]	113	VSS
9	VDDE	44	DQ23	79	RX_ER_0	114	VDDI
10	VSS	45	DQ24	80	RX_CLK_0	115	VDDE
11	VDDI	46	DQ25	81	VDDE	116	VSS
12	VDDE	47	DQ26	82	VSS	117	VDDI
13	VSS	48	DQ27	83	VDDI	118	CRS_DV_D
14	VDDI	49	DQ28	84	CRS_DV_1	119	COL_D
15	DQ0	50	DQ29	85	COL_1	120	TX_CLK_D
16	DQ1	51	DQ30	86	TX_CLK_1	121	VSS
17	DQ2	52	DQ31	87	VSS	122	RX_DV_D
18	DQ3	53	VDDE	88	RX_DV_1	123	RXD_D [0]
19	DQ4	54	VSS	89	RXD_1 [0]	124	RXD_D [1]
20	DQ5	55	VDDI	90	RXD_1 [1]	125	RXD_D [2]
21	DQ6	56	VDDE	91	RXD_1 [2]	126	RXD_D [3]
22	DQ7	57	VSS	92	RXD_1 [3]	127	RX_ER_D
23	DQ8	58	VDDI	93	RX_ER_1	128	RX_CLK_D
24	DQ9	59	TX_EN_0	94	RX_CLK_1	129	VDDE
25	DQ10	60	TXD_0 [0]	95	VDDE	130	VSS
26	VDDE	61	TXD_0 [1]	96	VSS	131	VDDI
27	VSS	62	TXD_0 [2]	97	VDDI	132	CRS_DV_W
28	VDDI	63	TXD_0 [3]	98	VDDE	133	COL_W
29	DQ11	64	VDDE	99	VSS	134	TX_CLK_W
30	DQ12	65	VSS	100	VDDI	135	VSS
31	DQ13	66	VDDI	101	TX_EN_1	136	RX_DV_W
32	DQ14	67	VDDE	102	TXD_1 [0]	137	RXD_W [0]
33	DQ15	68	VSS	103	TXD_1 [1]	138	RXD_W [1]
34	DQ16	69	VDDI	104	TXD_1 [2]	139	RXD_W [2]
35	DQ17	70	CRS_DV_0	105	TXD_1 [3]	140	RXD_W [3]

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
141	RX_ER_W	158	VDDI	175	A4	192	SDI4
142	RX_CLK_W	159	VDDE	176	A5	193	SDI5
143	VDDE	160	VSS	177	A6	194	SDI6
144	VSS	161	VDDI	178	A7	195	VSS
145	VDDI	162	MDIO	179	A8	196	XTCK
146	VDDE	163	VSS	180	A9	197	VSS
147	VSS	164	REF_CLK	181	A10	198	TRST
148	VDDI	165	VSS	182	A11	199	TMODE
149	TX_EN_W	166	CS_	183	A12	200	VPD
150	TXD_W [0]	167	WE_	184	A13	201	TDIN
151	TXD_W [1]	168	RE_	185	SRST_	202	TCLK
152	TXD_W [2]	169	VDDE	186	VDDE	203	VDDE
153	TXD_W [3]	170	VSS	187	VSS	204	VSS
154	VSS	171	VDDI	188	VDDI	205	VDDI
155	MDCLK	172	SCLK	189	SDI1	206	VDDE
156	VDDE	173	A2	190	SDI2	207	VSS
157	VSS	174	A3	191	SDI3	208	VDDI

■ PIN DESCRIPTION

• Host (SRAM) interface

Pin No.	Pin Name	I/O	Function
173 to 184	A2 to A13	I	ADDRESS BUS Address input
15 to 25 29 to 38 42 to 52	DQ0 to DQ31	I/O	DATA INPUT/OUTPUT Data input/output (32 bit)
166	CS_	I	CHIP SELECT Chip select input
167	WE_	I	WRITE ENABLE Write operation enable signal (low enable)
168	RE_	I	READ ENABLE Read operation enable signal (low enable)
8	INT_	O	INTERRUPT Interrupt indication (low enable)

• RMII interface

Pin No.	Pin Name	I/O	Function
164	REF_CLK	I	REFERENCE CLOCK Reference clock from the PHY device. The frequency is 50 MHz for both 10 Mbps and 100 Mbps.
150, 151 108, 109 60, 61 102, 103	TXD_W [1 : 0] TXD_D [1 : 0] TXD_0 [1 : 0] TXD_1 [1 : 0]	O	TRANSMIT DATA The two bit data is transmitted to PHY devices through this interface. Synchronous with REF_CLK.
149 107 59 101	TX_EN_W TX_EN_D TX_EN_0 TX_EN_1	O	TRANSMIT ENABLE Active high signal indicates that TX data is valid.Synchronous with REF_CLK.
141 127 79 93	RX_ER_W RX_ER_D RX_ER_0 RX_ER_1	I	RECEIVE ERROR Active high signal indicates that an invalid symbol has been detected within a received packet.This input is ignored when the CRS_DV signal is inactive.
137, 138 123, 124 75, 76 89, 90	RXD_W [1 : 0] RXD_D [1 : 0] RXD_0 [1 : 0] RXD_1 [1 : 0]	I	RECEIVE DATA The two bit data is received from the PHY device through this interface.
132 118 70 84	CRS_DV_W CRS_DV_D CRS_DV_0 CRS_DV_1	I	CARRIER SENSE / RECEIVE DATA VALID PHY Device inputs active high signal when the interface is receiving data. Asynchronous assertion/deassertion by PHY device upon carrier detection/carrier invalid.

Note : The logical AND of the TX_EN and CRS_DV signals indicate a collision during half duplex modes.

• MII Interface

Pin No.	Pin Name	I/O	Description
134 120 72 86	TX_CLK_W TX_CLK_D TX_CLK_0 TX_CLK_1	I	TX CLOCK This clock from the PHY device provides the timing reference for transfer of TX_EN and TXD signals. The frequency is 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps.
150 to 153 108 to 111 60 to 63 102 to 105	TXD_W [3 : 0] TXD_D [3 : 0] TXD_0 [3 : 0] TXD_1 [3 : 0]	O	TRANSMIT DATA The nibble data is transmitted to PHY devices through this interface.
149 107 59 101	TX_EN_W TX_EN_D TX_EN_0 TX_EN_1	O	TRANSMIT ENABLE Active high signal indicates that TX data is valid. Synchronous with TX_CLK.
142 128 80 94	RX_CLK_W RX_CLK_D RX_CLK_0 RX_CLK_1	I	RX CLOCK This clock from the PHY device provides the timing reference for reception. The frequency is 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps.
141 127 79 93	RX_ER_W RX_ER_D RX_ER_0 RX_ER_1	I	RECEIVE ERROR Active high signal indicates that an invalid symbol has been detected within a received packet.This input is ignored when RX_DV signal of the same interface is inactive.These pins are used for both RMII and MII modes.
136 122 74 88	RX_DV_W RX_DV_D RX_DV_0 RX_DV_1	I	RECEIVE DATA VALID Active high signal indicates that RXD is valid.
132 118 70 84	CRS_DV_W CRS_DV_D CRS_DV_0 CRS_DV_1	I	CARRIER SENSE Active high signal indicates that either the transmit or receive medium is not idle. It is not synchronous to any clock. These pins are used for both RMII and MII modes.
137 to 140 123 to 126 75 to 78 89 to 92	RXD_W [3 : 0] RXD_D [3 : 0] RXD_0 [3 : 0] RXD_1 [3 : 0]	I	RECEIVE DATA Nibble data from the PHY device.Bits [1:0] are used for both MII and RMII modes.
133 119 71 85	COL_W COL_D COL_0 COL_1	I	COLLISION DETECT Active high signal indicates that collision has been detected in half duplex mode. It is valid when TX_EN is active. It is not synchronous to any clock.

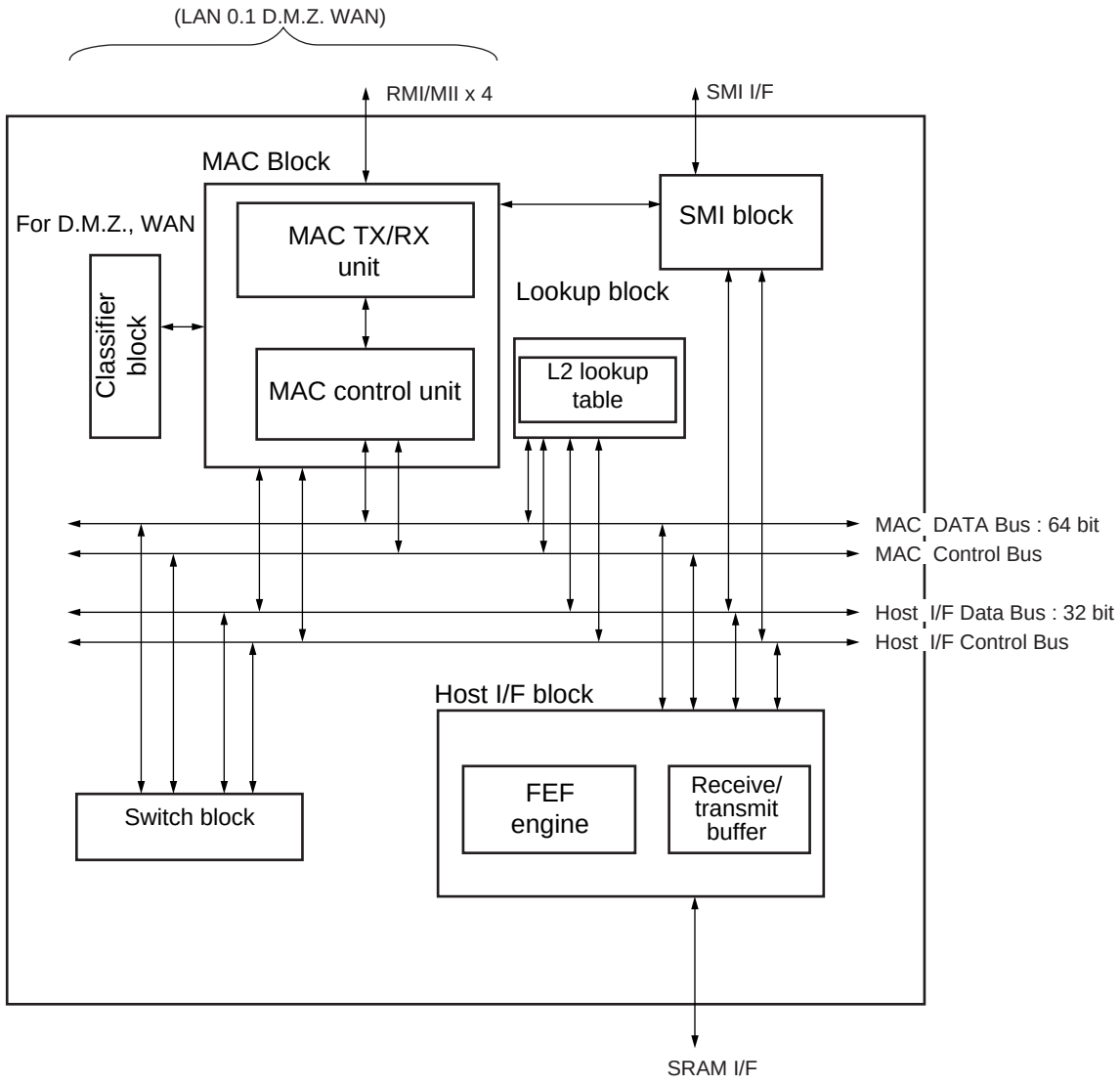
• SMI interface

Pin No.	Pin Name	I/O	Description
155	MDCLK	O	MANAGEMENT DATA CLOCK SMI Clock to PHYs.
162	MDIO	I/O	MANAGEMENT DATA INPUT/OUTPUT SMI Data to/from PHYs.

• Others

Pin No.	Pin Name	I/O	Description
185	SRST_	I	SYSTEM RESET System Reset signal.
172	SCLK	I	SYSTEM CLOCK System clock of this device. Also used as host interface reference clock.
198	TRST	I	Input the “H” level. For any system operation, be sure to input a reset signal to this pin. (Set the signal level to “L” and then to “H”)
199 201 202	TMODE TDIN TCLK	I	Input the “H” level.
9, 12, 26 39, 53, 56 64, 67, 81 95, 98, 112 115, 129, 143 146, 156, 159 169, 186, 203 206	VDDE	—	3.3 V power supply pin.
11, 14, 28 41, 55, 58 66, 69, 83 97, 100, 114 117, 131, 145 148, 158, 161 171, 188, 205 208	VDDI	—	1.8 V power supply pin.
10, 13, 27 40, 54, 57 65, 68, 73 82, 87, 96 99, 106, 113 116, 121, 130 135, 144, 147 154, 157, 160 163, 165, 170 187, 195, 197 204, 207	VSS	—	Ground pins.
189 to 194 196 200	SDI1 to SDI6 XTCK VPD	—	Ground pins.
1 2 to 7	TDOUT SDO1 to SDO6	NC	Leave this open.

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

1. MAC block

The MAC block transmits and receives packets through the RMII or MII Interfaces, and performs Layer 2 (MAC) functions as defined in IEEE 802.3. The MAC block transfers the received frames to the switch block, and transmits frames received from the switch block to the output interface.

2. SMI block

The SMI Block gathers various information (such as Full/Half Duplex, Link Status,10/100 Base, etc.) by reading the PHY device registers through the SMI Interface, and configures the PHY device by writing through the SMI Interface.

3. Switch block

The Switch block stores packets received from the MAC block in RAMs (PRAM) , and transfers the packets to the destination interface based on the information acquired from the Lookup block.

4. Lookup block

The Lookup block looks up the MAC Address of the packet received from the MAC block, and returns destination interface information to the switch block.

5. Classifier block

The classifier block is used to determine the priority of the packets to be transferred between the WAN and D.M.Z. ports. The packets can be classified into two priorities (high or low) by the classifier block. Packets classified as high are placed in the high priority queue, and are processed by the switch block before the low priority packets.

6. Host interface block

The Host Interface block contains the FEF Engine and other minor blocks. The FEF Engine forwards packets between interfaces and transmits packets to/from the host. The Host Interface is also used to read/write from/to the internal registers. When the MB86977 receives packets destined for the host, the host interface asserts an interrupt signal and specifies the information in the status register. The host transmits packets by writing a descriptor to an internal register with the information necessary to transmit.

The host interface block has two 3K Byte integrated dual port RAMs that can be randomly accessed for transmitting and receiving packets. The host interface can be accessed like a General-purpose SRAM.

■ FUNCTIONAL DESCRIPTION

1. FEF Engine-NAT/IP forwarding function

The FEF Engine-NAT/IP forwarding macro accelerates NAT transformation and IP forwarding through hardware, eliminating the use of software, i.e. host processing. Up to 128 NAT/IP forwarding connections, each defined by the parameters set in the NAT/IP forwarding table, can be configured. These connections are the transmission paths that connect the WAN and D.M.Z. interfaces, the WAN and LAN interfaces, and the D.M.Z. and LAN interfaces-all at full wire speed.

The IP forwarding and NAT operations are briefly explained below.

• IP Forwarding

When both the destination and source IP addresses of an input packet matches one of the entries in the NAT/IP forwarding table, the packet is forwarded through hardware to the destination interface indicated by the matching entry. This transmission does not require host processing and is performed at full wire speed. If there is no entry in the NAT/IP forwarding table that matches both IP addresses (destination and source IP address) of the input packet, the packet is sent to the host through the host interface.

Described below is the operation performed on the packet when IP Forwarding is being applied:

- MAC address replacement
- TTL subtraction
- IP header checksum recalculation
- Ethernet frame CRC recalculation
- Transmission from the destination interface indicated

As for IP forwarding, both IPv4 and IPv6 type packets can be processed.

• NAT

When the destination and source IP addresses and the destination and source TCP/UDP port numbers of an input packet matches one of the entries in the NAT/IP forwarding table, the hardware translates the address, replaces the port numbers, and forwards the packet to the destination interface, all according to the parameters defined by the matching entry. This transmission does not require host processing and is performed at full wire speed. If there is no entry in the NAT/IP forwarding table that matches both IP addresses (destination and source IP address) and both TCP/UDP port numbers of the input packet, the packet is sent to the host through the host interface.

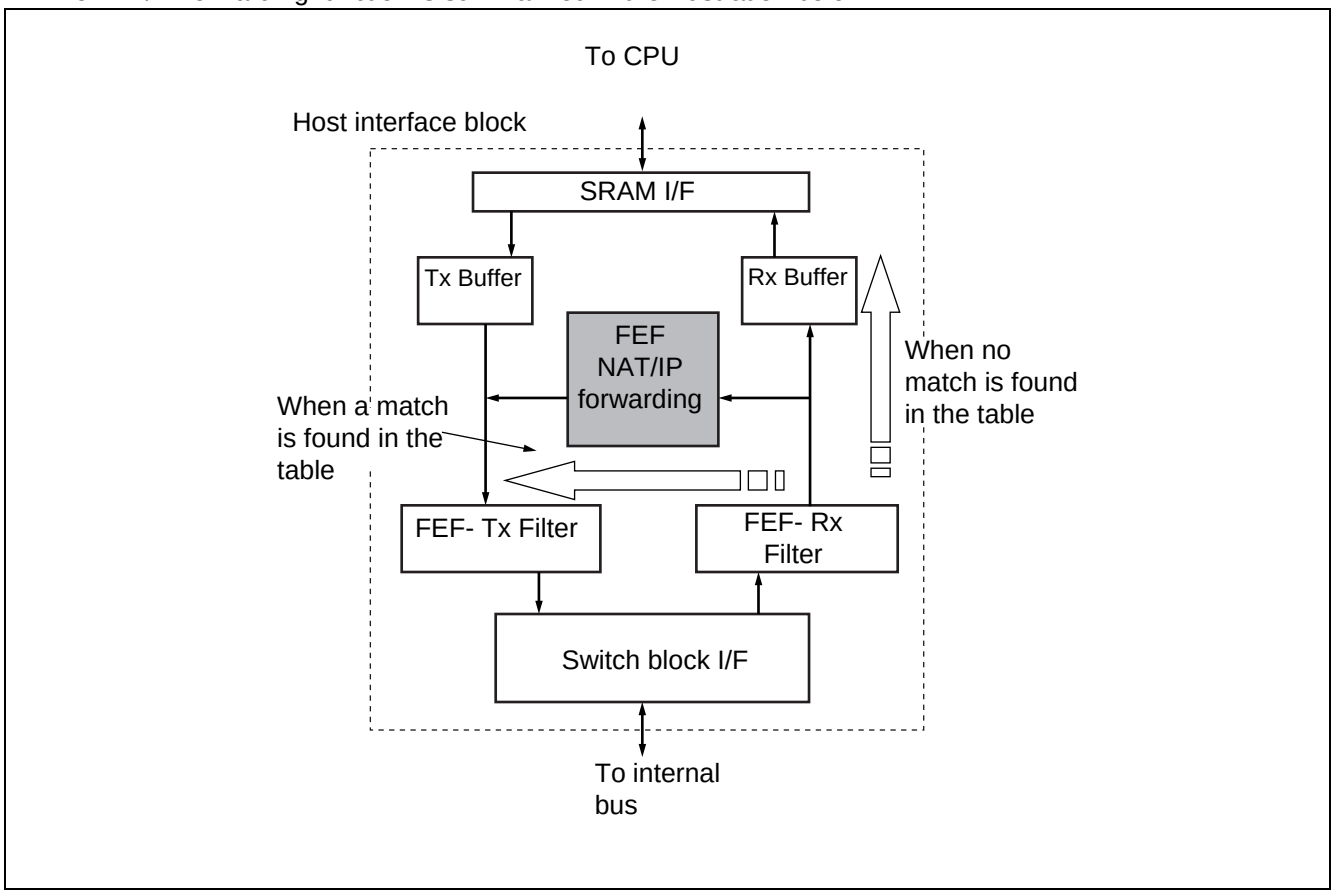
Described below is the operation performed on the packet when NAT is being applied:

- MAC address replacement
- TTL subtraction
- IP address replacement
- IP header checksum recalculation
- TCP/UDP port number replacement
- TCP/UDP header checksum recalculation
- Ethernet frame CRC recalculation
- Transmission from the destination interface indicated

As for NAT, only IPv4 type packets can be processed.

AH and ESP input packets are not subject to NAT translations.These types of packets are sent to the host through the host interface.

The NAT/IP forwarding function is summarized in the illustration below.



NAT/IP Forwarding Function Overview

2. FEF Engine-header processing function

This device implements the processing of PPPoE and IPv6 over IPv4 tunnel packets through hardware.

When an input packet is one of the four types shown in the figure below, its parameters are compared with parameters in the NAT/IP forwarding table. If one of the entries matches it, this device performs NAT/IP forwarding after removing the PPPoE header or v6 over v4 tunnel header by hardware.

When it is required to add one of the four kinds of headers shown in the figure below after performing NAT/IP forwarding, it is necessary for the PPPoE header field, the v4 tunnel header field, the control bit field in the NAT/IP forwarding table to be specified appropriately. Also, the PPPoE header register or v4 tunnel header has to be set properly.

The packet length is not checked after these headers are added. If the original packet length is long enough, the output packet may be larger than the desired MTU of the connection. To prevent this situation, the MTU value of the packets that will be received by this device that are transmitted by the networking device must be set carefully.

Only IP packets can be processed by hardware. LCP and IPCP packet sent during the PPPoE discovery or session stages are sent to the host through the host interface block.

IPv6 over IPv4

Ether header	IPv4 tunnel header	IPv6 header	Data (TCP/UDP)	CRC

IPv6 over PPPoE

Ether header	PPPoE header	PPP header	IPv6 header	Data (TCP/UDP)	CRC

IPv4 over PPPoE

Ether header	PPPoE header	PPP header	IPv4 header	Data (TCP/UDP)	CRC

IPv6 over IPv4 over PPPoE

Ether header	PPPoE header	PPP header	IPv4 tunnel header	IPv6 header	Data (TCP/UDP)	CRC

Packet Formats Supported by Header Processing Function

3. FEF Engine-filtering function

• Filtering

Filtering can be applied to packets that are forwarded between differing segments, i.e. the D.M.Z. and LAN, the D.M.Z. and WAN, and the WAN and LAN segments. Filtering is executed based on the following information.

- Protocol type (Type field in Ethernet)
- IP address
- TCP/UDP port number
- ICMP message type

There are two filters, one for inbound packets, and the other for outbound packets.A maximum of 64 entries can be set per filter. Filtering can be applied to both IPv4 and IPv6 packets. Filtering can also be executed on packets that include IP frames such as PPPoE session stage packets. In addition, filtering can also be applied to the L3/L4 information of AH packets, and the IP addresses of ESP type IPsec packets. The relation between the filter and FEF is shown in “NAT/IP forwarding function overview”. When the Host Interface block receives a packet from the switch block, it is first checked by the Rx filter and then forwarded to the NAT/IP forwarding block. The Tx filter is applied after the packet has been processed by the NAT/IP forwarding block.

• Filter Logging

This device can record several characteristics of the packets dropped by the filters. There are counters that can record the number of packets dropped, and buffers that can store the first 60 Bytes of up to four packets that were dropped by the filters.

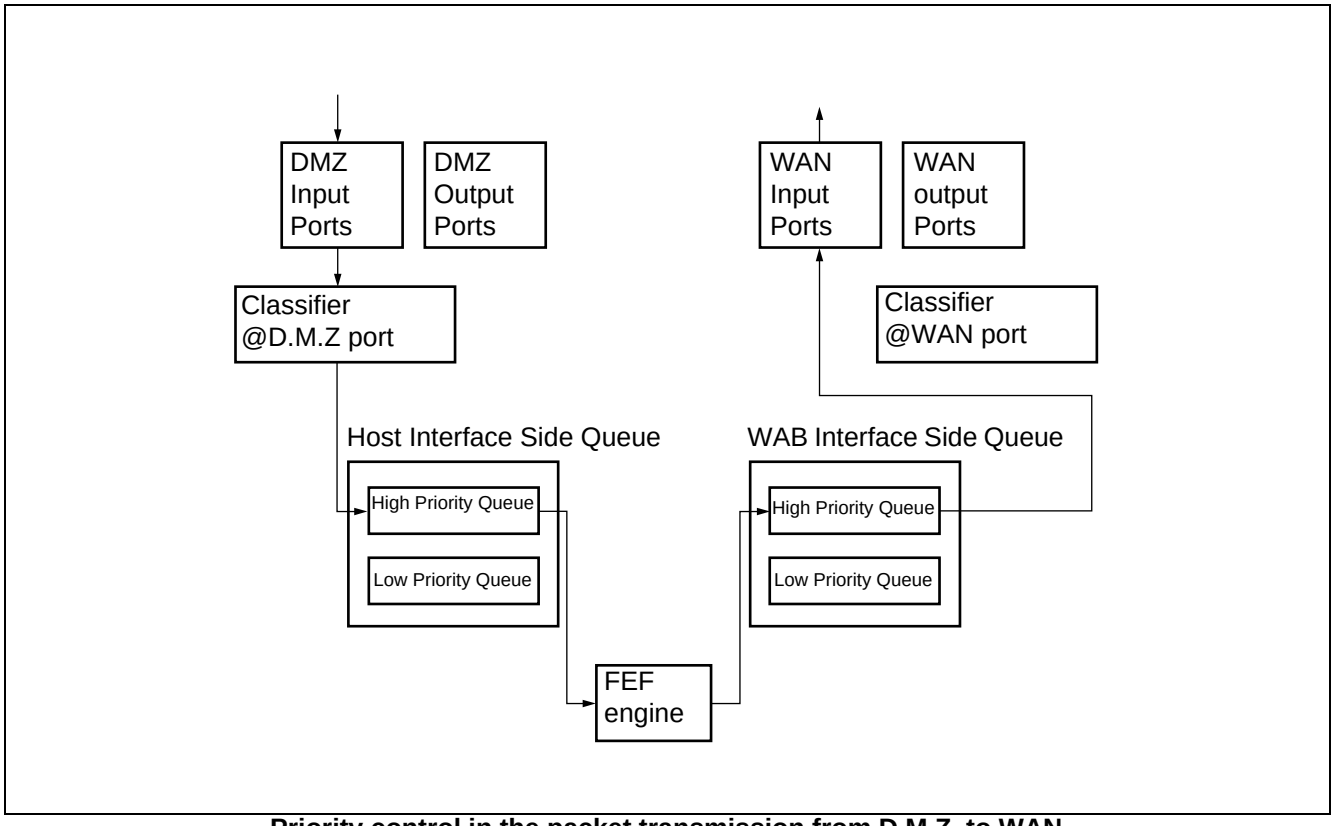
Each of the 64 filter Table entries (for both the input and output filters) has a counter that can count up to 255. If the counter overflows, it is informed to the host by asserting an interrupt signal. The host may poll the counter instead if required.

The buffers that store the headers of the packets (i.e. the first 60 bytes of the packet) can be configured to have the packets that match the condition (1) constantly overwrite the previously stored packet data, or (2) not overwrite the previously stored packets but assert the interrupt signal as soon as all four buffers have been occupied.

4. FEF Engine-priority control function

Priority control can be applied to D.M.Z. and WAN connections through the cooperation of the FEF engine, priority queues in the switch block, and the classifier block. Priority control is best recommended for applications such as VoIP where small jitter and minimal delay are required. The switch block forms both high and low priority queues as shown in the figure below. The low priority queue is used for the transmission of packets with normal priority such as data packets. The high priority queue is used for applications such as VoIP where high transmission quality is required. The classifier block determines the priority of an IP packet by referring the fields of the packet to the corresponding settings in the priority control table.

Below explains the operation of the classifier block when a packet is transmitted from the D.M.Z. to WAN. First, the classifier block defines the priority of the packet received at the D.M.Z. interface.If the packet is classified as high priority, the packet is linked to the high priority queue destined for the host interface block. The high priority queue is serviced prior to the low priority queue, and FEF processing is carried out on the packet. Since in this case the NAT/IP forwarding table has defined the WAN High Priority Interface as the packet destination, the FEF will process the packet and link it to the high priority queue destined for the WAN. This WAN high priority queue will be serviced at top priority.Packet transmission from the WAN to the D.M.Z. interface is also performed in the same manner.



Priority control in the packet transmission from D.M.Z. to WAN.

5. L2 Switch Function

The L2 switching is possible by the MAC address base between ports for LAN. The processing of FEF is not needed in the same segment, and the processing load of FEF reduced.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{DDI}*1	V_{SS} – 0.5	+ 2.5	V
	V_{DDE}*2	V_{SS} – 0.5	+ 4.0	V
Input voltage	V_I	V_{SS} – 0.5	V_{DDE} + 0.5	V
Output voltage	V_O	V_{SS} – 0.5	V_{DDE} + 0.5	V
Storage temperature	T_{stg}	– 55	+ 125	°C
Operation junction temperature	T_j	– 40	+ 125	°C
Output current	I_O	– 4	+ 4	mA

*1 : 1.8 V

*2 : 3.3 V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DDI}	1.65	1.8	1.95	V
	V_{DDE}	3.0	3.3	3.6	V
H level input voltage	V_{IH}	2.0	—	V_{DDE} + 0.3	V
L level input voltage	V_{IL}	– 0.3	—	0.8	V
Operating temperature	Ta	– 20	—	85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

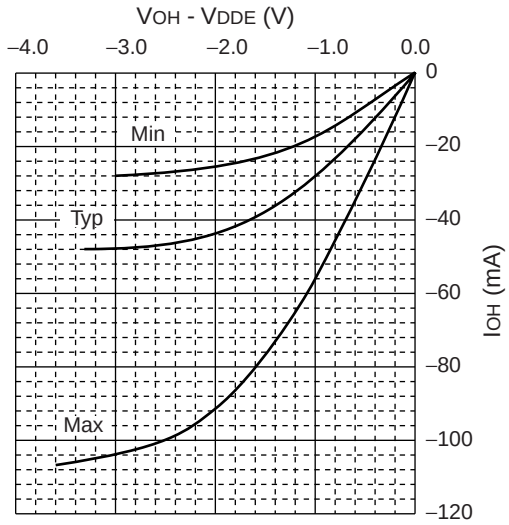
3. DC Characteristics

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

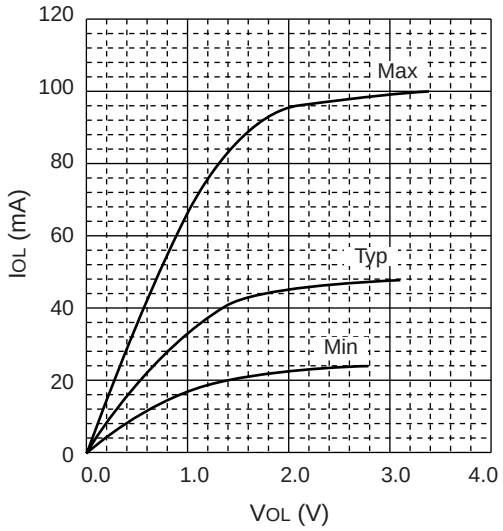
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
power supply current	I_{DD}	Operation state	—	450	700	mA
	I_{DDS}	Static state	—	—	10	mA
H level output voltage	V_{OH}	H level output current I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
L level output voltage	V_{OL}	L level output current I_{OL} = − 100 µA	0	—	0.2	V
H level output V-I characteristics	—	V_{DDE} = 3.3 V ± 0.3 V	*			—
L level output V-I characteristics	—	V_{DDE} = 3.3 V ± 0.3 V	*			—
Input leak current	I_L	—	− 5	—	+ 5	µA

* : Refer to the figures below.

H level output V-I characteristics



L level output V-I characteristics

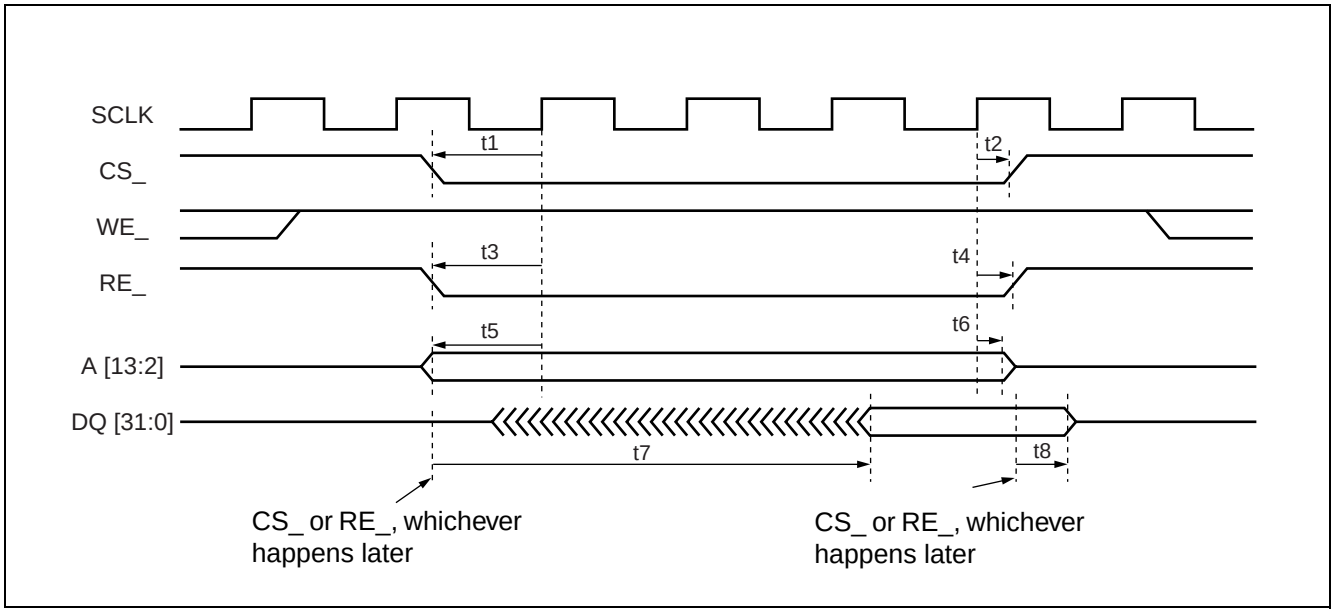


4. AC Characteristics

(1) Host interface data read timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

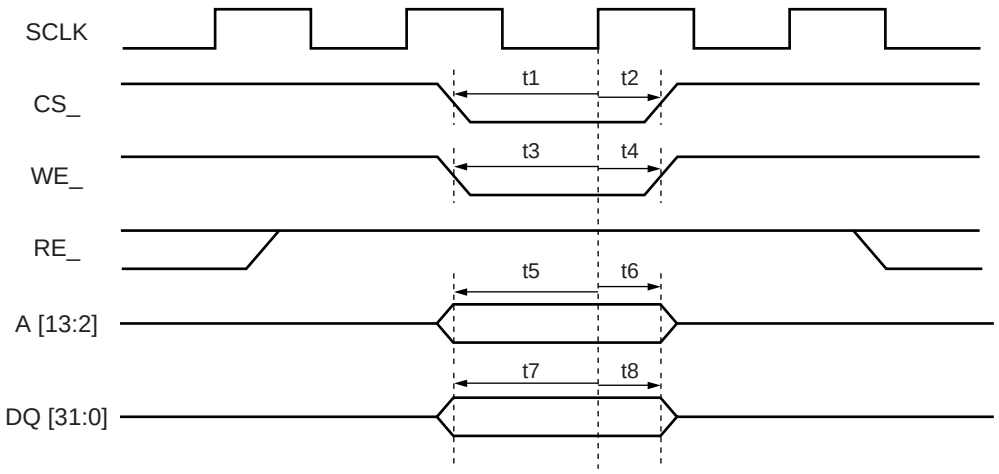
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
chip select input setup time	t_1	5	—	—	ns
chip select input hold time	t_2	5	—	—	ns
Read enable input setup time	t_3	5	—	—	ns
Read enable input hold time	t_4	5	—	—	ns
Address Input setup time	t_5	5	—	—	ns
Address Input hold time	t_6	5	—	—	ns
Read data output delay time	t_7	—	—	42	ns
Read data output hold time	t_8	—	—	42	ns



(2) Host interface data write timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

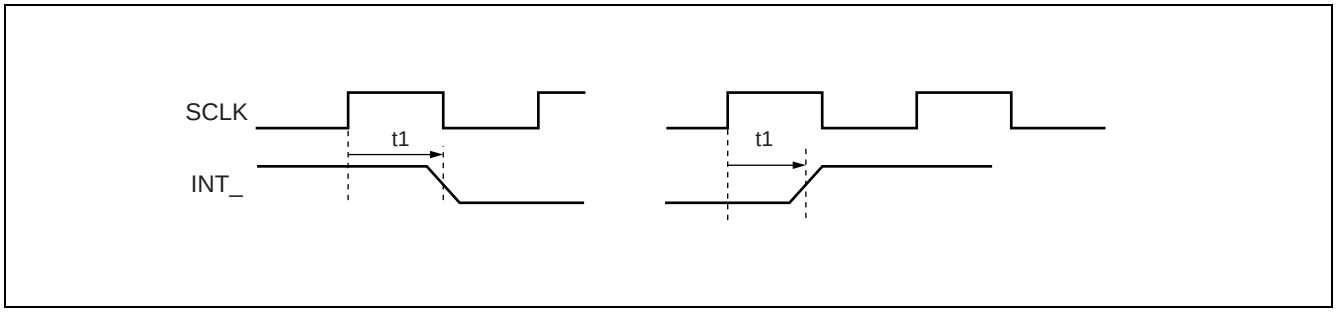
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
chip select input setup time	t_1	5	—	—	ns
chip select input hold time	t_2	5	—	—	ns
Write Enable input setup time	t_3	5	—	—	ns
Write Enable input hold time	t_4	5	—	—	ns
Address Input setup time	t_5	5	—	—	ns
Address Input hold time	t_6	5	—	—	ns
Write data input setup time	t_7	5	—	—	ns
Write data input hold time	t_8	5	—	—	ns



(3) Host interface interrupt timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

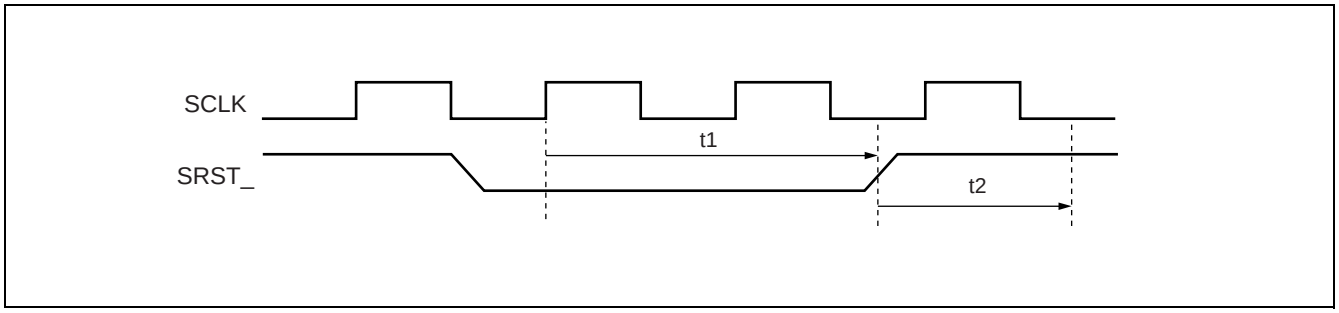
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Interrupt signal output delay time	t_1	—	—	15	ns



(4) Reset Timings

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

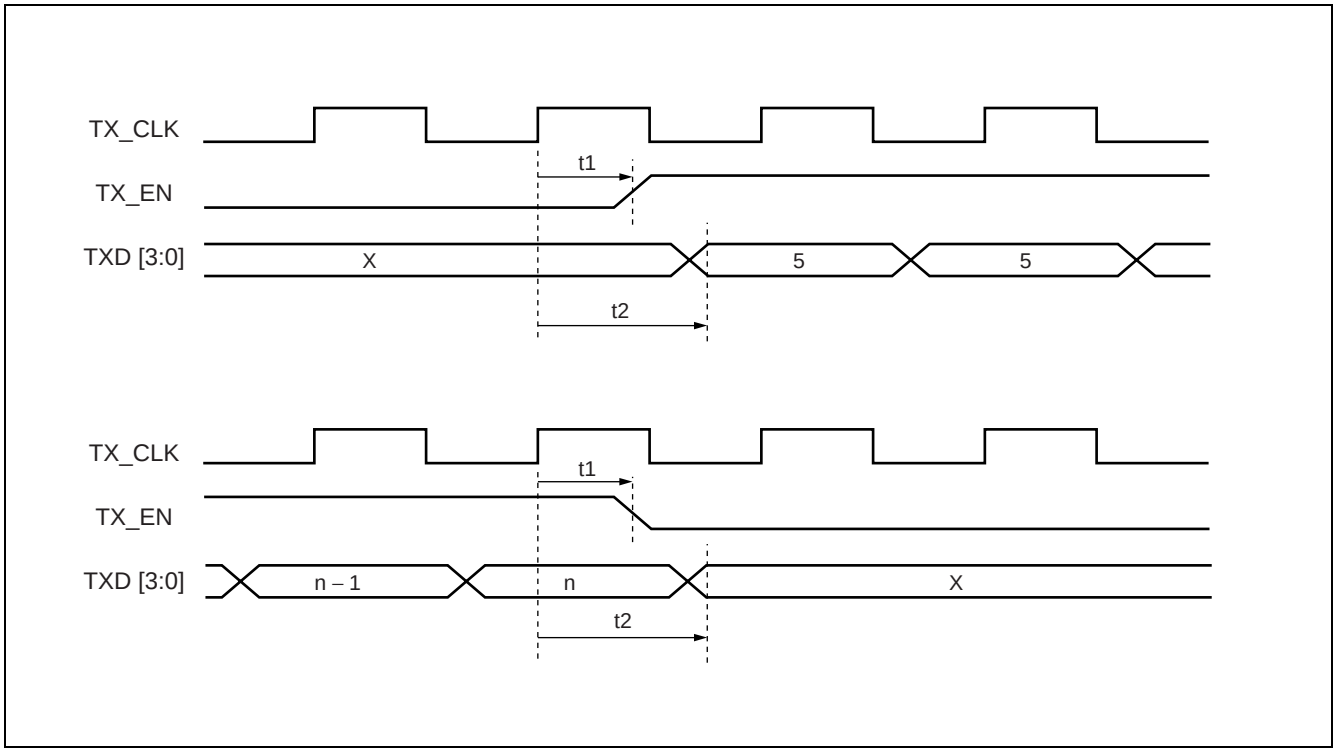
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Reset assert time	t_1	5	—	—	Clock cycle
Access barred time after reset deassertion	t_2	1000	—	—	Clock cycle



(5) MII interface data transmission timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

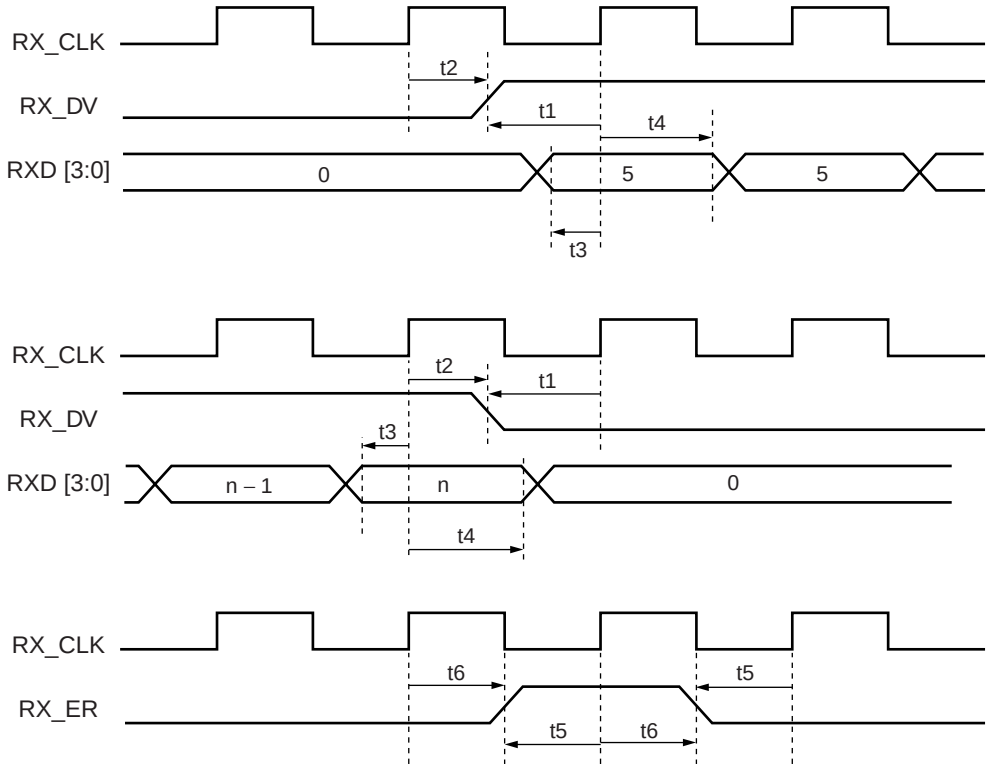
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
TX_EN output delay time	t_1	—	—	20	ns
TXD output delay time	t_2	—	—	20	ns



(6) MII interface data reception timing

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

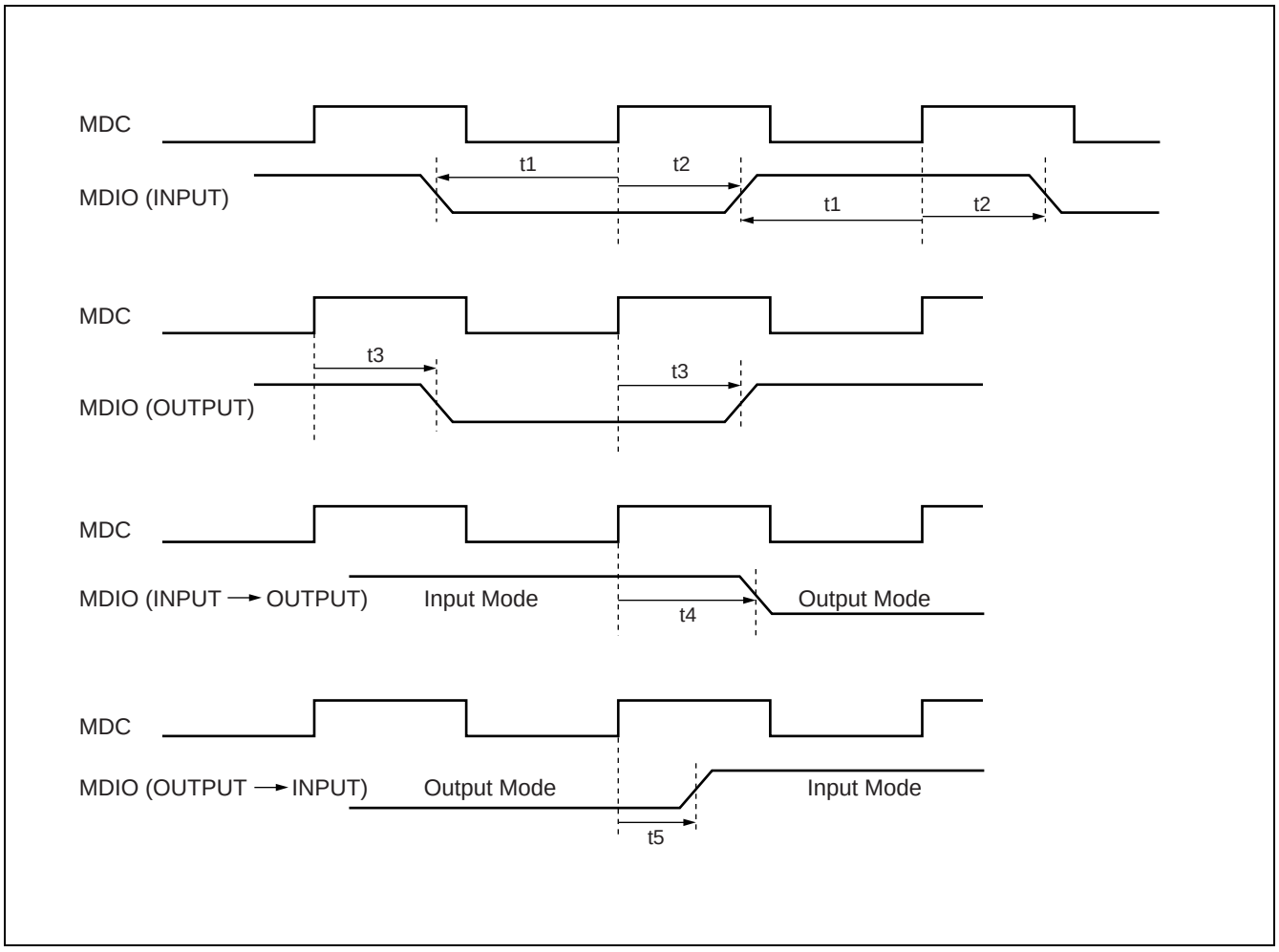
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RX_DV input setup time	t_1	3	—	—	ns
RX_DV input hold time	t_2	3	—	—	ns
RXD input setup time	t_3	3	—	—	ns
RXD input hold time	t_4	3	—	—	ns
RX_ER input setup time	t_5	3	—	—	ns
RX_ER input hold time	t_6	3	—	—	ns



(7) SMI Interface

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

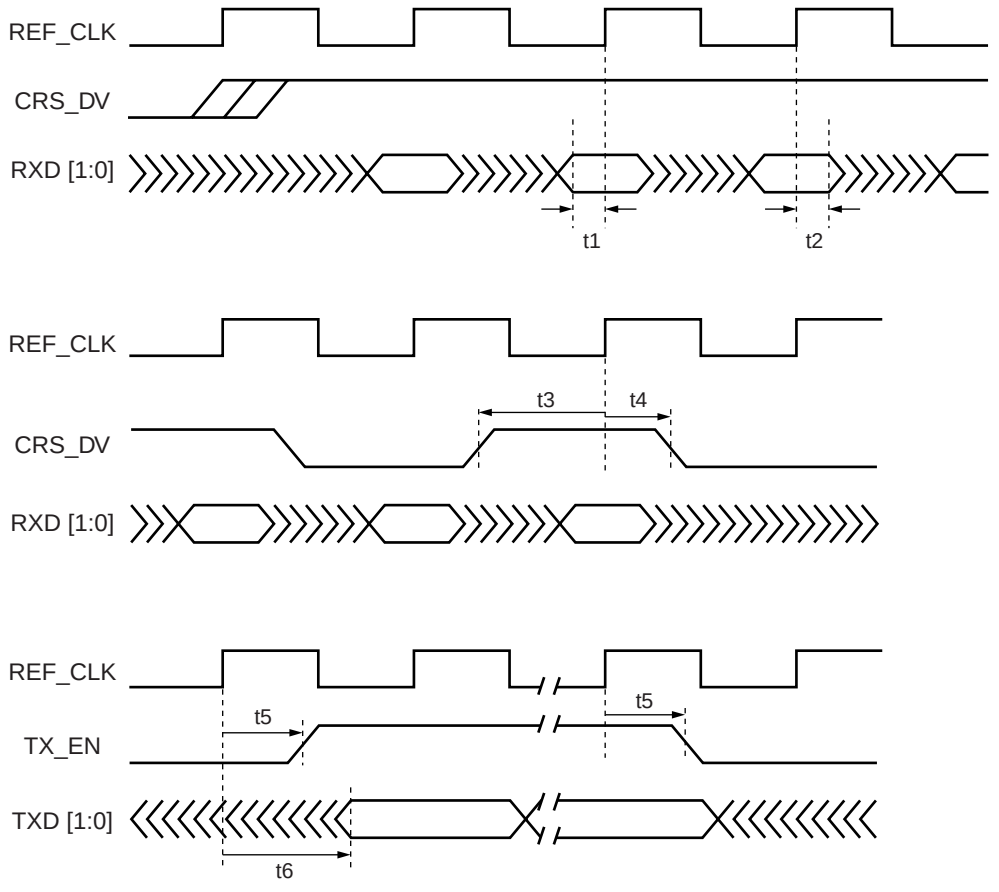
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
SMI data input setup time	t_1	20	—	—	ns
SMI data input hold time	t_2	20	—	—	ns
SMI data output delay time	t_3	—	—	100	ns
SMI turn-on delay time (Input mode → Output mode)	t_4	—	—	100	ns
SMI turn-off delay time (Output mode → Input mode)	t_5	—	—	100	ns



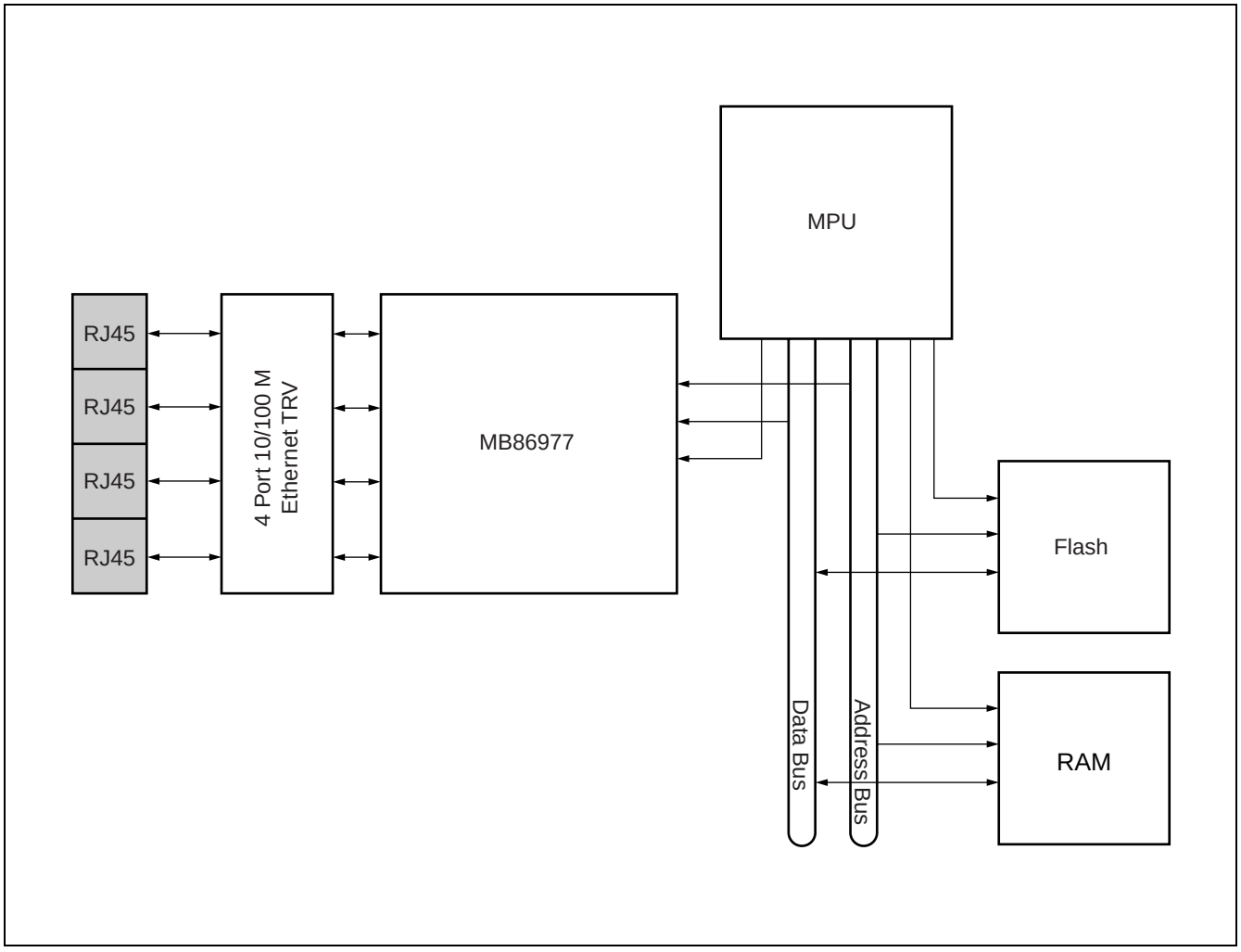
(8) RMII Interface

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V, V_{SS} = 0 V, Ta = − 20 °C to + 85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
RXD input setup time	t_1	4	—	—	ns
RXD input hold time	t_2	4	—	—	ns
CRS_DV input setup time	t_3	4	—	—	ns
CRS_DV input hold time	t_4	4	—	—	ns
TX_EN output delay time	t_5	—	—	15	ns
TXD output delay time	t_6	—	—	15	ns



■ SYSTEM CONFIGURATION



■ NOTES ON HARDWARE SETTING

This section describes the sequence of On/Off of the power supply.

Though the sequence of On/Off is not restricted, the following sequences are recommended.

Power-ON sequence:

1) VDDI

2) VDDE

3) Signal

Power-Off sequence:

1) Signal

2) VDDE

3) VDDI

Notes :
- VDDE should not be supplied with signals while VDDI is off; otherwise a through current may flow, causing potential reliability problems of the LSI.
- When switching VDDE from off to on, it is possible that the internal state of the circuit is not be maintained due to power source noises. Therefore, the circuit should be initialized.
- The circuit should be initialized after power-ON.

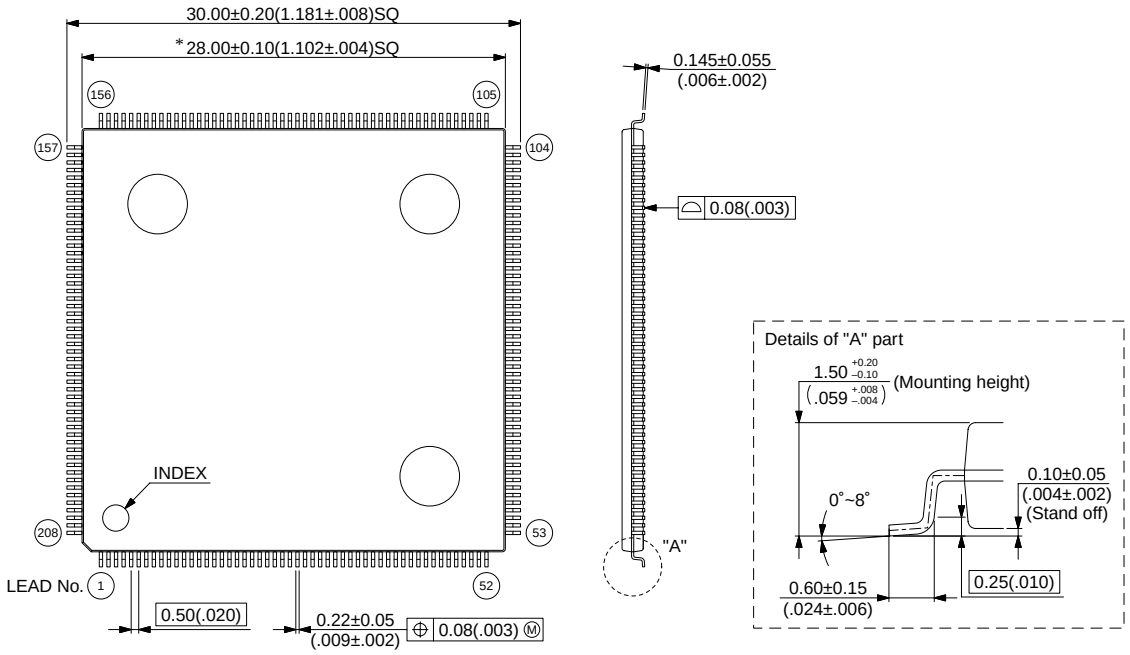
■ ORDERING INFORMATION

Part number	Package	Remarks
MB86977PFV-G-BND	208 - pin plastic LQFP (FPT-208P-M06)	

■ PACKAGE DIMENSION

208-pin plastic LQFP
(FPT-208P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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