



SANYO Semiconductors

DATA SHEET

LB11993W — Monolithic Digital IC

For Digital Video Camera

Three-phase Brushless 3-in-1 Motor Driver

Overview

The LB11993W is a 3-phase brushless motor driver for digital video camera. It integrates, on a single chip, three motor driver functions (for capstan, drum, and loading motors) for driving a tape. This IC also includes 4-channel operation amplifiers (2 channels for reel and 2 channels for general purpose), which significantly reduces the number of peripheral components required.

Functions

- Capstan unit
 - Voltage linear drive
 - Built-in torque ripple compensation circuit
 - FG amplifier
- Drum unit
 - Current drive
 - Sensorless drive
 - FG amplifier
 - PG amplifier
- Loading unit
 - 2-channel reel amplifiers
- Common unit
 - Thermal shutdown circuit
 - 2-channel OP amplifiers

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LB11993W

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------------|----------------|----------------------|-----------------------|------------------|
| Supply voltage 1 | V_{CC1} max | | 7 | V |
| Supply voltage 2 | V_{CC2} max | | 9.0 | V |
| Supply voltage 3 | V_{S_C} max | Capstan motor driver | 7.0 | V |
| Supply voltage 4 | V_{S_D} max | Drum motor driver | 7.0 | V |
| Supply voltage 5 | V_{S_L} max | Loading motor driver | 7.0 | V |
| Output voltage | V_O max | | 9.0 | V |
| Input voltage | V_{I1} max | Control system | -0.3 to $V_{CC1}+0.3$ | V |
| | V_{I2} max | U, V, W, COM | 9.0 | V |
| Capstan output current | I_{OC} max | | 1.0 | A |
| Drum output current | I_{OD} max | | 1.0 | A |
| Loading output current | I_{OL} max | | 0.6 | A |
| Internal power dissipation | P_d max | Independent IC | 0.6 | W |
| Operating temperature | T_{opr} | | -20 to +75 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

Recommended Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|------------|-------------------------|----------------------|-------|
| Supply voltage 1 | V_{CC1} | $V_{CC1} \leq V_{CC2}$ | 2.7 to 6.0 | V |
| Supply voltage 2 | V_{CC2} | | 3.5 to 8.5 | V |
| Supply voltage 3 | V_{S_C} | $V_{S_C} \leq V_{CC2}$ | up to 6.5 | V |
| Supply voltage 4 | V_{S_D} | $V_{S_D} \leq V_{CC2}$ | up to 6.5 | V |
| Supply voltage 5 | V_{S_L} | $V_{S_L} \leq V_{CC2}$ | 2.2 to 6.5 | V |
| Hall input amplitude | V_{HALL} | Capstan motor | ± 20 to ± 80 | mVp-p |

Electrical Characteristics / Capstan motor driver block at $T_a = 25^\circ\text{C}$, $V_{CC1}=3\text{V}$, $V_{CC2}=4.75\text{V}$, $V_S=1.5\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------|-------------------|--|---------|------|-----------|---------------|
| | | | min | typ | max | |
| [Supply currents] | | | | | | |
| V_{CC1} supply current | I_{CC1} | $I_{OUT}=100\text{mA}$ $V_{STBY_C}=3\text{V}$ | | 5.6 | 10 | mA |
| V_{CC2} supply current | I_{CC2} | $I_{OUT}=100\text{mA}$ $V_{STBY_C}=3\text{V}$ | | 6 | 12 | mA |
| V_{CC1} quiescent current | I_{CC1Q} | $V_{STBY_C}=0\text{V}$ | | 3.3 | 5 | mA |
| V_{CC2} quiescent current | I_{CC2Q} | $V_{STBY_C}=0\text{V}$ | | | 100 | μA |
| V_S quiescent current | I_{SQ} | $V_{STBY_C}=0\text{V}$ | | 75 | 100 | μA |
| [VX1] | | | | | | |
| Upper-side residual voltage | V_{XH1} | $I_{OUT}=0.2\text{A}$ | | 0.22 | 0.28 | V |
| Lower-side residual voltage | V_{XL1} | $I_{OUT}=0.2\text{A}$ | | 0.22 | 0.28 | V |
| [VX2] | | | | | | |
| Upper-side residual voltage | V_{XH2} | $I_{OUT}=0.5\text{A}$ | | 0.3 | 0.4 | V |
| Lower-side residual voltage | V_{XL2} | $I_{OUT}=0.5\text{A}$ | | 0.3 | 0.4 | V |
| Output saturation voltage | $V_{O\text{sat}}$ | $I_{OUT}=0.8\text{A}$, Sink+Source | | | 1.3 | V |
| Amount of overlap | O.L | $R_L=39\Omega \times 3$, $R_{\text{angle}}=20\text{k}\Omega$, Note 2 | 70 | 80 | 90 | % |
| [Hall amplifier] | | | | | | |
| Input offset voltage | V_{HOFF} | Design target value* | -5 | | +5 | mV |
| Common-mode input range | V_{HCM} | $R_{\text{angle}}=20\text{k}\Omega$ | 0.95 | | 2.1 | V |
| Input/output voltage gain | V_{GVH} | $R_{\text{angle}}=20\text{k}\Omega$ | 25 | 27.5 | 30.5 | dB |
| [Standby pin] | | | | | | |
| High-level voltage | V_{STH} | | 2.5 | | V_{CC1} | V |
| Low-level voltage | V_{STL} | | -0.2 | | 0.7 | V |
| Input current | I_{STIN} | $V_{STBY_C}=3\text{V}$ | | | 50 | μA |
| Leakage current | I_{STLK} | $V_{STBY_C}=0\text{V}$ | -30 | | | μA |

Continued on next page.

LB11993W

Continued from preceding page.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------|--------|----------------------------------|---------|------|------------------|------|
| | | | min | typ | max | |
| [FRC pin] | | | | | | |
| High-level voltage | VFRCH | | 2.5 | | V _{CC1} | V |
| Low-level voltage | VFRCL | | -0.2 | | 0.4 | V |
| Input current | IFRCIN | VFRC_C=3V | | 20 | 40 | μA |
| Leakage current | IFRCLK | VFRC_C=0V | | | -30 | μA |
| [VH] | | | | | | |
| Hall supply voltage | VHALL | I _H =5mA, VH(+)-VH(-) | 0.83 | 0.93 | 1.03 | V |
| Minus (-) pin voltage | VH(-) | I _H =5mA | 0.90 | 0.97 | 1.04 | V |
| [FG comparator] | | | | | | |
| Input offset voltage | VFGOFF | | -3 | | +3 | mV |
| Input bias current | IbFG | VFGIN+=VFGIN-=1.5V | | | 500 | nA |
| Input bias current offset | ΔIbFG | VFGIN+=VFGIN-=1.5V | -100 | | 100 | nA |
| Common-mode input range | VFGCM | | 1.2 | | 2.5 | V |
| High-level output voltage | VFGOH | When internally pulled up | 2.8 | | | V |
| Low-level output voltage | VFGOL | When internally pulled up | | | 0.2 | V |
| Voltage gain | VGFG | Design target value, Note 1 | | 100 | | dB |
| Output current (sink) | IFGOs | Output pin set to low | | | 5 | mA |

Note 1: Design target value parameters are not tested.

Note 2: The standard for the overlap amount parameter is to report the measured value without change.

Cylinder Motor Driver Block at Ta=25°C, V_{CC1}=3V, V_{CC2}=4.75V, VS=3V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|-------------------|--|---------|------|-----------------------|------|
| | | | min | typ | max | |
| Supply current 4 | I _{CC2} | I _O =76mA, VSTBY_D=3V VSTBY_C=0V | | 0.75 | 2.5 | mA |
| Output quiescent current 4 | I _{CC2Q} | VSTBY_D=VSTBY_C=0V | | | 100 | μA |
| Output quiescent current 5 | IS(D)Q | VSTBY_D=VSTBY_C=0V | | 100 | 300 | μA |
| Output saturation voltage upper side 1 | VOU1 | I _O =0.1A, RF=0.25Ω | | 0.2 | 0.4 | V |
| Output saturation voltage lower side 1 | VOD1 | I _O =0.1A, RF=0.25Ω | | 0.2 | 0.4 | V |
| Output saturation voltage upper side 2 | VOU2 | I _O =0.4A, VS=3V, RF=0.25Ω | | 0.3 | 0.6 | V |
| Output saturation voltage lower side 2 | VOD2 | I _O =0.4A, VS=3V, RF=0.25Ω | | 0.3 | 0.6 | V |
| COM pin common-mode input voltage range | VIC | | 0.3 | | V _{CC2} -0.9 | V |
| Standby pin high-level voltage | VSTBYH | | 2 | | V _{CC1} | V |
| Standby pin low-level voltage | VSTBYL | | -0.2 | | 0.7 | V |
| Standby pin input current | ISTBYH | VSTBY_D=3V | | | 50 | μA |
| Standby pin leakage current | ISTBYL | VSTBY_D=0V | -10 | | | μA |
| FRC pin high-level voltage | VFRCH | | 2 | | V _{CC1} | V |
| FRC pin low-level voltage | VFRCL | | -0.2 | | 0.7 | V |
| FRC pin input current | IFRCI | VFRC_D=3V | | | 50 | μA |
| FRC pin leakage current | IFRCL | VFRC_D=0V | -10 | | | μA |
| Slope pin source current ratio | RSOURCE | ICSLP1SOURCE/ICSLP2SOURCE | -20 | | 20 | % |
| Slope pin sink current ratio | RSINK | ICSLP1SINK/ICSLP2SINK | -20 | | 20 | % |
| CSLP1 source-to-sink current ratio | RCSLP1 | ICSLP1SOURCE/ICSLP1SINK | -35 | | 15 | % |
| CSLP2 source-to-sink current ratio | RCSLP2 | ICSLP2SOURCE/ICSLP2SINK | -35 | | 15 | % |
| Startup frequency | Freq | Cosc=0.1μF, OSC frequency Design target value, Note 1 | | 11.5 | | Hz |
| Phase delay width | Dwidth | Design target value, Note 1 | | 30 | | deg |

Note 1: Design target value parameters are not tested.

LB11993W

FG and PG Amplifier Blocks at Ta=25°C, VCC1=3V, VCC2=4.75V, VS=3V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|------------------------------------|--------|--------------|----------|------|------|------|
| | | | min | typ | max | |
| [FG amplifier] | | | | | | |
| Input offset voltage | VIO | | | ±1 | ±5 | mV |
| Input bias current | IBIN- | | | | 250 | nA |
| Common-mode input voltage range | VICOM | | 1 | | 2 | V |
| Open loop gain | GVFG | f=1kHz | | 55 | | dB |
| Output ON voltage | VOL | When IO=10μA | | | 0.4 | V |
| Output OFF voltage | VOH | When IO=10μA | VCC1-0.5 | | | V |
| Schmitt amplifier hysteresis width | VSHIS | | | 50 | | mV |
| Reference voltage | VREF | | 1.30 | 1.40 | 1.50 | V |
| [PG amplifier] | | | | | | |
| Input offset voltage | VIO | | | ±1 | ±5 | mV |
| Input bias current | IBIN- | | | | 250 | nA |
| Common-mode input voltage range | VICOM | | 1 | | 2 | V |
| Open loop gain | GVPG | f=1kHz | | 55 | | dB |
| Output ON voltage | VOL | When IO=10μA | | | 0.4 | V |
| Output OFF voltage | VOH | When IO=10μA | VCC1-0.5 | | | V |
| Schmitt amplifier hysteresis width | VSHIS | | | 50 | | mV |

Loading Motor Driver Block at Ta=25°C, VCC1=3V, VCC2=4.75V, VS=3V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------------|--------|--|---------|-----|------|------|
| | | | min | typ | max | |
| VCC1 supply current 1 | ICC11 | Standby mode VSTBY_C=VSTBY_D=0V | | 3.3 | 5 | mA |
| VCC1 supply current 2 | ICC12 | Forward/reverse mode VSTBY_C=VSTBY_D=0V | | 14 | 21 | mA |
| VCC1 supply current 3 | ICC13 | Brake mode VSTBY_C=VSTBY_D=0V | | 12 | 18 | mA |
| VCC2 supply current 1 | ICC21 | Standby mode(VCC1=OPEN) VSTBY_C, D=0V | | | 100 | μA |
| VCC2 supply current 2 | ICC22 | Standby mode(VCC1=3.0V) VSTBY_C, D=0V | | | 100 | μA |
| VCC2 supply current 3 | ICC23 | Forward/reverse mode VSTBY_C, D=0V | | 23 | 35 | mA |
| VS_L supply current | IVS_L | Standby mode VSTBY_C, D=0V | | | 20 | μA |
| [Logic inputs] (DEC1 and DEC2 pins) | | | | | | |
| High-level input voltage | VINH | VCC1=2.7 to 4.0V | 2.0 | | VCC1 | V |
| High-level influx current | IINH | VIN=3.0V | | 45 | 100 | μA |
| Low-level input voltage | VINL | VCC1=2.7 to 4.0V | -0.2 | | 0.6 | V |
| Low-level influx current | IINL | VIN=0.6V | | 5 | 10 | μA |
| [Loading motor driver] | | | | | | |
| Output saturation voltage 1 | VOH | IO=200mA (upper and lower composition) | | 0.2 | 0.3 | V |
| Output saturation voltage 2 | VSHIS | IO=400mA (upper and lower composition) | | 0.4 | 0.6 | V |
| [OP-AMP1, OP-AMP2] | | | | | | |
| Input offset voltage | VIO | | | ±1 | ±5 | mV |
| Input bias current | IB | | | | 1 | μA |
| Common-mode input voltage range | VICM | | 1 | | 2 | V |
| Open loop gain | GV1 | | 50 | 55 | | dB |

Continued on next page.

LB11993W

Continued from preceding page.

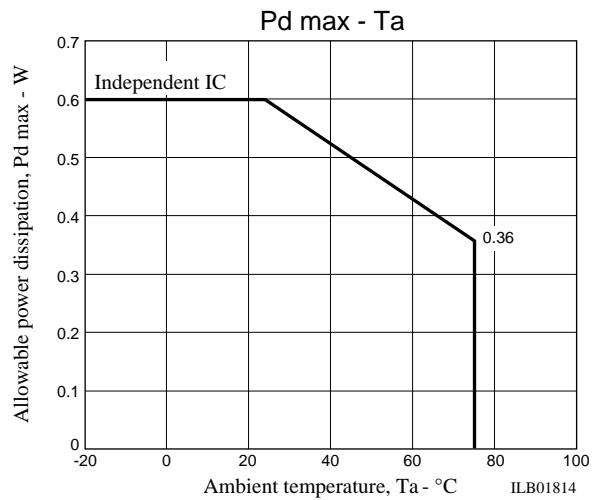
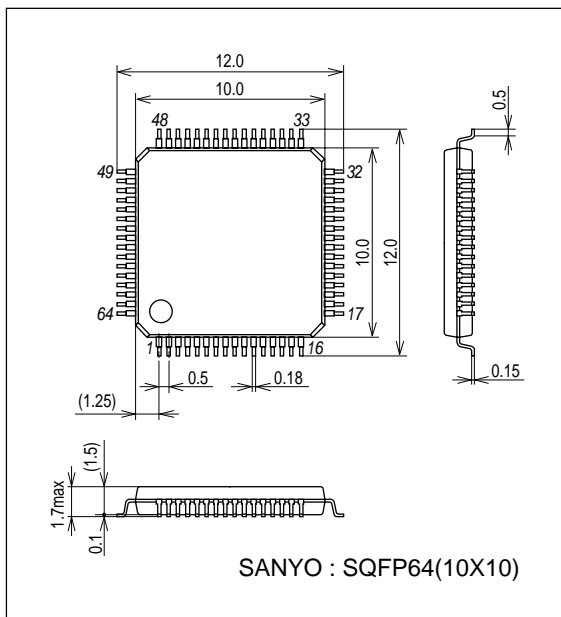
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------------|--------|-----------------------------|---------|-----|-----|------|
| | | | min | typ | max | |
| [OP-AMP3, 4] | | | | | | |
| Input offset voltage | VIO | | | ±1 | ±5 | mV |
| Input bias current | IB | | | | 1 | μA |
| Common-mode input voltage range | VICM | | 1 | | 2 | V |
| Open loop gain | GV1 | | 50 | 55 | | dB |
| [Thermal shutdown circuit] | | | | | | |
| TSD operating temperature | T-TSD | Design target value, Note 1 | 150 | 180 | 210 | °C |
| TSD temperature hysteresis width | ΔTSD | Design target value, Note 1 | | 15 | | °C |

Note 1: Design target value parameters are not tested.

Package Dimensions

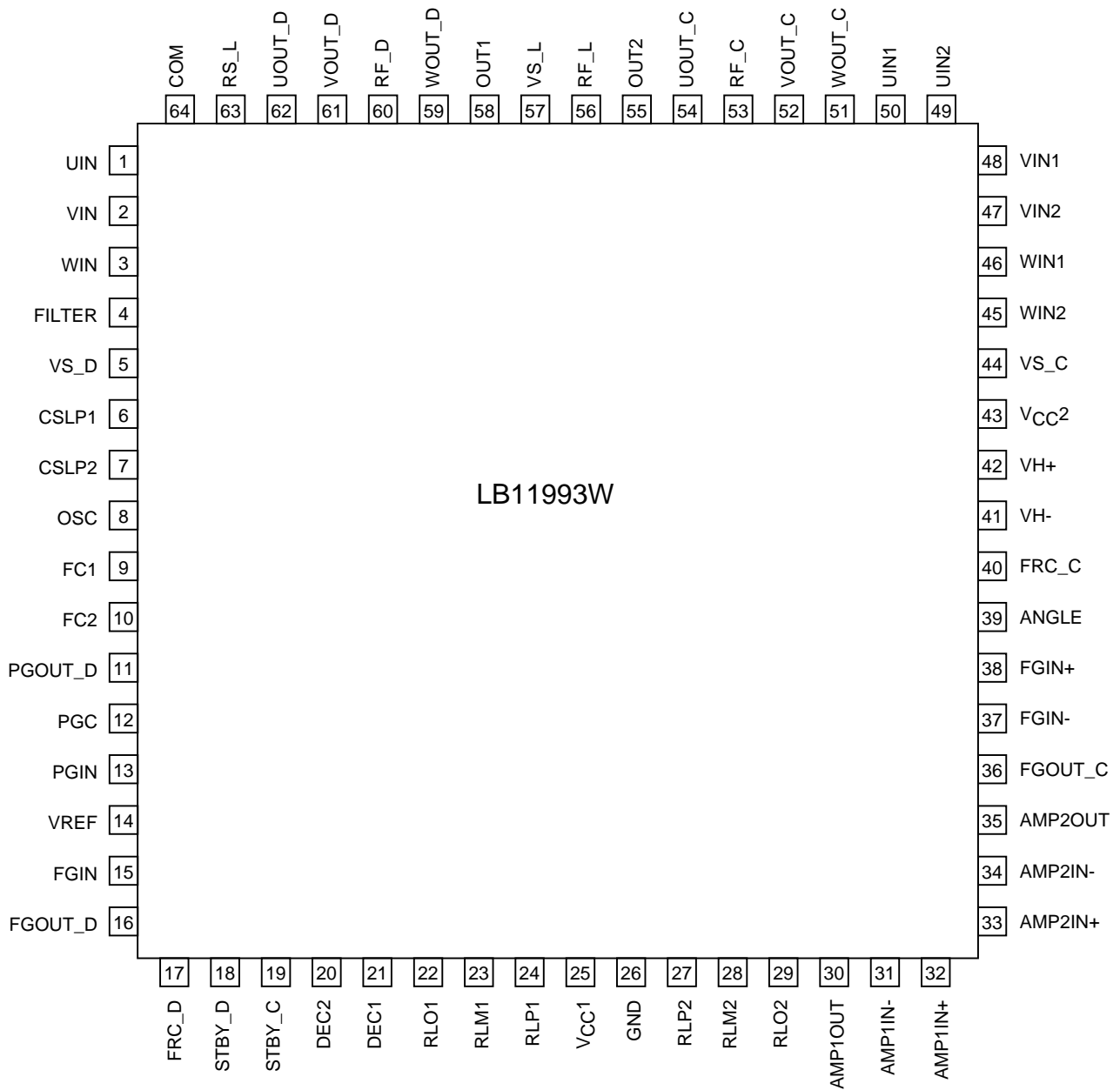
unit : mm (typ)

3190A



LB11993W

Pin Assignment



Top view

Truth Table

Capstan Motor Driver Truth Table

| | Source → Sink | Hall input | | | FRC |
|---|---------------|------------|---|---|-----|
| | | U | V | W | |
| 1 | V → W | H | H | L | H |
| | W → V | | | | L |
| 2 | U → W | H | L | L | H |
| | W → U | | | | L |
| 3 | U → V | H | L | H | H |
| | V → U | | | | L |
| 4 | W → V | L | L | H | H |
| | V → W | | | | L |
| 5 | W → U | L | H | H | H |
| | U → W | | | | L |
| 6 | V → U | L | H | L | H |
| | U → V | | | | L |

Note 1: H in the FR column means the voltage of 2.50V or more while L means the voltage of 0.4V or less.
(at V_{CC1}=3V)

Note 2: For the Hall input, the input H means the condition in which (+) relative to each phase input (-) is higher by 0.02V or more.

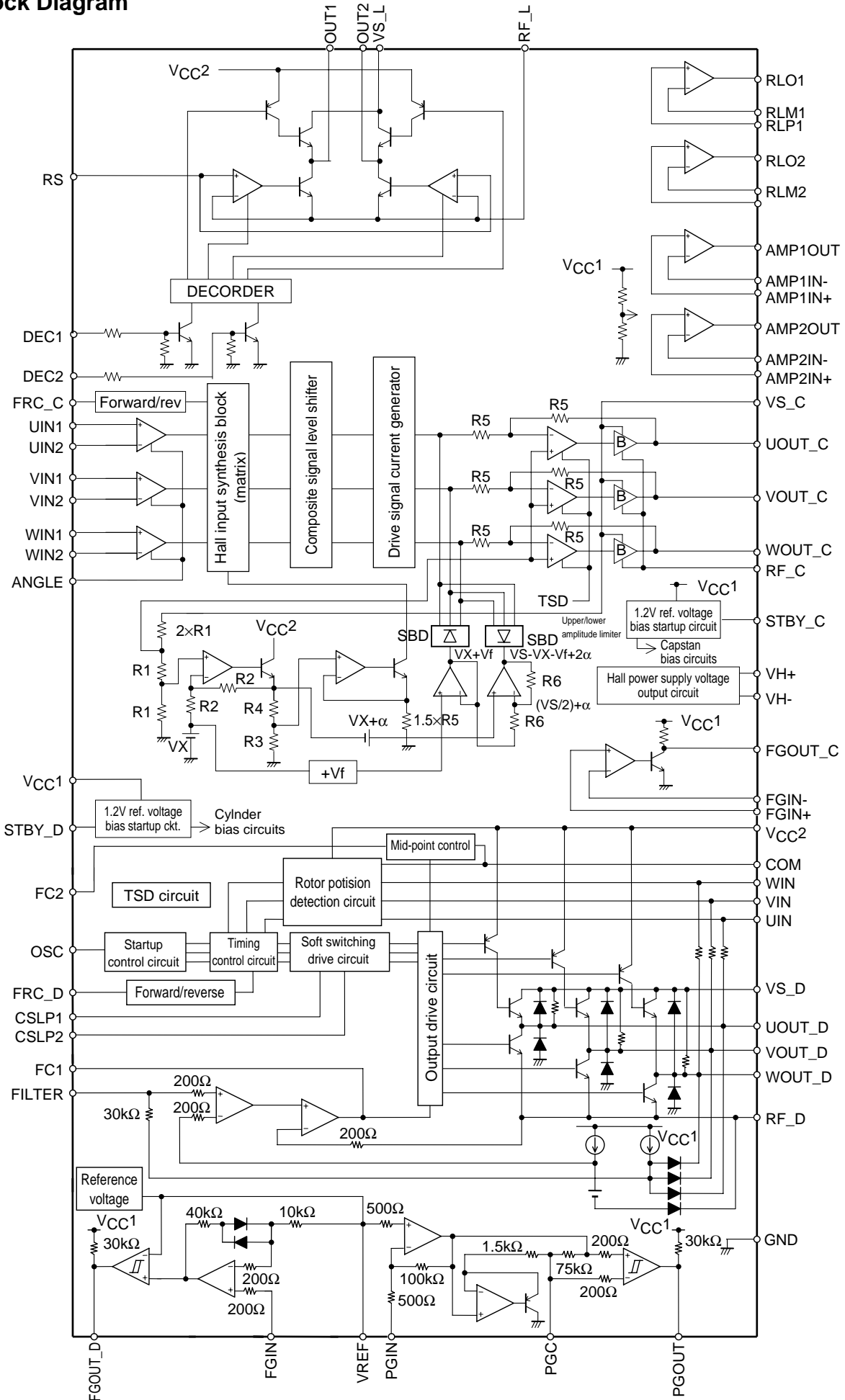
The input L means the condition in which (+) relative to (-) is lower by 0.02V or more.

Loading Motor Driver Truth Table

| Input | | Output | | Mode |
|-------|------|--------|------|---------|
| DEC1 | DEC2 | OUT1 | OUT2 | |
| L | L | Off | Off | Standby |
| H | L | H | L | Forward |
| L | H | L | H | Reverse |
| H | H | L | L | Brake |

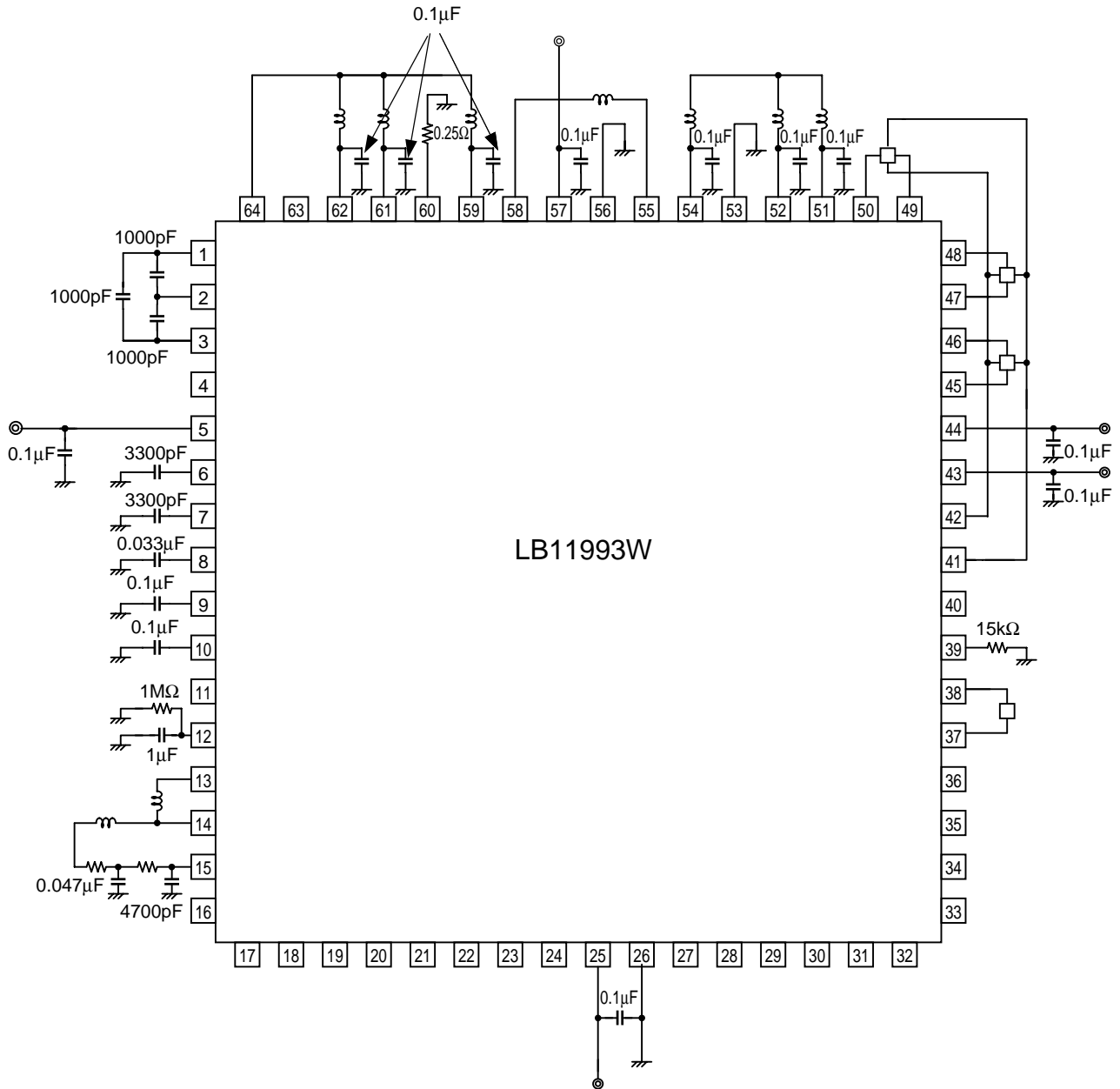
LB1193W

Block Diagram



LB11993W

Sample Application Circuit



Note: The external constant is reference and may vary depending on the motor to be connected.

LB11993W

Pin Description

| Pin No. | Symbol | Voltage | Equivalent Circuit Diagram | Description |
|----------------------------------|--|-----------------------|---|---|
| 50 49 48 47 46 45 | UIN1 UIN2 VIN1 VIN2 WIN1 WIN2 | 0 to V _{CC1} | | Capstan motor driver U, V, and W phase Hall element input/output. IN1 > IN2 state for logic H |
| 39 | ANGLE | | | Hall input/output gain control. Insertion of a resistor between this pin and ground controls the gain. |
| 44 | VS_C | 0 to V _{CC2} | | Power pin that determines the amplitude of the outputs to the capstan motor. The voltage applied to this pin must be lower than V _{CC2} . |
| 54 52 51 53 | UOUT_C VOUT_C WOUT_C Rf_C | | | Capstan motor driver U, V, and W phase output. |
| 42 41 | VH+ VH- | | | Hall element bias voltage supply. A voltage that is typically 0.85V is generated between the VH+ and VH- pins (when I _H = 5mA). |
| 37 38 | FGIN- FGIN+ | 0 to V _{CC1} | | FG comparator inverting input. There is no internally applied bias. |
| 36 | FGOUT_C | | FG comparator noninverting input. There is no internally applied bias. | |
| 40 19 | FRC_C STBY_C | 0 to V _{CC1} | | FG comparator output. There is an internal 20kΩ resistor load. |
| 40 | FRC_C | 0 to V _{CC1} | | Capstan forward/reverse select pin. The voltage on this pin selects forward or reverse rotation. (with hysteresis) |
| 19 | STBY_C | | Pin to select bias supply to capstan circuits other than FG comparator. Setting this pin to low cuts-off the bias supply. Capstan motor standby pin. | |

Continued on next page.

LB11993W

Continued from preceding page.

| Pin No. | Symbol | Voltage | Equivalent Circuit Diagram | Description |
|---------|--------|--|----------------------------|---|
| 13 | PGIN | max2.0V min1.0V (when $V_{CC}=3V$) | | PG amplifier input. Connect PG coil between this pin and VREF. |
| 14 | VREF | | | Internal 1.3V reference voltage. Used as reference voltage for FG and PG amplifiers. |
| 15 | FGIN_D | max2.0V min1.0V (when $V_{CC1}=3V$) | | FG amplifier input. Connect FG coil between this pin and VREF. |
| 18 | STBY_D | 0 to V_{CC1} | | When this pin is at 0.7V or lower or when it is open, only the FG/PG amplifier operates. In the motor drive state, the pin should be at 2V or higher. Drum motor standby pin. |
| 17 | FRC_D | 0 to V_{CC1} | | Drum motor forward/reverse rotation select pin. Low: forward (-0.2V to 0.7V or open) High: reverse (2V to V_{CC1}) |
| 5 | VS_D | 0V to V_{CC2} | | Power supply for determining output amplitude by supplying drum motor voltage. Must be lower than V_{CC2} voltage. |

Continued on next page.

LB11993W

Continued from preceding page.

| Pin No. | Symbol | Voltage | Equivalent Circuit Diagram | Description |
|----------------|----------------------------|------------|----------------------------|--|
| 43 | V _{CC2} | 3.5V to 6V | | Power supply for supplying source side predriver voltage and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors. |
| 25 | V _{CC1} | 2.7V to 6V | | Power supply for circuits except motor voltage, source side predriver voltage, and coil waveform detect comparator voltage. Common for loading, capstan, and drum motors. |
| 6 7 | CSLP1 CSLP2 | | | Connection for the triangular wave generator. The coil output waveform is made to operate in a soft switching manner by this triangular wave. |
| 26 | GND | | | Ground for all circuits except output. |
| 3 2 1 | WIN UIN VIN | | | Coil waveform detect comparator input. |
| 64 | COM | | | Motor coil midpoint input. Using this voltage as a reference, the coil voltage waveform is detected. |
| 59 62 61 | WOUT_D UOUT_D VOUT_D | | | U, V, and W phase coil output. |
| 60 | RF_D | | | Drum motor driver output. transistor ground. Constant current drive is performed by detecting the voltage at this pin. |
| 10 | FC2 | | | Output midpoint control. Connection for oscillation prevention capacitor. |

Continued on next page.

LB11993W

Continued from preceding page.

| Pin No. | Symbol | Voltage | Equivalent Circuit Diagram | Description |
|----------------------|------------------------------|-----------------------|----------------------------|--|
| 57 | VS_L | 2.2 to V_{CC2} | | Loading motor power supply. Stabilize against noise in the same way as for V_{CC2} . |
| 56 | RF_L | | | Output transistor P ground. Output current can be detected for motor current control by inserting a resistor between Rf pin and ground. |
| 58 55 | OUT1 OUT2 | | | Loading motor driver output. Connect to loading motor. |
| 23 24 28 27 | RLM1 RLP1 RLM2 RLP2 | 0.2V to V_{CC1} -1V | | L-FG amplifier input. RLM1 and RLM2 are negative input. RLP1 and RLP2 are positive input. |
| 22 29 | RLO1 RLO2 | | | R-FG amplifier output. |
| 21 20 | DEC1 DEC2 | 0 to V_{CC1} | | Loading motor input. When $V_{CC1} = 3.0V$ 2.0V or higher: High 0.6V or lower: Low |

Continued on next page.

LB11993W

Continued from preceding page.

| Pin No. | Symbol | Voltage | Equivalent Circuit Diagram | Description |
|----------------------|--|-----------------------------|----------------------------|---|
| 63 | RS_L | 0 to V_{CC1} -1.5V | | Current limiter setting. Set voltage between RF pin and ground, for limiting current. |
| 31 32 34 33 | AMP1IN- AMP1IN+ AMP2IN- AMP2IN+ | 0.2V to (V_{CC1} -1)V | | OP amplifier input. AMP1IN+ and AMP2IN+ are non-inverting input. AMP1IN- and AMP2IN- are inverting input. |
| 30 35 | AMP1OUT AMP2OUT | | | OP amplifier output. |

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of April, 2007. Specifications and information herein are subject to change without notice.