

**3V 10-Bit, 20MSPS A/D Converter with Internal Voltage Reference**

The HI3300 is a monolithic, 10-bit analog-to-digital converter fabricated in an advanced CMOS process. It is designed for high speed applications where integration, bandwidth and accuracy are essential. The HI3300 features a 2-step parallel architecture to allow the system designer to realize an increased level of system integration resulting in decreased cost and power dissipation.

The HI3300 has excellent dynamic performance while consuming less than 40mW power at 20MSPS. The A/D only requires a single +3.0V power supply.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.	SAMPLING RATE (MSPS)
HI3300IN	-40 to 85	48 Ld LQFP	Q48.7x7-S	20

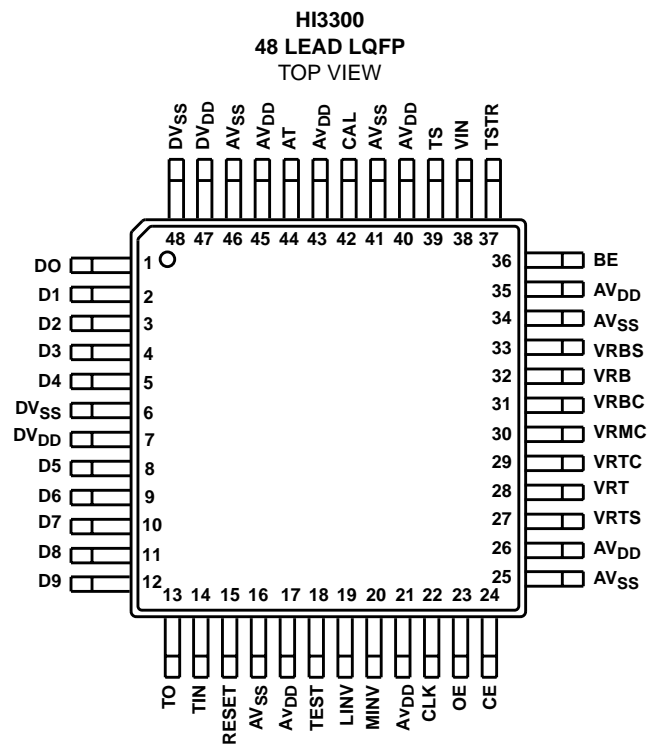
**Features**

- Sampling Rate . . . . .20MSPS
- Low Power at 20MSPS . . . . .40mW
- Power Down Mode . . . . . 3mW
- Wide Full Power Input Bandwidth . . . . . 100MHz
- On-Chip Sample and Hold Amplifiers
- Single Supply Voltage Operation . . . . .+2.7V - 3.3V

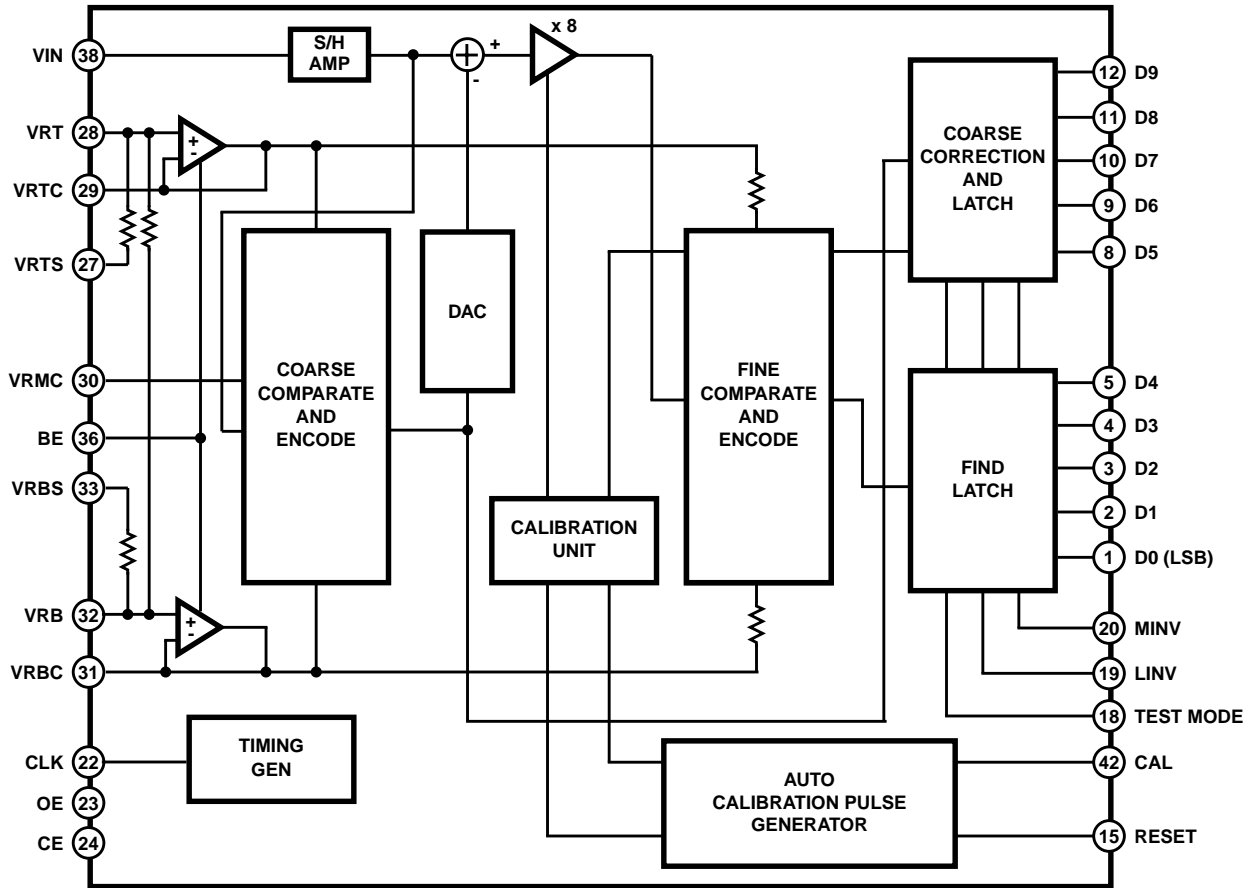
**Applications**

- Wireless Local Loop
- PSK and QAM I&Q Demodulators
- Medical Imaging
- Wireless Communications Systems
- Battery Powered Instruments

**Pinout**



Block Diagram



**Absolute Maximum Ratings**

Supply Voltage ( $V_{DD}$ ) .....  $V_{SS}$  -0.5V to 4.5V  
 ( $DV_{DD}$ ) .....  $DV_{SS}$  -0.5V to 4.5V  
 Reference Voltage ( $V_{RT}$ ,  $V_{RB}$ ) .....  $V_{DD}$  +0.5V to  $V_{SS}$  -0.5V  
 Input Voltage (Analog) ( $V_{IN}$ ) .....  $V_{DD}$  +0.5V to -0.5V  
 Input Voltage (Digital) ( $V_{IH}$ ,  $V_{IL}$ ) .....  $V_{DD}$  +0.5V to  $V_{SS}$  -0.5V  
 Output Voltage (Digital) ( $V_{OH}$ ,  $V_{OL}$ ) .....  $DV_{DD}$  +0.5V to  $DV_{SS}$  -0.5V

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  
 48 Ld LQFP ..... 122  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 (Lead Tips Only)

**Operating Conditions**

Temperature Range ..... -40°C to 85°C  
 Supply Voltage Range ( $V_{DD}$ ,  $V_{SS}$ ) ..... 3.0V to  $\pm$ 0.3V  
 ( $DV_{DD}$ ,  $DV_{SS}$ ) ..... 3.0V to  $\pm$ 0.3V  
 |  $DV_{SS}$  -  $AV_{SS}$  | ..... 0mV to 100mV  
 Reference Input Voltage ( $V_{RB}$ ) ..... 0.3  $V_{DD}$  to 0.5  $V_{DD}$   
 ( $V_{RT}$ ) ..... 0.6  $V_{DD}$  to 0.8  $V_{DD}$   
 Analog Input ( $V_{IN}$ ) ..... 0.9 Vp-p or More  
 Clock Pulse Width ( $t_{PW1}$ ), ( $t_{PW0}$ ) ..... 25ns (Min)  
 Operating Ambient Temperature ( $T_{OPR}$ ) ..... -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $f_C = 20\text{MSPS}$ ,  $V_{DD} = 3\text{V}$ ,  $DV_{DD} = 3\text{V}$ ,  $V_{RB} = 1\text{V}$ ,  $V_{RT} = 2\text{V}$ ,  $T_A = 25^\circ\text{C}$

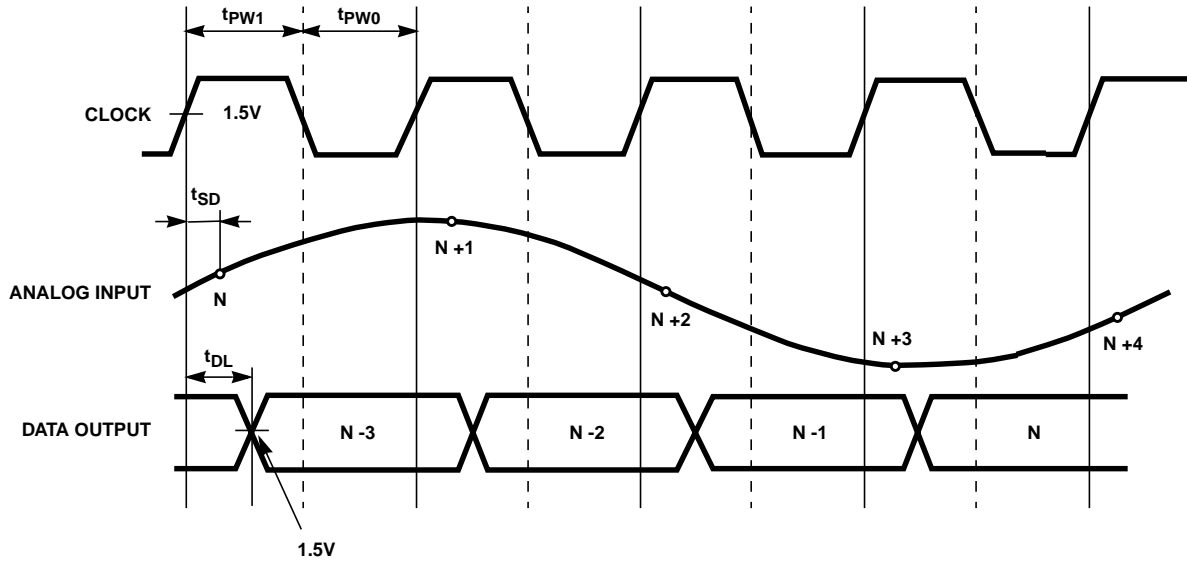
PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Maximum Conversion Rate		$f_C$ max	$f_{IN} = 1.0\text{kHz}$ Triangular Wave Input	20	-	-	MSPS
Minimum Conversion Rate		$f_C$ min		-	-	0.5	
Supply Voltage	Analog	$I_{ADD}$	$f_{IN} = 1.0\text{kHz}$ Triangular Wave Input BE = High	-	12	-	mA
	Digital	$I_{DD}$		-	1.0	-	
Standby Current	Analog	$I_{AST}$	CE = $V_{DD}$	-	1.0	-	mA
	Digital	$I_{DST}$		-	1.0	-	
Reference Pin Current 1		$I_{RT1}$	VRTS, VRBS: Open Between $V_{RT}$ and $V_{RB}$	-	100	-	$\mu\text{A}$
		$I_{RB1}$		-	-100	-	
Reference Pin Current 2		$I_{RT2}$	BE = $V_{DD}$ Between $V_{RTC}$ and $V_{RBC}$	-	2	-	mA
		$I_{RB2}$		-	-2	-	
Analog Input Band		BW	-1dB	-	TBD	-	MHz
Analog Input Capacitance		$C_{IN}$		-	10	-	pF
Reference Resistance Value 1		$R_{REF1}$	Between $V_{RTS}$ and $V_{RT}$ , $V_{RT}$ and $V_{RB}$ , $V_{RB}$ and $V_{RBS}$	-	10k	-	$\Omega$
Reference Resistance Value 2		$R_{REF2}$	Between $V_{RTC}$ and $V_{RBC}$	-	500	-	$\Omega$
Offset Voltage		EOT	EOT = Theoretical Value - Measured Value	-	TBD	-	mV
		EOB	EOB = Measured Value - Theoretical Value	-	TBD	-	
Digital Input Voltage		$V_{IH}$	$V_{DD} = 2.7$ to $3.3\text{V}$	0.7	-	-	V
		$V_{IL}$		-	-	0.2	
Analog Input Current		$A_{IH}$	$V_{IN} = 2\text{V}$	-	20	-	$\mu\text{A}$
		$A_{IL}$	$V_{IN} = 1\text{V}$	-	-20	-	
Digital Input Current		$I_{IH}$	$V_{DD} = 3.3\text{V}$	$V_{IH} - V_{DD}$	-	-	$\mu\text{A}$
				$V_{IL} = V_{SS}$	-	-	

# HI3300

## Electrical Specifications $f_C = 20\text{MSPS}$ , $AV_{DD} = 3\text{V}$ , $DV_{DD} = 3\text{V}$ , $V_{RB} = 1\text{V}$ , $V_{RT} = 2\text{V}$ , $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Digital Output Current	$I_{OH}$	$OE = AV_{SS}$ $DV_{DD} = 2.7\text{V}$	$V_{OH} = DV_{DD} - 0.4\text{V}$	1.0	-	-	mA
	$I_{OL}$		$V_{OL} = 0.4\text{V}$	1.0	-	-	
Digital Output Current	$I_{OZH}$	$OE = AV_{DD}$ $DV_{DD} = 3.3\text{V}$	$V_{OH} = DV_{DD}$	-	-	1.0	$\mu\text{A}$
	$I_{OZL}$		$V_{OL} = 0\text{V}$	-	-	1.0	
Three-State Output Disable time	$t_{PEZ}$	Clock not Synchronized for Active $\rightarrow$ High Impedance		-	2	-	ns
Three-State Output Enable Time	$t_{PEZ}$	Clock not Synchronized For High Impedance $\rightarrow$ Active		-	2	-	ns
Integral Nonlinearity Error	$E_L$			-	$\pm 1.0$	-	LSB
Differential Nonlinearity Error	$E_D$			-	$\pm 0.5$	-	LSB
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp, $f_C = 14.3\text{MSPS}$		-	TBD	-	%
Differential Phase Error	DP			-	TBD	-	Deg
Output Data Delay	$t_{DL}$	$C_L = 20\text{pF}$		-	3	-	ns
Sampling Delay	$t_{SD}$			-	2	-	ns
SNR	SNR	$f_{IN} = 100\text{kHz}$		-	TBD	-	dB
		$f_{IN} = 500\text{kHz}$		-	TBD	-	dB
		$f_{IN} = 1\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 3\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 7\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 10\text{MHz}$		-	TBD	-	dB
SFDR	SFDR	$f_{IN} = 100\text{kHz}$		-	TBD	-	dB
		$f_{IN} = 500\text{kHz}$		-	TBD	-	dB
		$f_{IN} = 1\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 3\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 7\text{MHz}$		-	TBD	-	dB
		$f_{IN} = 10\text{MHz}$		-	TBD	-	dB

Timing Diagrams



NOTE: ○: Indicates point at which analog data is sampled.

FIGURE 1. TIMING CHART 1

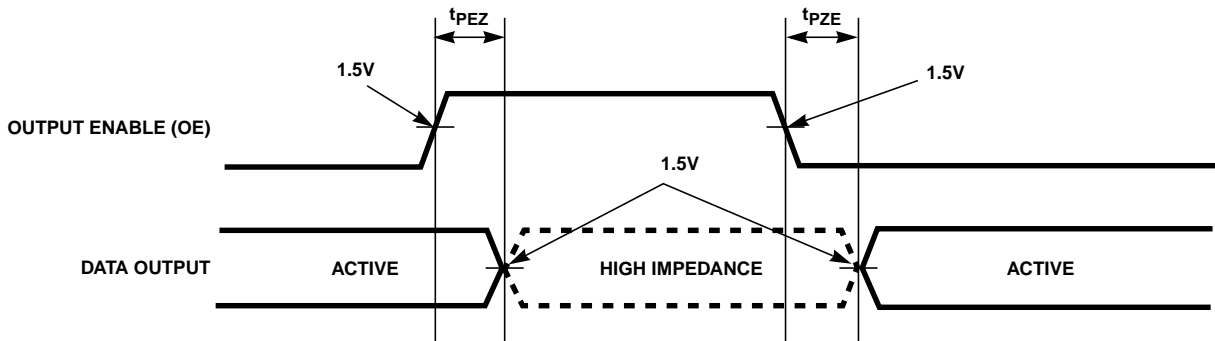
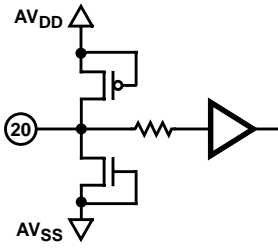
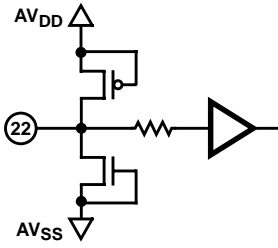
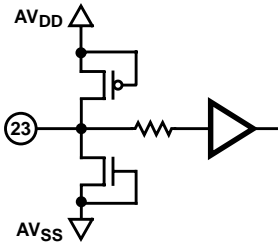
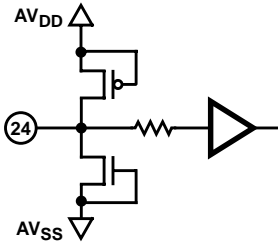


FIGURE 2. TIMING CHART 2

**Pin Description**

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 5 8 to 12	D0 to D9		D0 (LSB) to D9 (MSB) output.
6, 48	DVSS		Digital Ground.
7, 47	DVDD		Digital Power.
13	TO		Test signal output. High impedance when TS = high.
14	TIN		Test signal input. Normally fixed to AVDD or AVSS.
15	RESET		Calibration circuit reset and startup calibration restart.
16, 25, 34, 4, 46	AVSS		Analog Ground.
17, 21, 26, 35, 40, 43, 45	AVDD		Analog Power.
18	TEST MODE		N/C Do not use.
19	LINV		Output Inversion. High: D0 to D8 are inverted and output. Low: D0 to D8 are normal output.

**Pin Description** (Continued)

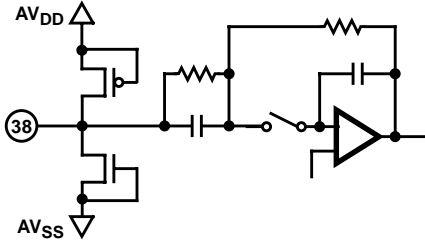
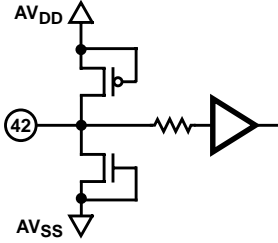
PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
20	MINV		Output Inversion. High: D9 is inverted and output. Low: D9 is Normal output.
22	CLK		Clock Input.
23	OE		D0 to D9 Output Enable. Low: Output Active. High: High Impedance state.
24	CE		Chip Enable. Low: Active state. High: Standby state.

Pin Description (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
27	VRTS		Self bias (Reference top).
28	VRT		Reference top.
29	VRTC		Reference top output.
30	VRMC		Reference middle output.
31	VRBC		Reference bottom output.
32	VRB		Reference bottom.
33	VRBS		Self bias (reference bottom).
36	BE		Bias enable.
37	TSTR		Test signal input. Tie to AV <sub>DD</sub> or AV <sub>SS</sub> .



**Pin Description** (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
44	AT		No Connect
38	$V_{IN}$		Analog input.
42	CAL		Calibration pulse input.
39	TS		Test signal input. Normally fixed to $AV_{DD}$ .

**Digital Output**

The following table shows the correlation between the analog input voltage and the digital output code (TESTMODE = 1, LINV, MINV = 0).

TABLE 1.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE	
		MSB	LSB
VRT	1023	1	1
•	•	1	1
•	•	1	1
•	•	1	1
•	•	1	1
•	•	1	1
•	512	1	0
•	•	0	0
•	511	0	1
•	•	0	1
•	•	0	1
•	•	0	1
•	•	0	1
•	•	0	1
•	•	0	0
VRB	0	0	0

The following table shows the output state for the combination of TESTMODE, LINV, and MINV states.

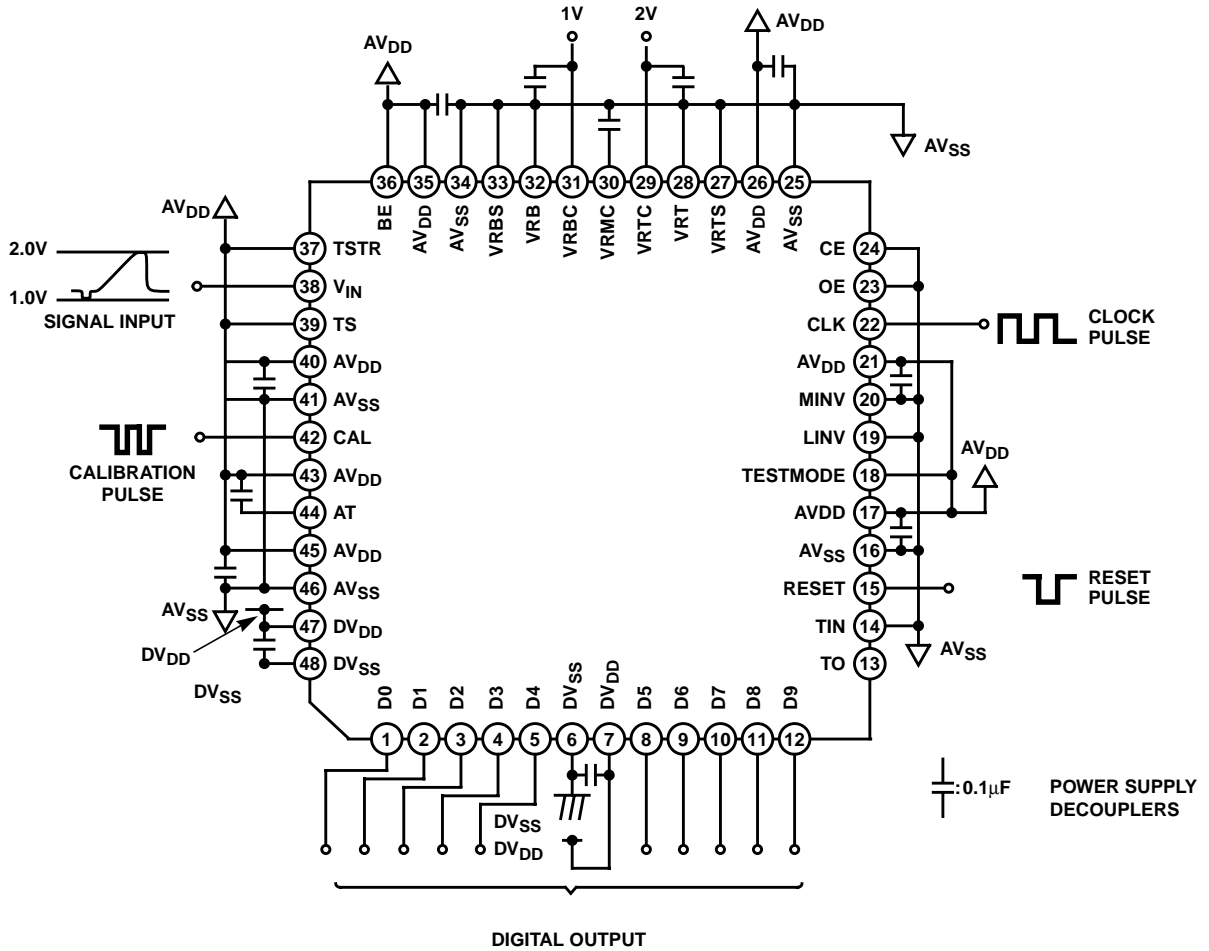
TABLE 2.

TEST MODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	P	P	P	P	P	P	P	P	P	P
1	1	0	N	N	N	N	N	N	N	N	N	P
1	0	1	P	P	P	P	P	P	P	P	P	N
1	1	1	N	N	N	N	N	N	N	N	N	N
0	0	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	0
0	0	1	1	0	1	0	1	0	1	0	1	1
0	1	1	0	1	0	1	0	1	0	1	0	1

NOTE: P: Forward-phase output; N: Inverted output.

**Application Circuit 1**

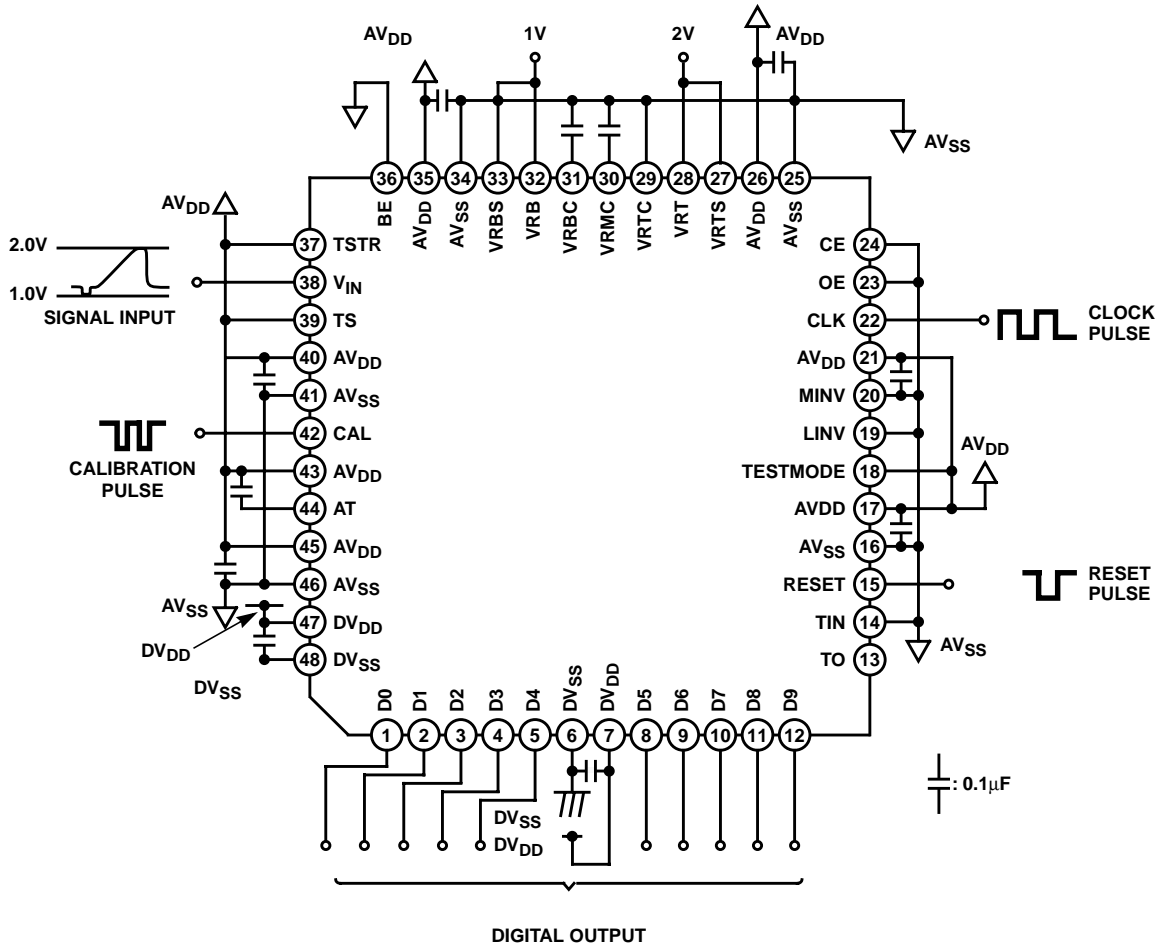
When not using self-bias and the internal bias circuits and supplying the reference voltage from an external source.



NOTE: Application circuits shown are typical examples illustrating the operation of the devices. Intersil cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

### Application Circuit 2

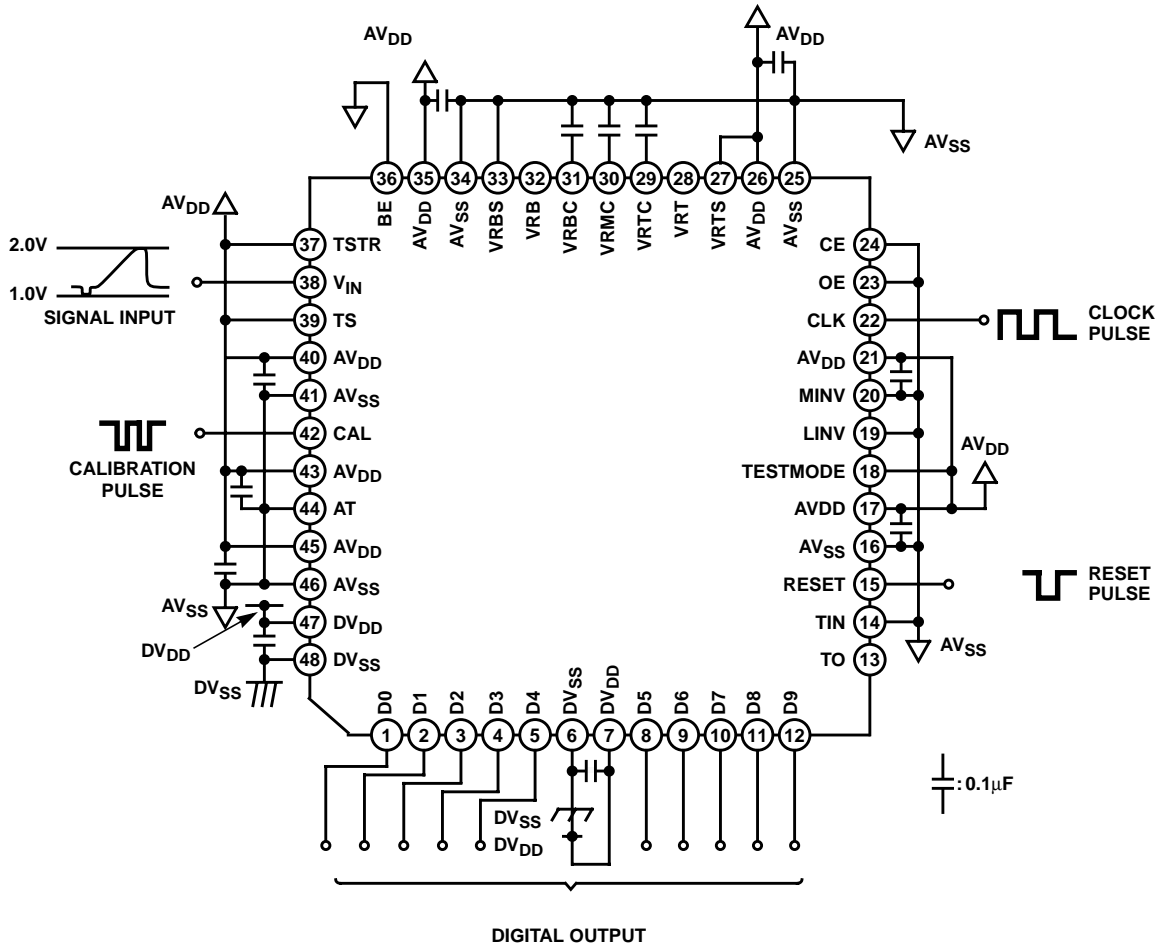
When not using self-bias circuit, using only the internal bias circuit, and supplying the reference voltage from an external source.



NOTE: Application circuits shown are typical examples illustrating the operation of the devices. Intersil cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Application Circuit 3**

When not using self bias circuit, using only the internal bias circuit, and supplying the reference voltage from an external source.



NOTE: Application circuits shown are typical examples illustrating the operation of the devices. Intersil cannot assume responsibility for any problems arising out of these use of the circuits or for any infringement of third party patent and other right due to same.

## Calibration Function

### Activating Startup Calibration

To achieve superior linearity, the HI3300 has a built-in calibration circuit. Startup calibration must be activated when the power supply and reference voltage have risen and stabilized. Care should be taken as only the upper five bits may be output in the worst case if startup calibration is not activated.

Startup calibration can be activated either at the rise of the RESET pin (Pin 15) or at the fall of the CE pin (Pin 24). The startup calibration activation method for each case is shown in Figure 3.

As shown in the Figure 3, startup calibration must be activated after the supply voltage has risen and stabilized (full scale of 90% or more). After activation, startup calibration is performed for an interval of about 33,000 clocks. Therefore, care should be taken as the output data during this interval (about 2.3ms at 14.3MHz) cannot be used.

### Calibration Pulse Supply

The IC's operating status with changes due to fluctuations in the supply voltage and ambient temperature during use can be constantly monitored and then compensated appropriately by inputting a pulse at regular intervals to the CAL pin (Pin 41). Figure 4 shows the timing chart.

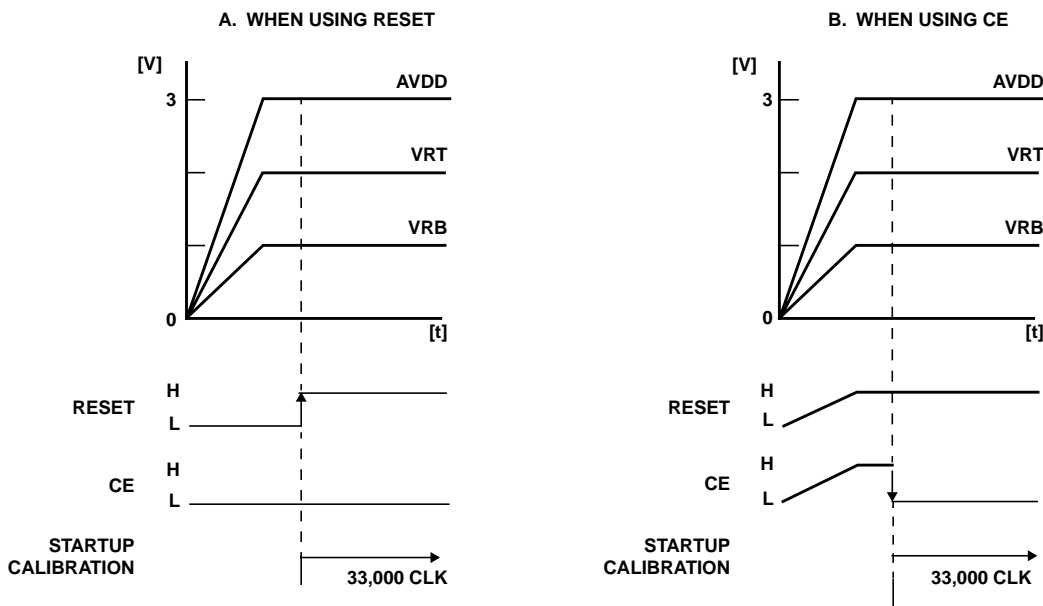


FIGURE 3. STARTUP CALIBRATION ACTIVATION METHODS

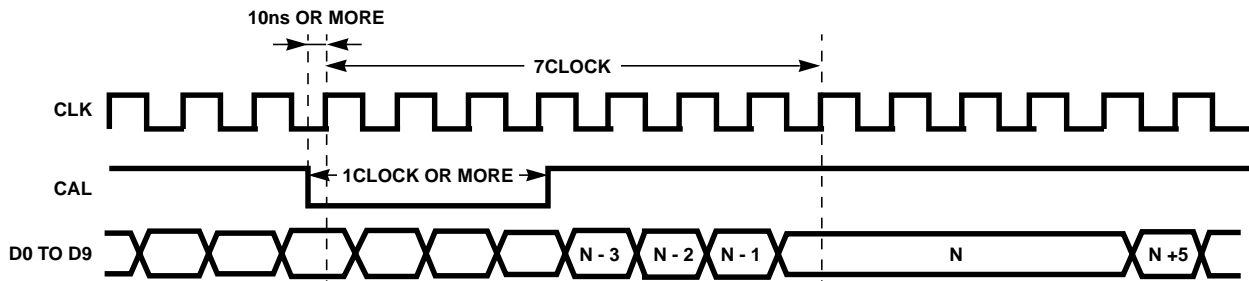


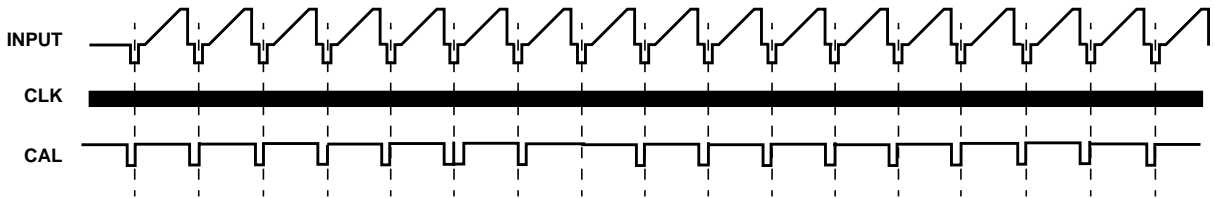
FIGURE 4. CALIBRATION TIMING CHART

Calibration starts when the fall of the pulse input to the CAL pin (Pin 41) is detected at the clock rise. At this time, the comparator is used in an exclusive manner for a four clock interval. So, the output data holds the immediately previous data for a four clock interval after seven clocks from the rise

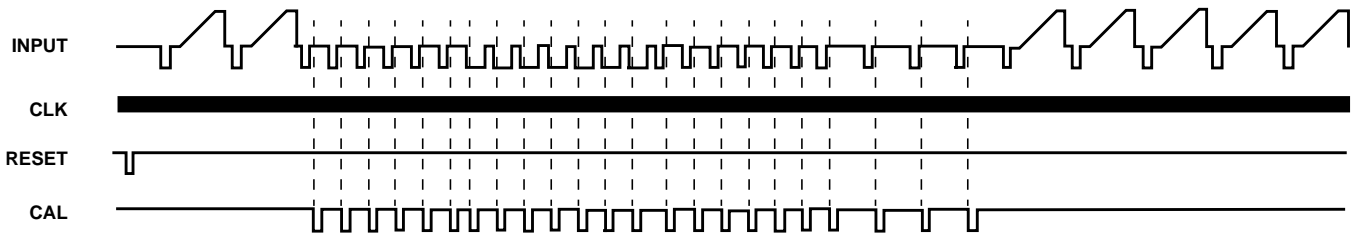
of the clock where the fall of the calibration pulse was detected, and then the data during this interval is missing.

Therefore, the effects of this function can be avoided by inputting a sync or other signal as the calibration pulse so that calibration is performed outside of the interval of the actually used video signal. An input example is shown below.

**Input over H Sync**



**Input over V Sync**



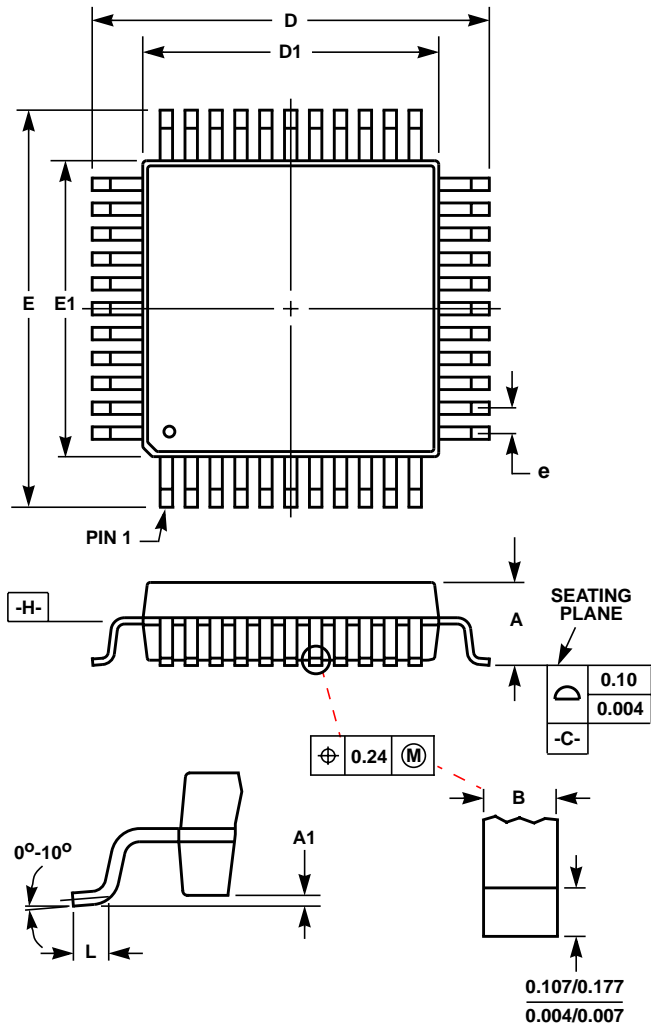
**Latch-up**

Ensure that the AVDD and DVDD pins share the same power supply on a board to prevent latch-up which may be caused by power-ON time lag.

**Board**

To obtain full-expected performance from this IC, be sure that the mounting board has a large ground pattern for lower impedance. It is recommended that the IC be mounted on a board without using a socket to evaluate its characteristics adequately.

**Metric Plastic Quad Flatpack Packages (MQFP/PQFP)**



**Q48.7x7-S**

**48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

Rev. 1 4/95

**NOTES:**

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)

**Sales Office Headquarters**

**NORTH AMERICA**  
 Intersil Corporation  
 P. O. Box 883, Mail Stop 53-204  
 Melbourne, FL 32902  
 TEL: (321) 724-7000  
 FAX: (321) 724-7240

**EUROPE**  
 Intersil SA  
 Mercure Center  
 100, Rue de la Fusee  
 1130 Brussels, Belgium  
 TEL: (32) 2.724.2111  
 FAX: (32) 2.724.22.05

**ASIA**  
 Intersil (Taiwan) Ltd.  
 7F-6, No. 101 Fu Hsing North Road  
 Taipei, Taiwan  
 Republic of China  
 TEL: (886) 2 2716 9310  
 FAX: (886) 2 2715 3029