

# Self Recovering Watchdog

## Description

The H6060 is a monolithic low-power CMOS device combining a programmable timer and a series of voltage comparators on the same chip. The device is specially suited for watchdog functions such as microprocessor and supply voltage monitoring. If the  $\mu P$  system malfunctions, the watchdog will recover it by issuing repeated active reset signals. The voltage monitoring part provides double security by combining both the unregulated voltage ( $V_{IN}$ ) and the regulated voltage ( $V_{DD}$ ) monitoring simultaneously. The H6060 initializes the power-on reset after  $V_{IN}$  reaches  $V_{SH}$  (see table 4) and  $V_{DD}$  rises above 3.V. If  $V_{IN}$  drops below  $V_{SL}$  (see table 4), the H6060 gives an advanced warning signal for register saving and if the voltage drops further below  $V_{RL}$  (see table 4), RES and  $\overline{RES}$  go active. The H6060 functions at any supply voltage down to 1.6 V and is therefore particularly suited for start-up and shut-down control of microprocessor systems.

## Features

- Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100 ms), externally programmable if required
- Unregulated DC monitoring ( $V_{IN}$ ) with 3 standard or programmable trigger voltages for: power-on reset initialization, advanced power-fail warning ( $\overline{SAVE}$ ), reset at power-down ( $\overline{RES}$ )
- Regulated DC monitoring ( $V_{DD}$ ): power-on reset initialization enabled only if  $V_{DD} \geq 3.5 V$
- Internal voltage reference
- Works down to 1.6 V supply voltage
- Push-pull or Open drain outputs
- Low current consumption
- SO8 package

## Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems

## Typical Operating Configuration

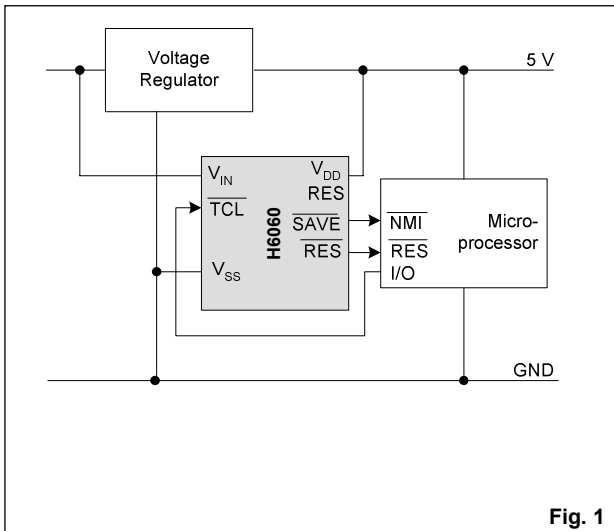


Fig. 1

## Pin Assignment

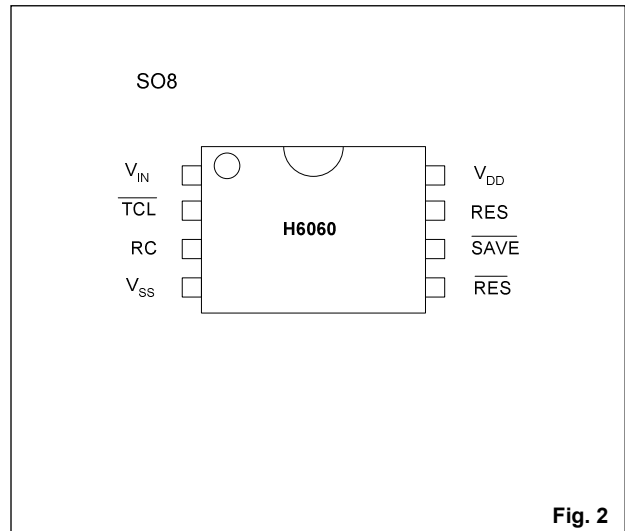
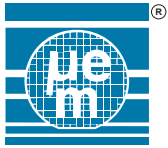


Fig. 2



## Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage $V_{DD}$ to $V_{SS}$	$V_{DD}$	- 0.3 to + 8 V
Voltage at any pin to $V_{SS}$	$V_{MIN}$	- 0.3
Voltage at any pin to $V_{DD}$ (except $V_{IN}$ )	$V_{INMAX}$	+ 0.3
Voltage at $V_{IN}$ to $V_{SS}$	$V_{MIN}$	+ 15 V
Current at any output	$I_{MAX}$	$\pm 10$ mA
Storage temperature	$T_{STO}$	-65°C to +150°C

**Table 1**

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

## Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when

all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

## Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating temperature Industrial	$T_{AI}$	-40	+85	°C
Supply voltage	$V_{DD}$	1.6	5.5	V
Comparator input voltage				
Version 13, 14, 15, 16	$V_{IN}$	0	$V_{DD}$	V
Version 11,12	$V_{IN}$	0	12	V
RC-oscillator programming (see Fig. 15)				
External capacitance*	C1		1	$\mu$ F
External resistance	R1	10		k $\Omega$

**Table 2**

\* Leakage < 1 $\mu$ A

## Electrical Characteristics

$V_{DD} = 5.0$  V,  $T_A = -40$  to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
$V_{DD}$ activation threshold	$V_{ON}$	$T_A = 25$ °C	3		3.5	V
$V_{DD}$ deactivation threshold	$V_{OFF}$	$T_A = 25$ °C		$V_{ON} - 0.3$		V
Supply current Input $V_{IN}$ , $\overline{TCL}$	$I_{DD}$	RC open, $\overline{TCL}$ at $V_{DD}$ or $V_{SS}$		80	140	$\mu$ A
Leakage current	$I_{IP}$	$V_{SS} \leq V_{IP} \leq V_{DD}$ ; $T_A = 85$ °C		0.005	1	$\mu$ A
Input current on pin $V_{IN}$	$I_{IN}$	Version 12; $V_{IN} = 10$ V		100	180	$\mu$ A
$\overline{TCL}$ input low level	$V_{IL}$				0.8	V
$\overline{TCL}$ input high level	$V_{IH}$		2.4			V
SAVE, RES, RES outputs Leakage currents	$I_{OLK}$	Version 15; $V_{OUT} = V_{DD}$		0.05	1	$\mu$ A
Drive currents (all versions)	$I_{OL}$	$V_{OL} = 0.4$ V	3.2	8		mA
	$I_{OL}$	$V_{DD} = 3.5$ V; $V_{OL} = 0.4$ V	2			mA
	$I_{OL}$	$V_{DD} = 1.6$ V; $V_{OL} = 0.4$ V	80			$\mu$ A
Drive currents (versions 14,16) <sup>1)</sup>	$I_{OH}$	$V_{OH} = 4.0$ V	3.2	8		mA
	$I_{OH}$	$V_{DD} = 3.5$ V; $V_{OH} = 2.8$ V	2			mA
	$I_{OH}$	$V_{DD} = 1.6$ V; $V_{OH} = 1.2$ V	80			$\mu$ A

1) Versions: 15 = open drain outputs; 14, 16 = push-pull outputs

**Table 3**

## $V_{IN}$ Surveillance

Voltage thresholds at  $T_A = 25$  °C

Version <sup>1)</sup>	Comparator Reference	Input Resistance on $V_{IN}$ ( $R_{VIN}$ )	Threshold			Thresholds Tolerance	Ratio Tolerance <sup>3)</sup>
			$V_{SH}$	$V_{SL}$	$V_{RL}$		
14	$V_{DD}$	$\sim 100$ M $\Omega$	2.25	2.00	1.75 <sup>2)</sup>	$\pm 5\%$	$\pm 2\%$
15, 16	Band-gap reference	$\sim 100$ M $\Omega$	2.00	1.95	1.90	$\pm 10\%$	$\pm 2\%$

1) Version: 15 = open drain outputs; 14, 16 = push-pull outputs

2) at  $V_{DD} = 5$  V

3) Threshold ratio tolerance is defined as the tolerance of  $V_{SH} / V_{SL}$  and  $V_{SL} / V_{RL}$ .

**Table 4**

## Timing Characteristics

$V_{DD} = 5.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{\text{TCL}}$ to output pins	$T_{DIDO}$	Excluding debounce time $T_{DB}$		250	500	ns
$V_{IN}$ to output pins	$T_{AIDO}$		4	10	$\mu\text{s}$	
Logic transition times on all output pins	$T_{TR}$	Load 10 k $\Omega$ , 100 pF		30	100	ns
Timeout period	$T_{TO}$	RC open, unshielded, $T_A = 25\text{ }^\circ\text{C}$	60	100	160	ms
	$T_{TO}$	RC open, unshielded (not tested)	45		200	ms
$T_{TCL}$ input pulse width	$T_{TCL}$		150			ns
Power-on reset debounce	$T_{DB}$			$T_{TO}/64$		ms
$V_{IN}$ low pulse	$T_{VINL}$	Where debounce time $T_{DB}$ is guaranteed	10			$\mu\text{s}$

Table 5

## Timing Waveforms

### Voltage Reaction: $V_{DD}$ Monitoring

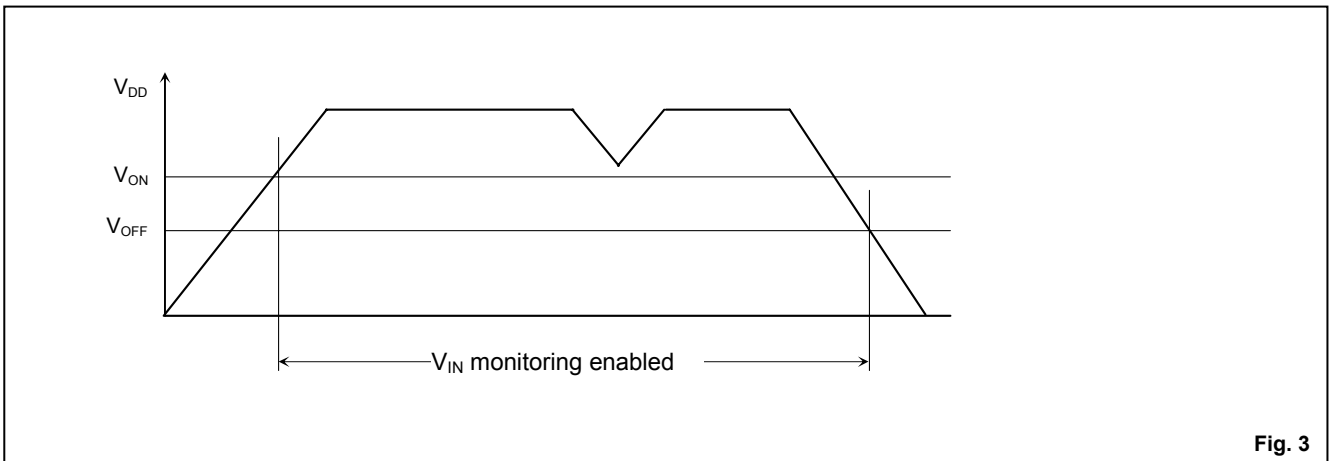
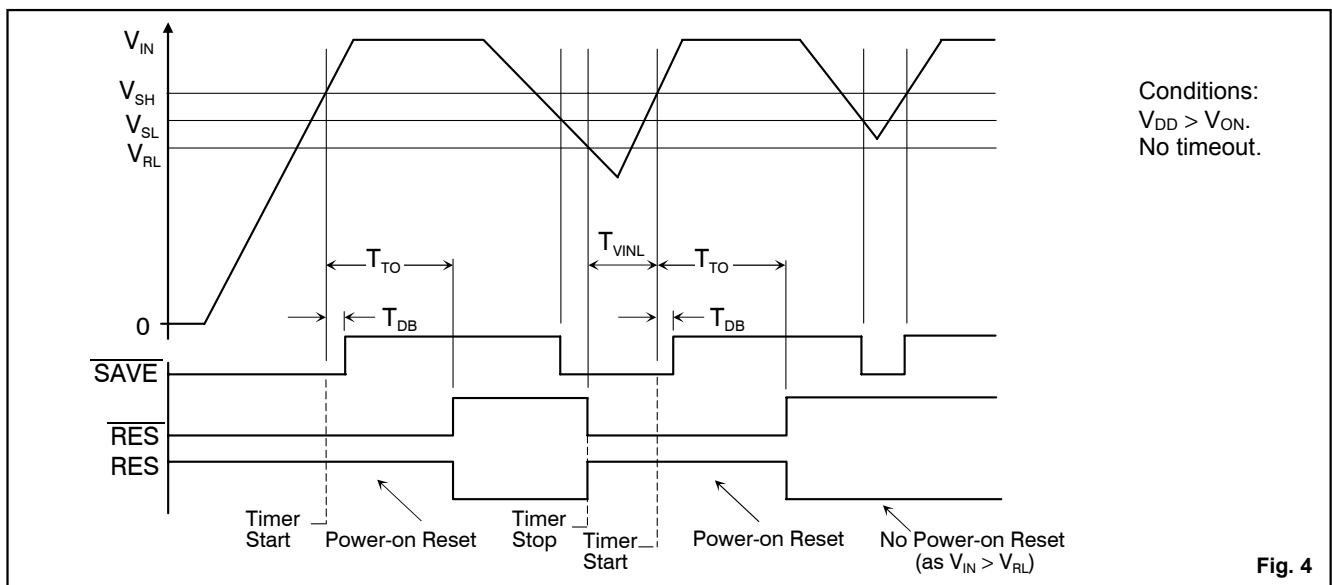


Fig. 3

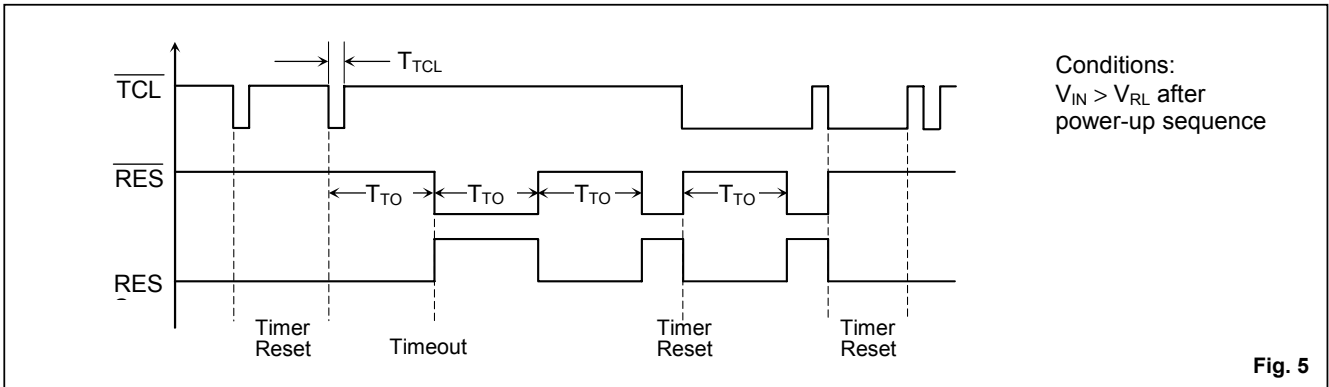
### Voltage Reaction: $V_{IN}$ Monitoring



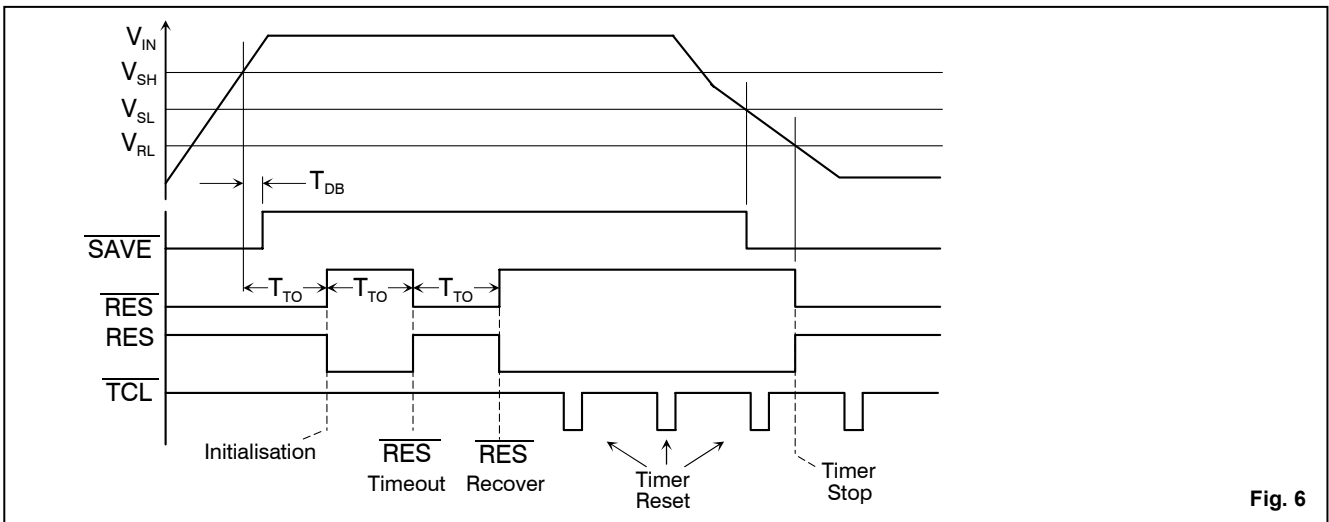
Conditions:  
 $V_{DD} > V_{ON}$ .  
 No timeout.

Fig. 4

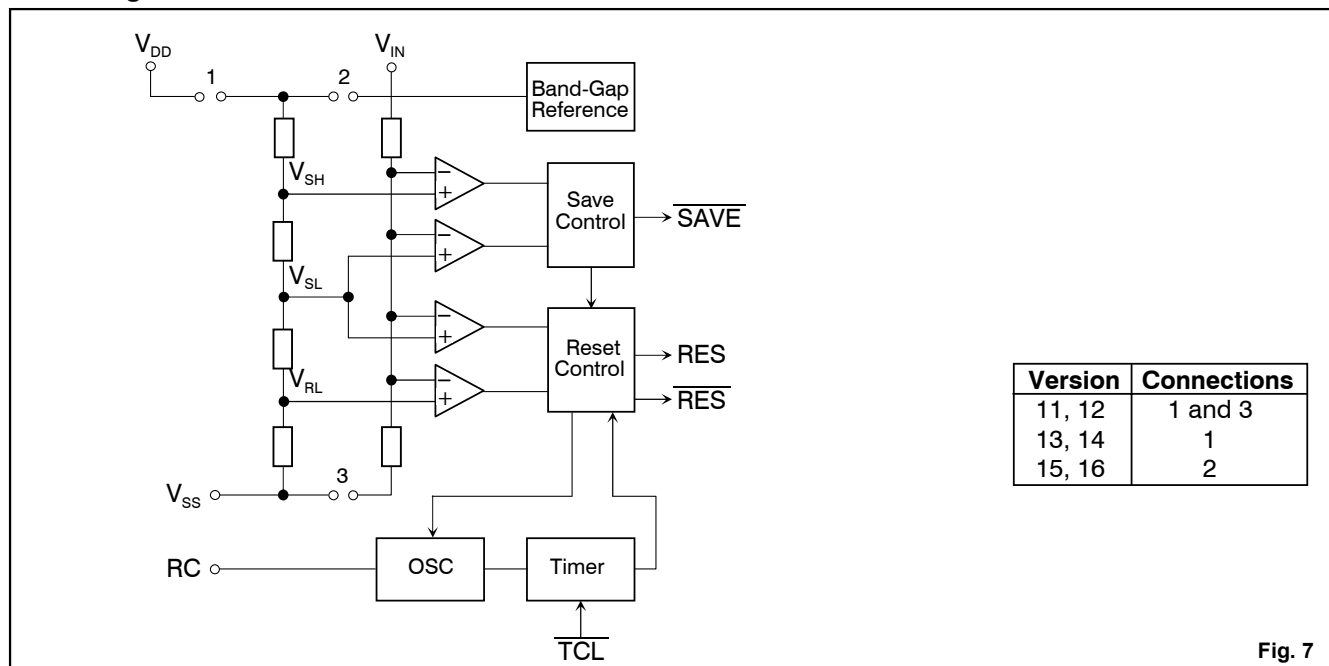
## Timer Reaction



## Combined Voltage and Timer Reaction



## Block Diagram



## Pin Description

Pin	Name	Function
1	$V_{IN}$	Voltage sense input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	$V_{SS}$	GND terminal
5	$\overline{RES}$	Active low reset output
6	$\overline{SAVE}$	Save output
7	RES	Active high reset output
8	$V_{DD}$	Positive supply voltage terminal

Table 6

## Functional Description

### Supply Lines

The circuit is powered through the  $V_{DD}$  and  $V_{SS}$  pins. It monitors both its own  $V_{DD}$  supply and a voltage applied to the  $V_{IN}$  input.

### $V_{DD}$ Monitoring

During power-up the  $V_{IN}$  monitoring is disabled and  $\overline{RES}$ , RES and  $\overline{SAVE}$  stay active low as long as  $V_{DD}$  is below  $V_{ON}$  (3.5 V). As soon as  $V_{DD}$  reaches the  $V_{ON}$  level, the state of the outputs depend on the watchdog timer and the voltage at  $V_{IN}$  relative to the thresholds (see Fig. 4). If the supply voltage  $V_{DD}$  falls back below  $V_{OFF}$  ( $V_{ON} - 0.3$  V) the watchdog timer and the  $V_{IN}$  monitoring are disabled and the outputs  $\overline{RES}$ , RES and  $\overline{SAVE}$  become active. The  $V_{DD}$  line should be free of voltage spikes.

### $V_{IN}$ Monitoring

The analog voltage comparators compare the voltage applied to  $V_{IN}$  (typically connected to the input of the voltage regulator) with the stabilized supply voltage  $V_{DD}$  (version 14) or with the bandgap voltage (versions 15, 16) (see Fig. 7). At power-up, when  $V_{DD}$  reached  $V_{ON}$  and  $V_{IN}$  reaches the  $V_{SH}$  level, the  $\overline{SAVE}$  output goes inactive, and the timer starts running, setting  $\overline{RES}$  and RES in active after the time  $T_{TO}$  (see. Fig. 4). If  $V_{IN}$  falls below  $V_{SL}$ , the  $\overline{SAVE}$  output goes active and stays active until  $V_{IN}$  rises again above  $V_{SH}$ . If  $V_{IN}$  falls below the voltage  $V_{RL}$ ,  $\overline{RES}$  and RES will become active and the on-chip timer will stop. When  $V_{IN}$  rises again above  $V_{SH}$ , the timer will initiate a power-up sequence. The  $\overline{RES}$  and RES outputs may however be influenced independently of the voltage  $V_{IN}$  by the timer action, see section "Combined Voltage and Timer Action". Monitoring the rough DC side of the regulator, as shown in Fig. 11, is the only way to have advanced warning of power-down. Spikes on  $V_{IN}$  should be filtered if they are likely to exceed the value ( $V_{SL} - V_{RL}$ ).

The combination of  $V_{IN}$  and  $V_{DD}$  monitoring provide high system security: if  $V_{IN}$  rises much faster than  $V_{DD}$ , then the device starts the power-on sequence only when  $V_{DD}$  reached  $V_{ON}$  (Fig. 10). Short circuits on the regulated supply voltage can be detected.

### Voltage Thresholds on $V_{IN}$

The H6060 is available with 3 different sets of thresholds:

**Version 14:** monitor the unregulated voltage and are ideal for programming of the  $V_{IN}$  voltage thresholds. Fixed resistor values can be used for programming.

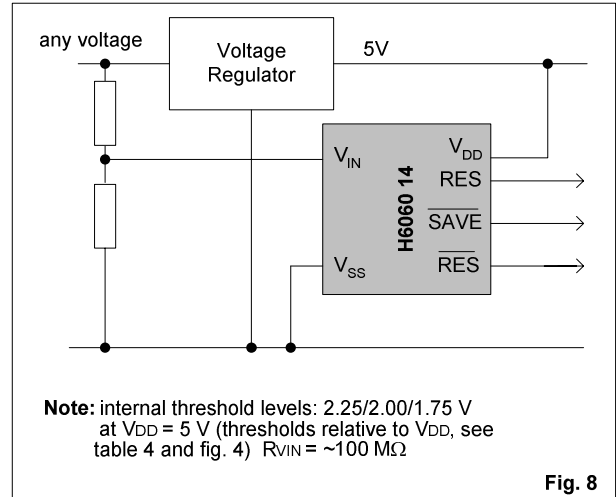


Fig. 8

**Version 15, 16:** monitor the regulated voltage. They are suited to applications where the unregulated voltage is not available. (The tolerance is  $\pm 10\%$ , see table 4. For tighter tolerances, trimming can be used, see Fig. 9).

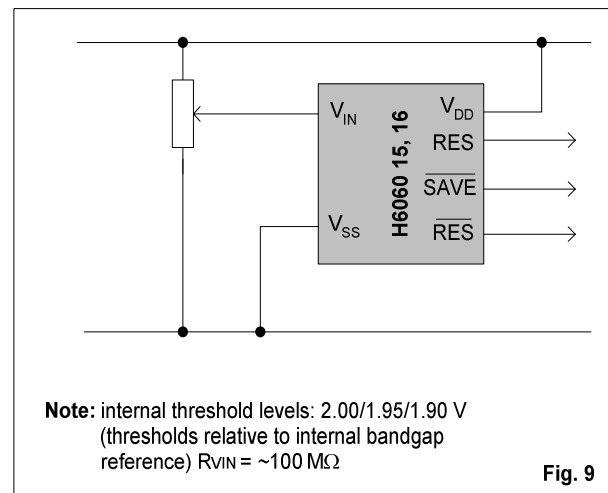


Fig. 9

Monitoring of the unregulated voltage requires version 14. These versions are based on the principle that  $V_{DD}$  rises with  $V_{IN}$  on power-up and  $V_{DD}$  holds up for a certain time after  $V_{IN}$  starts dropping on power-down. The versions 11 and 12 have a 100 k $\Omega$  nominal resistance from  $V_{IN}$  to  $V_{SS}$  (internal voltage divider). The versions 14, 15 and 16 have high impedance  $V_{IN}$  inputs (see Fig. 7 and Table 4) for external threshold voltage programming by a voltage divider on pin  $V_{IN}$ . The levels obtained are proportional to the internal levels  $V_{SH}$ ,  $V_{SL}$  and  $V_{RL}$  on the chip itself (see Electrical Specifications).

## Timer Programming

With pin RC unconnected, the on-chip RC oscillator together with its divider chain give a timeout  $T_{TO}$  of typically 100 ms. To program different  $T_{TO}$ , an approximation for calculating component values is given by the formula:

$$T_{TO} = \left[ 0.75 + \frac{(32 + C_1) \cdot 2}{5.5 + \frac{V_{DD} - 1}{R_1}} \right] 8.192$$

$R_1 \text{ min.} = 10 \text{ k}\Omega$ ,  $C_1 \text{ max.} = 1 \mu\text{F}$

If  $R_1$  is in  $\text{M}\Omega$  and  $C_1$  in pF,  $T_{TO}$  will be in ms.

A resistor decreases and a capacitor increases the interval to timeout. Excellent temperature stability of  $T_{TO}$  can be achieved by using external components. A precise square wave of period  $2 \times T_{TO}$  is generated at the outputs  $\overline{\text{RES}}$  and RES when  $\overline{\text{TCL}}$  is tied to either  $V_{DD}$  or  $V_{SS}$ . The oscillator and watchdog timer start running when both  $V_{IN}$  is greater than  $V_{SH}$  (see Fig. 6) and  $V_{DD}$  is greater than  $V_{ON}$  (see Fig. 3).

They will remain running while both  $V_{IN}$  is greater than  $V_{RL}$  and  $V_{DD}$  is greater than  $V_{OFF}$  (see Fig. 3).

## Timer Clearing and $\overline{\text{RES}}$ /RES Action

A negative edge or a negative pulse at the  $\overline{\text{TCL}}$  input for longer than 150 ns will reset the timer and set  $\overline{\text{RES}}$  and RES inactive. If a further  $\overline{\text{TCL}}$  signal edge or pulse is applied before  $T_{TO}$  timeout,  $\overline{\text{RES}}$  and RES will remain inactive and the timer will again be reset to zero (see Fig. 5). If no  $\overline{\text{TCL}}$  signal is applied before the  $T_{TO}$  timeout,  $\overline{\text{RES}}$  and RES will start to generate square waves of period  $2 \times T_{TO}$  starting with the inactive state. The watchdog will remain in this state until the next  $\overline{\text{TCL}}$  signal appears, or until a fresh power-up sequence.

## Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. One timeout period after  $V_{IN}$  reaches  $V_{SH}$ , during power-up,  $\overline{\text{RES}}$  and RES go inactive. A  $\overline{\text{TCL}}$  pulse will have no effect until this power-on reset delay is completed. After completing the power-up sequence the watchdog timer starts acting. If no  $\overline{\text{TCL}}$  pulse occurs,  $\overline{\text{RES}}$  and RES go active after one timeout period  $T_{TO}$ . After each subsequent timeout period, without a timer clear pulse at  $\overline{\text{TCL}}$ ,  $\overline{\text{RES}}$  and RES change polarity providing square wave signals. A  $\overline{\text{TCL}}$  pulse clears the watchdog timer and causes  $\overline{\text{RES}}$  and RES to go inactive. A voltage drop below the  $V_{RL}$  level overrides the timer and immediately forces  $\overline{\text{RES}}$ , RES and  $\overline{\text{SAVE}}$  active. Any further  $\overline{\text{TCL}}$  pulse has no effect until the next power-up sequence is completed.

## Typical Applications

### Microprocessor Watchdog with Power-On Reset and Voltage Monitor

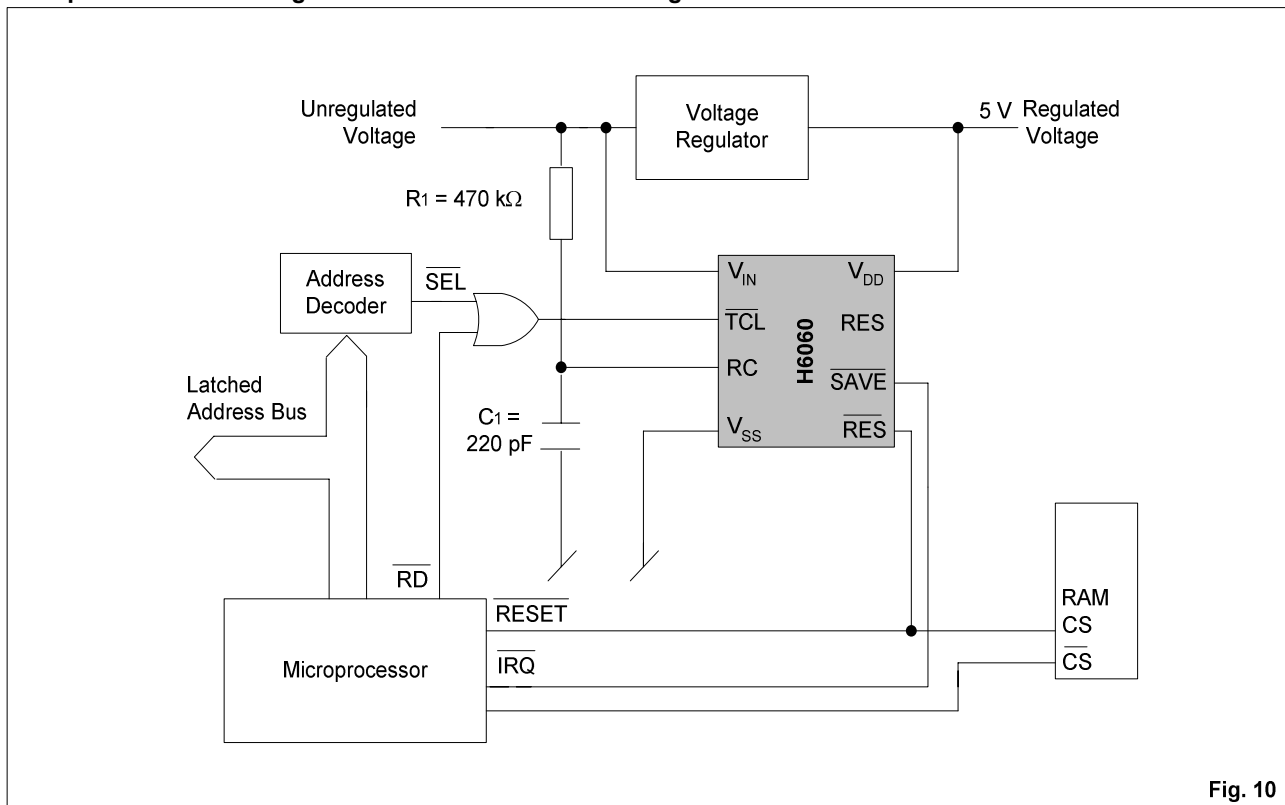
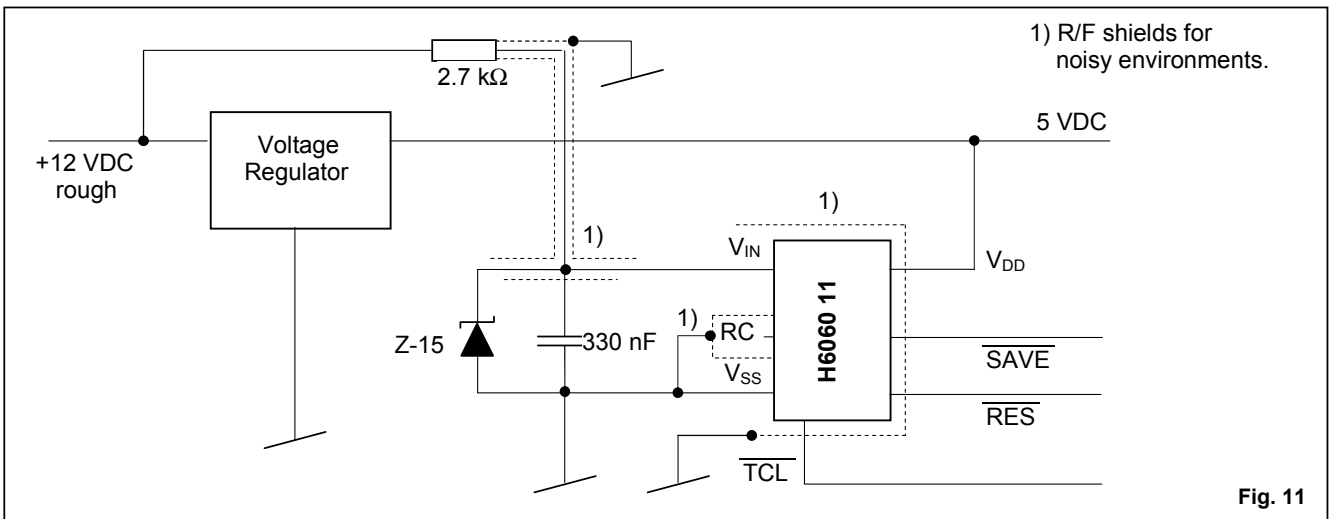
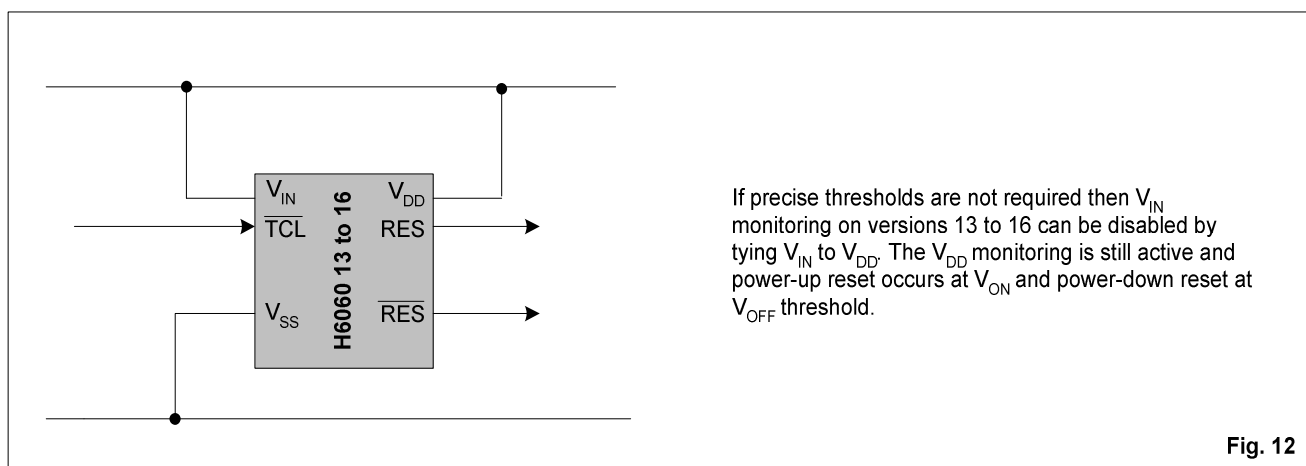


Fig. 10

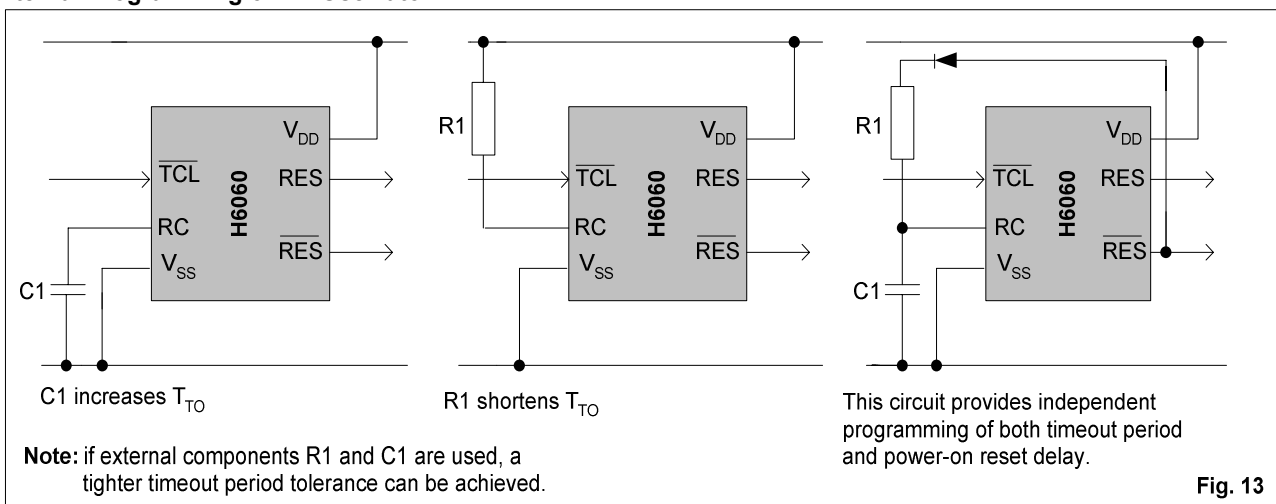
## Voltage Monitor with Spike Suppression



## Watchdog and Power-On Reset

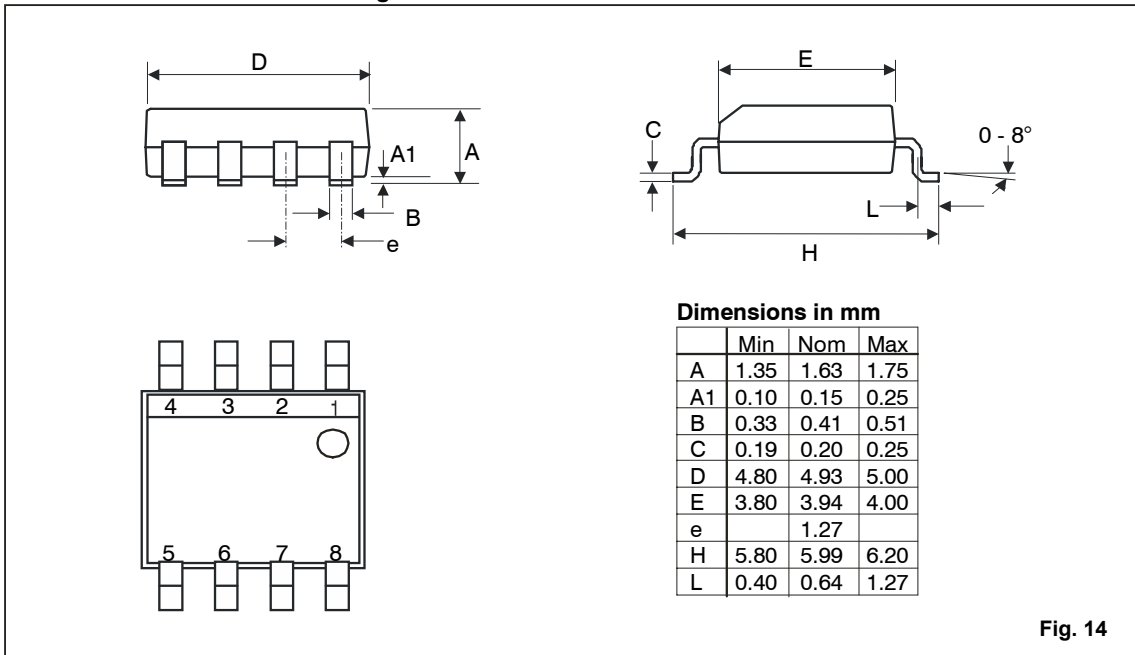


## External Programming of RC Oscillator



## Package Information

### Dimensions of 8-Pin SOIC Package



## Ordering Information

When ordering please specify complete part number.

Part Number	Version	Threshold (see Table 4)	Output	Package	Delivery Form	Package Marking (first line)	Temperature
H6060V15SO8A	V15	1.95	Open drain	8-pin SOIC	Stick	606015	-40°C to °85°C
H6060V15SO8B				8-pin SOIC	Tape&Reel	606015	
H6060V14SO8A	V14	2.00	Push-pull	8-pin SOIC	Stick	606014	
H6060V14SO8B				8-pin SOIC	Tape&Reel	606014	
H6060V16SO8A	V16	1.95		8-pin SOIC	Stick	606016	
H6060V16SO8B				8-pin SOIC	Tape&Reel	606016	

**Note:** Other versions are no longer available

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