Low Power Microcontroller with RC and 32kHz oscillators and 9 high drive outputs

Features

- **32'768Hz crystal oscillator**
- **500kHz RC Oscillator (no external component)**
- **External clock (metal option)**
- **9 High drive outputs: up to 20mA**
- **Melody generator with 255 programmable frequencies**
- **True Low Power:** 1.5uA active mode
  0.4uA halt mode
  @ 1.55V, 32kHz, 25°C
- **Low Supply Voltage 1.2V to 3.6V**

- Max. 14 Inputs with selectable debouncers; Port P1, P2, P6, P70, P71
- Max. 15 outputs (9 I/O High drive outputs); Port P3, P4, P6, P70, P71, P72
- Mask ROM 4096 x 16bits
- RAM 256 x 4bits
- 2 clocks per instruction cycle
- 72 basic instructions
- 2 outputs; Reset OUT, Buzzer OUT
- 2 timers 8bits
- 2 x 4 bits BCD counters
- Event counter 3bits
- Prescaler down to 1Hz (crystal =32kHz), readable by CPU in 2 ranges
- Serial Port as selectable configuration of Port 5
- 18 Interrupts: 12 internal, 6 external
- Voltage Level Detector, 3 levels software selectable
- Die form and MLF2, 40 pin (Micro Lead Frame) package

Description

The EM6635 is a low voltage, low power microcontroller containing 9 integrated high-drive outputs able to provide up to 20mA. It is ideal for use in applications in which one must drive devices such as motor drivers, small stepping motors, LEDs, triacs, external EEPROM or other ICs in the system.
EM6635 has both a 32kHz crystal oscillator and a 500kHz RC oscillator without external component, as well as an external clock to be driven up to 4MHz.
The CPU operating clock can be switched from crystal to RC oscillator for high-speed operation.
It has a frequency/melody generator with 255 programmable frequencies for quality buzzer.

The EM6635 contains the equivalent of 8kB mask ROM and the RAM has a capacity of 256x4 bits.

It also has a power-on reset, watchdog timer, 2 timers 8bits, 2 BCD counters, 3bits event counter, 4 wire serial port 8bits and several clock functions.

Figure 1. Architecture

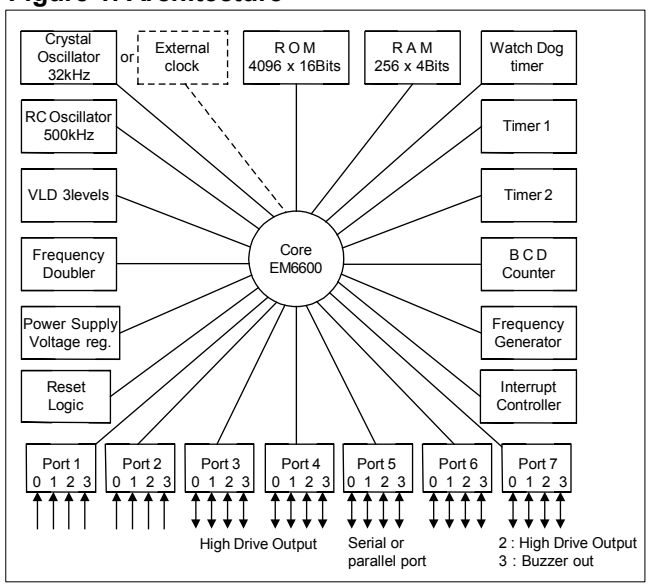
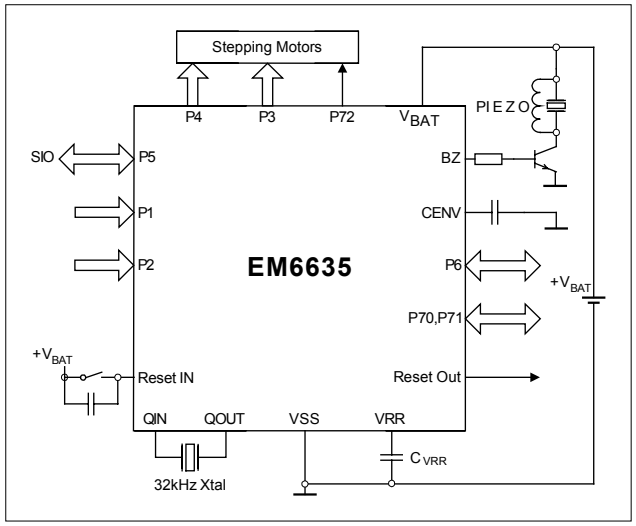


Figure 2. Typical application



Applications

- Watch & clock
- Timer / sports timing devices
- Security / industrial
- Toys
- Sensor interface

EM6635 at a glance

❑ **Power Supply**
- Low voltage low power architecture
- including internal voltage regulator
- 1.2 to 3.6 V battery voltage
- 1.5µA in active mode (Xtal, 25°C)
- 0.4 µA in HALT mode (Xtal, 25°C)
- 32'768Hz Crystal Oscillator
- 500kHz RC oscillator (no external component)
- External clock (metal option)

❑ **RAM**
- 4 pages of 64 x 4bits, page 0 is direct addressable

❑ **ROM**
- 4096 x 16bits, metal mask programmable

❑ **CPU**
- 4-bits RISC architecture
- 2 clock cycles per instruction (CPI=2)
- 72 basic instructions
- operating frequency selectable by SW

❑ **Main Operating Modes and Resets**
- Active mode, CPU is running
- Halt mode, CPU in halt, peripheral are running
- Initial reset on power on (POR)
- Watchdog reset (logic)
- Reset terminal with Schmitt Trigger
- Reset with input combination on Port P1 & Port P2 (register selectable)

❑ **Prescaler**
- 15 stage system clock divider from 32kHz down to 1Hz
- 4 Interrupt requests; 128Hz, 64Hz, 32Hz and 1Hz or 64Hz, 16Hz, 8Hz and 1Hz
- Prescaler state readable to CPU from 128Hz to 16Hz and from 8Hz to 1Hz
- Prescaler reset (32Hz to 1Hz)

❑ **8bit Serial Interface at Port 5**
- 4 wire (serial clock In/Out, serial output, serial status In/Out (RDY), serial input)
- Master mode: 32kHz, 16kHz or 4kHz serial clock
- Slave mode: external clock from P33
- Selectable word length: 8 - 7 - 6 - 5 bit
- Selectable synchronized or direct output
- Selectable positive or negative active clock edge by direct or inverted serial clock SCK
- Special ready output mode when port is in master mode
- RDY can be set by SW

❑ **Frequency Generator with 255 output frequencies**
- 8bit programmable frequency divider
- 50% duty cycle output signal
- Clock frequency is 65536Hz (doubled 32768Hz)
- SW activated

❑ **Watchdog Timer**
- Creates watchdog reset after time-out
- Can be disabled by SW and mask option

❑ **Interrupt Controller**
- 12 internal, 6 external interrupt request sources
- Individually maskable, individually resettable
- Global interrupts disable,with auto-enable at HALT mode

❑ **Voltage Level Detector (SVLD)**
- 3 software selectable levels
- Busy flag during measure
- Active only on request during measurement to reduce power consumption

❑ **Timer 1**
- 8bits timer with 3 modes: Zero Stop, Synchron Mode and Auto Reload Mode
- Timer clock selectable 4kHz-2kHz-1kHz-512Hz by SW
- Zero Stop: Timer starts counting down when loaded from CPU with data (> 0). When at zero, an interrupt is generated.
- Synchron Mode: After loading by CPU, timer starts synchronized by the positive edge of the prescaler 64Hz signal. An interrupt is generated when timer reaches zero. During timer count down, Port P3 and P4 are outputting their data, otherwise P3 and P4 are at high level (acc. to selected port configuration).
- Auto Reload Mode: (see text at Timer 2)

❑ **Timer 2**
- 8bits timer with 2 modes: Zero Stop and Auto Reload
- Zero Stop as timer1
- Auto Reload mode: Timer starts when a non-zero data is loaded by CPU and counts down to zero. Then the loaded data (internally stored) is automatically reload to the timer counter and the sequence starts again. Each time when zero is reached, an interrupt is generated.
- Timer clock selectable 256Hz-64Hz-16Hz-4Hz by SW

❑ **CHRONO 2x4bits BCD counters**
- Start, stop, reset by SW
- 1/100th second resolution
- CARRY flag can be read by SW when the counter changes from 99 to 0

❑ **Event Counter 3bits**
- Associated to input port P10, P11; readable to CPU
- Counter counts up to 7 and stays there
- Counter reset by CPU-write

❑ **Buzzer Output**
- Piezo driver via external NPN transistor
- Activated together with frequency generator

❑ **Input Ports P1, P2**
- Direct or debounced input read selectable by SW for each port
- Clocked pulldown or no pulldown by mask option
- P1: Edge detector at P10, P11 (both edges) to generate pulse for event counter
- Interrupt by P12: both edges, by P13: both edges
- Interrupt by positive edge (debounced) of any P2 input
- Reset by debounced input combination: P13, P22, P23 = high, enabled by SW

❑ **Input / Output Ports P3, P4, P5, P6, P7**
- High current drive capability at P3, P4 and P72
- P3, P4: Common direction select P30-P32, P40-P42; P33 and P43 are individually selectable
- P5: individual direction select, debouncer when input
- As input: direct read of terminal data, as output: register data
- P3,P4,P72: selectable 9,8,7,6,5,4 or 3 high drive output in combination with special synchron mode of timer 1
- P5: pull down / pull up according to mask option
- P6: As input: Direct or debounced input read selectable by SW
- Interrupt by positive edge (debounced) of any P6 input
- Common direction select P60-P61, P62-P63
- P70, P71: As input: Direct or debounced input read selectable by SW for each port
- Interrupt by positive edge (debounced) of P70, P71 input
- Common direction select P70, P71

1. Pin Description

Package MLF2	Function	Symbol	Type	Description
1	**Ports**	P23	I	Input port with selectable debouncer
2		P22	I	Input port with selectable debouncer
3		P21	I	Input port with selectable debouncer
4		P20	I	Input port with selectable debouncer
5	**System**	BZ	O	Buzzer output
6		RESET OUT	O	Reset output
7	**Power Supply**	V_{SS}		negative supply, substrate
8	**Test**	TCK		EM test access, must be without any connection
9		TESTRC		EM test access, must be without any connection
10	**Oscillator**	QOUT		32 kHz quartz connection, input **or** External clock (metal option)
11		QIN		32 kHz quartz connection, output
12				Not connected
13	**Test**	TEST		EM test access, must be without any connection
14	**System**	CENV		Capacitor connection for envelop control tw. V_{SS}
15	**Power Supply**	V_{RR}		Regulated supply voltage, capacitor connection tw. V_{SS}
16	**System**	RESET IN	I	active high reset input
17	**Ports**	P71	I/O	Input/output; low current drive
18		P70	I/O	Input/output; low current drive
19		P63	I/O	Input/output; low current drive
20		P62	I/O	Input/output; low current drive
21		P61	I/O	Input/output; low current drive
22		P60	I/O	Input/output; low current drive
23		P53	I/O	Input/output: configurable as serial clock I/O: SCK
24		P52	I/O	Input/output: configurable as serial output: SOUT
25		P51	I/O	Input/output: configurable as serial status I/O: RDY
26		P50	I/O	Input/output: configurable as serial input: SIN
27	**Power Supply**	VBAT (V_{DD})		Positive supply, capacitor tw. V_{SS} (C depends on VBAT noise)
28	**Ports**	P13	I	Input port with selectable debouncer and edge detector
29		P12	I	Input port with selectable debouncer and edge detector
30		P11	I	Input port with selectable debouncer and edge detector
31		P10	I	Input port with selectable debouncer and edge detector
32		P72	I/O	Input/output; high current drive
33		P43	I/O	Input/output; high current drive
34		P42	I/O	Input/output; high current drive
35		P41	I/O	Input/output; high current drive
36		P40	I/O	Input/output; high current drive
37		P33	I/O	Input/output; high current drive, P33 configurable as Fout
38		P32	I/O	Input/output; high current drive
39		P31	I/O	Input/output; high current drive
40		P30	I/O	Input/output; high current drive
		NC/P63		Not connected

2. Peripheral Memory Allocation

Address HEX	Peripheral Function
0 - 3F	Data RAM page 0, 1, 2, 3
40 - 46	HW Control, Configuration
47 – 4C	Input/output Ports
4D - 4F	Free
50 - 55	Input/output Ports
56 – 5E	Timer1, Timer2, BCD counter
5F	Free
60 – 6B	Event Counter, Freq. Generator Interrupt Controller
6C	Supply voltage level detector
6D	RC-Oscillator
6E 6F	CPU Index Reg. Low CPU Index Reg. Hi
70 - 74	Serial Interface
75, 76	EM Test
77	RAM Page Register
78	Reserved
79 – 7D	Free
7E 7F	EM Test EM Test

Special Access Modes for HW-Control 1 and -2:

There are two HW-Control registers (HW-Ctl-1, HW-Ctl-2) with different access modes. Each of these two registers can be accessed by two different addresses. The access by address H40 for HW-Ctl-1 (H42 for HW-Ctl-2) is the normal access method as every other register in the EM6635: The corresponding data bus value is written into the register bit.
Using address H41 (HW-Ctl-1) or address H43 (HW-Ctl-2) allows a bitwise access to the register. The CPU has not to care about the states of the register bits which must not be modified.
With a high level at bits 0 to 2, the corresponding bits in the register are selected, while a low level unselects the register bits. The level of bit 3 defines the action on the selected bits: a high level will set and a low level will clear the selected register bits. Read access is done in the normal way.
If bits 0, 1, 2 are not selected (at Low level), the register at bit 3 is set if bit 3 is high or reset if it is low.
This concerns SelTBCapHi at HW-Ctl-2, address H43.

2.1 RAM Address Modes

The EM6635 has 4 pages of 64x4bits RAM's built-in. The page number is coded on 2 bits, there are 4 pages.
The page number is stored on RAM index register at address H77.
The RAM is directly addressable on addresses decimal (0 to 63), and it is paged adressable.
To write or read the RAM page1, 2, 3 the user has first to set the offset value in the **RAM Index** register.

RAM index		Page
PageSel[1]	PageSel[0]	
0	0	0
0	1	1
1	0	2
1	1	3

Ram Architecture

Add Page	64x4 direct addressable RAM		Add Page	64x4 indirect addressable RAM		Add Page	64x4 indirect addressable RAM		Add Page	64x4 indirect addressable RAM	
0	RAM_0	4 bit R/W	1	RAM_0	4 bit R/W	2	RAM_0	4 bit R/W	3	RAM_0	4 bit R/W
	RAM_1	4 bit R/W									
	RAM_2	4 bit R/W									
	RAM_3	4 bit R/W									
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	.	.		.	.		.	.		.	.
	RAM_60	4 bit R/W									
	RAM_61	4 bit R/W									
	RAM_62	4 bit R/W									
	RAM_63	4 bit R/W		RAM_63	4 bit R/W		RAM_63	4 bit R/W		RAM_63	4 bit R/W

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
RAM index	77	119	W	x	x	PageSel[1]	PageSel[0]
			R	0	0	PageSel[1]	PageSel[0]

3. Operating Modes

The EM6635 has two low power operating modes, the active and the halt mode. The oscillator is always active in both modes, whereas the RC-Oscillator is controlled by the CPU.

3.1 Active Mode:

The CPU is running. Instructions are read from the internal ROM and executed by the CPU.
After a system reset, the EM6635 is in active mode at ROM-address H000.
The active mode is stopped by executing the HALT instruction.

3.2 HALT Mode:

After a HALT instruction, the EM6635 is in HALT mode. The CPU is stopped. The 32kHz-oscillator, the prescaler are running, whereas the timers, the watchdog timer, the BCD counters and the frequency generator are only working, if activated before.
The RC-oscillator is stopped.
All registers, RAM and output buffers retain their states prior to **HALT** mode.
The **HALT** mode is left by an interrupt occurence or by a system reset.
The HALT command enables the global interrupt, i.e. DisINT=0.
Note: HALT mode is activated and XTAL Oscillator is not running. Only a system reset allows to go back in **Active** mode.

4. Power Supply

The EM6635 is supplied by a single external power supply between V_{DD} (VBAT) and V_{SS} (Ground).
A built-in voltage regulator generates V_{RR} providing regulated voltage for the oscillator and the internal logic. The output drivers are supplied directly from the external supply V_{DD}. The internal power configuration is shown below in figure 3.
To supply the internal core logic it is possible to use either the internal voltage regulator ($V_{RR} < V_{DD}$) or VBAT directly ($V_{RR} = V_{DD}$). The selection is done by mask option. By default the voltage regulator is used. Refer to chapter 17 for the mask options.
The internal voltage regulator is chosen for high voltage systems. It saves power by reducing the internal core logic's power supply to an optimum value. However, due to the inherent voltage drop over the regulator the minimal V_{DD} is restricted to 1.4V.
A direct VBAT connection can be selected for systems running on a 1.5V battery. The internal RFIL 1kOhm resistor together with the external capacitor on V_{RR} is filtering the V_{DD} supply to the internal logic (as a low pass filter to protect the logic against parasitic over- and under-voltages, e.g. created by piezo shocks).
In this case the minimum V_{DD} can be as low as 1.2V.
The output buffers are directly supplied from the external power supply.

Note: State of I/O pads may not be defined until V_{RR} reaches typ. 0.8V and Power-On-Reset supplied by V_{RR} clears them to inputs.

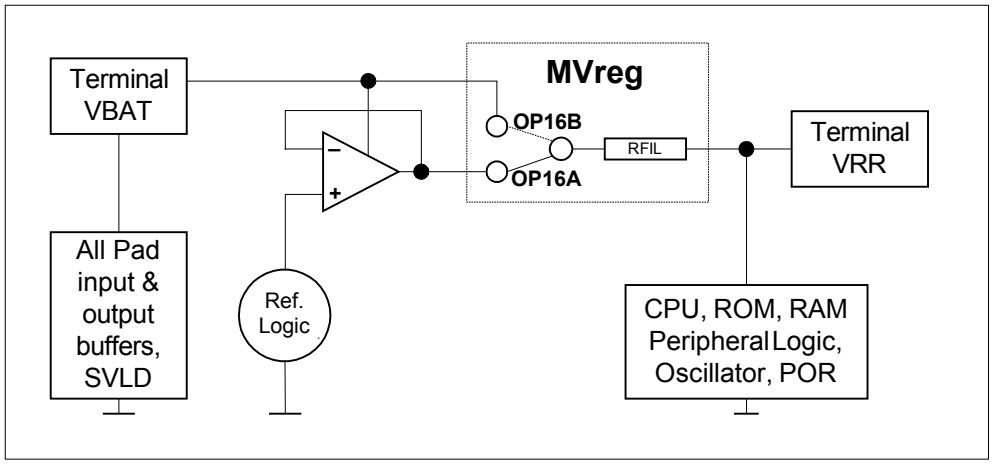


Fig.3: Power Supply Principle

5. Reset

The EM6635 has 4 reset sources:
- the Power On Reset
- external reset input
- reset by input combination
- watchdog timer reset

If one of these reset sources becomes active, a system reset is generated. All registers are set to their corresponding initial values and the program counter of the CPU is set to H000.
If the EM6635 is in HALT mode, it is reset to active mode.
An internal Cold Start delay is triggered from the system reset, which holds the CPU in reset state until its time out. This ensures that the crystal oscillator can settle to stable oscillation.
The Cold Start delay time can be selected by mask option OP-2.
The Cold Start can be disabled by input P22 AND P23 = 1, if this input combination is applied longer than the duration of SYSRES signal (SYSRES terminates after the oscillator start time plus 10 valid clock time periods.) If this condition becomes active after the SYSRES has changed to low, but during an active Cold Start, the Cold Start will be stopped immediately. During the CPURES (corresponds to the Cold Start, after system starts on Xtal oscillator), pull down transistors are active at all port inputs.
Note that all 4 reset sources are triggering the Cold Start delay.

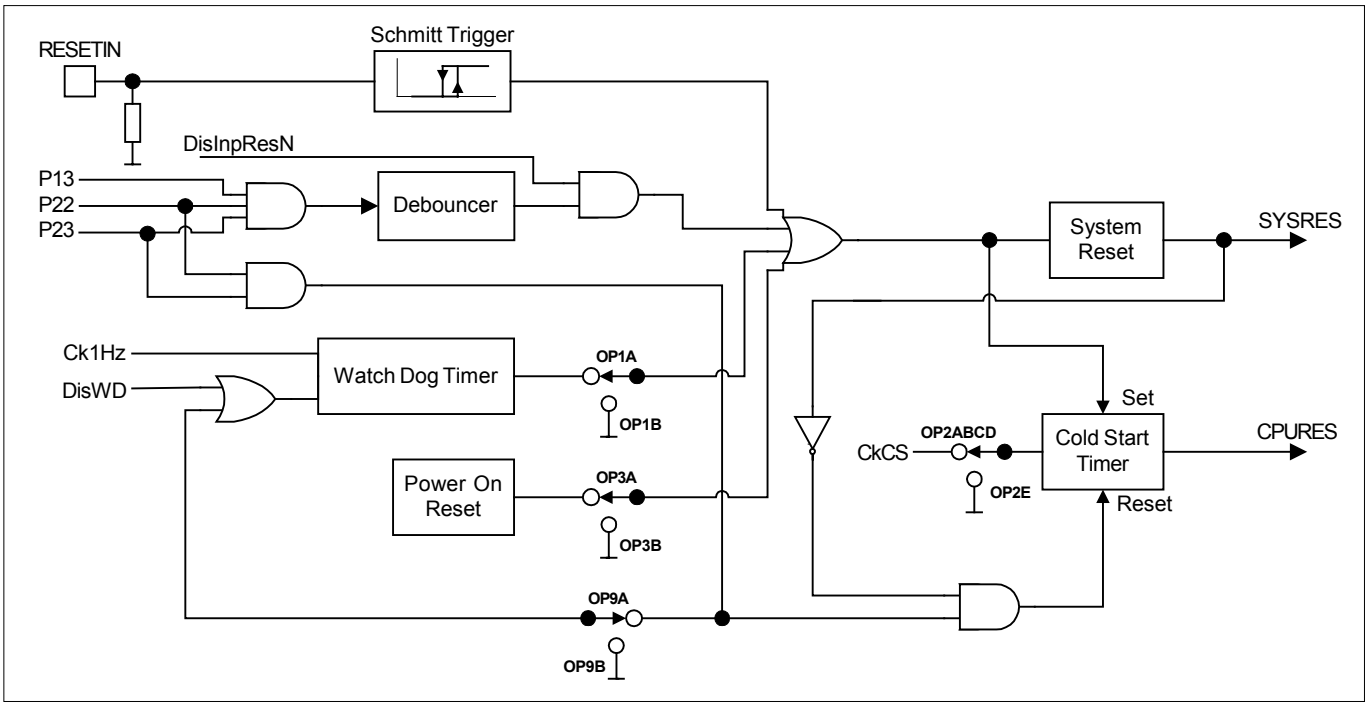


Fig.4: Reset Structure

5.1 Power On Reset

The Power on Reset can be activated by mask option OP-3A.
When the positive power supply VBAT is applied, the internal logic supply voltage VRR rises to the VBAT value with a time constant given by the filter resistor RFIL and the external capacitor CVRR. The POR cell is active until VRR becomes higher than the trigger voltage VPOR of the POR cell. The output signal of the POR cell triggers the system reset.

The EM6635 has two oscillation circuits (refer to chapter 6 for the oscillators).
With the metal option OP-20A, the oscillation circuit starts the operating clocks from RC oscillator.
With the metal option OP-20B, the oscillation circuit starts the operating clocks from XTAL oscillator.

With the metal option OP-20C, the input P50 selects the RC oscillator or XTAL oscillator during SYSRES.
A high level at P50 terminal activates the RC oscillator, a low level activates XTAL oscillator.

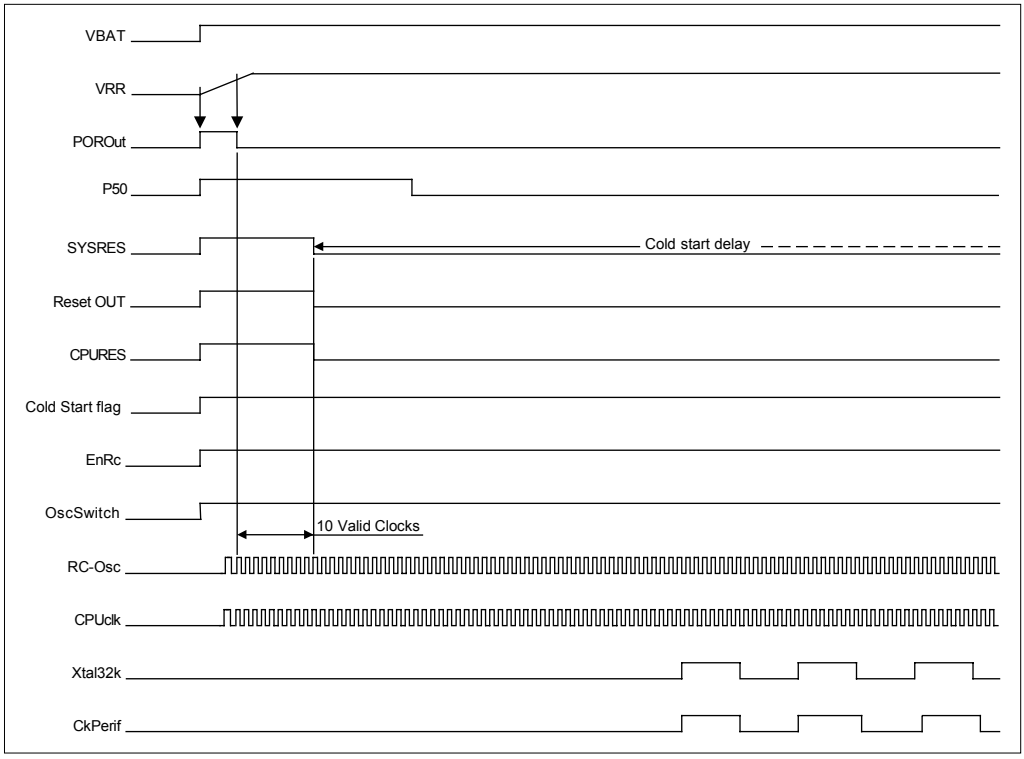


Fig.5: Power On Reset Timing and Clock Generation after System starts on the RC Oscillator

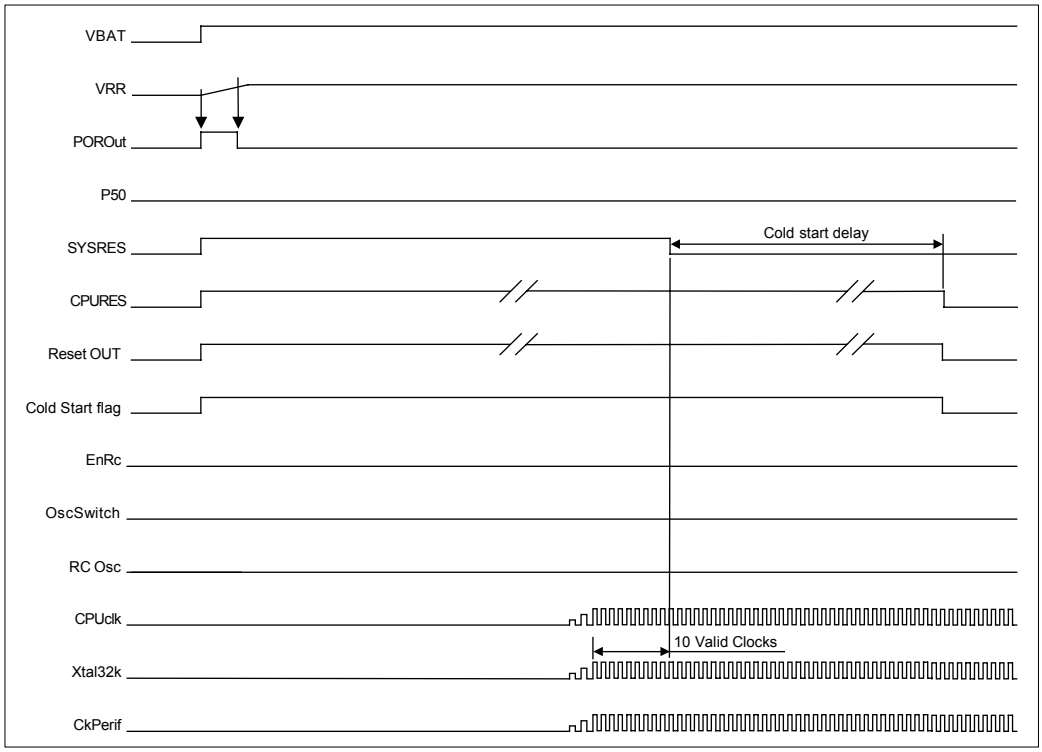


Fig.6: Power On Reset Timing and Clock Generation after System starts on Xtal Oscillator

5.2 External Reset Input

A high level on the reset input "RESET" creates a system reset as long as it is applied. The reset input has an internal pull down resistor RRES, and includes a Schmitt Trigger circuit. The reset input creates the system reset in the same way as the POR signal, both are triggering the Cold Start delay for oscillator stabilisation.

5.3 Input Reset

If input reset is enabled by bit 3 of Config-2 register (at "0" level, address H45, in "DisInpRes"), a high level at input port P13 together with high levels at port P22 and P23 is creating a system reset after a debouncing time of 1.95ms (1 period of 512Hz). This reset is maintained as long as this input condition is applied.

5.4 Watchdog Timer Reset

The watchdog timer is a 2bits timer counting on rising edges of Ck1Hz. It generates a system reset if it is not cleared by the CPU periodically (writing "1" to HW-Ctl-1, bit 0, address H41).
This resets the watchdog timer to zero and timer operation restarts by counting up. Writing "0" has no effect.
The watchdog timer counts also in halt mode, therefore the standby duration must not exceed the watchdog time out tWD = 3-4sec to avoid a system reset.
Note: a prescaler reset is shortening the watchdog time out.
It is recommended to reset the watchdog timer periodically with the 1Hz interrupt.
The watchdog timer function is inhibited, if the input ports P22 and P23 are at high level, if this is enabled by mask option OP-9A.
The watchdog timer can be disabled by Config-1 register, bit 2 at high level (H44), or by mask option OP-1B.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
HW-Ctl-1	41	65	W			(DisINT)	ResetWD
bit access			R	0	0	(DisINT)	0
Config-1	44	68	W	(Mot3Mode)	DisWD	(EnFOut)	(SelIINT8)
			R	(Mot3Mode)	DisWD	(EnFOut)	(SelIINT8)
Config-2	45	69	W	DisInpRes	P5DebOn	P2DebOn	P1DebOn
			R	DisInpRes	P5DebOn	P2DebOn	P1DebOn

5.5 Reset Output

The Reset output outputs the CPU-reset signal. This signal is triggered by a system reset and its duration is the oscillator start time plus the cold start delay time.
The output buffer has the same electrical parameters as the port P5 output buffers.

6. Oscillators

By metal option the 32kHz quartz oscillator can be replaced by external clock coming from QOUT terminal.
When external clock is used Xtal oscillator can not work.

6.1 32kHz Oscillator

The 32768Hz quartz oscillator of the EM6635 is working and supplies the timing functions with precise clock frequencies. The necessary oscillator capacitors are integrated within the EM6635, therefore the only external element needed is the 32kHz quartz.
The external impedance between QOUT and QIN terminal must be higher than 10MOhm.
As this type of oscillator has a relatively slow start-up behavior, precautions are necessary to make sure, that always corrects 32Khz clock signals are provided at the system start. The flag ColdStart in “RCOSC” to high level (bit2, address H6D) indicates an active Quartz Oscillator ColdStart delay when circuit starts to run under RC oscillator and ColdStart is not finished yet.
The 32kHz signal can be used to clock the µProcessor. This selection is done by setting OscSwitch in “RCOSC” to low level (bit 0, address H6D). The default selection at system start is the RC oscillator (metal option OP-20 A) or the Quartz oscillator (metal option OP-20 B).

6.2 RC Oscillator

The EM6635 has an internal RC oscillator, which delivers a fast clock for the µProcessor. This RC oscillator can be switched On or Off by the CPU with EnRC in “RCOSC” (bit 1, address H6D). A high level activates the RC oscillator. After a system start, the RC oscillator is active (metal option OP-20 A is selected).
The µProcessor can be configured to run with the 32kHz clock of the Quartz Oscillator. In this case, the RC oscillator can be set inactive. This selection is done by setting OscSwitch in “RCOSC” to low level.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
RCOSC	6D	109	W	x	x	EnRC	OscSwitch
			R	0	ColdStart	EnRC	OscSwitch

Note1: “RCOSC” register value is depending on supply voltage and metal option. With the metal option: OP-20B, Init=0100 and OP-20A, Init=0111. When 3.00V range is operating, register value can be set to 0111. When very low voltage e.g.1.2V is operating, register value must be set to 0000.

6.3 External Clock Input

RC and/or external clock where external clock replaces the Xtal frequency and supplies the main prescaler.
These inputs must be specified according to mask option OP-19 and OP-20. See chapter 17.
QOUT terminal becomes the external clock.

6.4 Clock Switching Notes

When switching the CPU from Quartz Oscillator to RC Oscillator, it’s start-up time of max. 1ms must be respected. First EnRC must be set to 1 and after 1ms also OscSwitch can be set to 1. In order to synchronise the internal logic a Xtal clock of 32kHz is taken into account, then the RC Oscillator delivers fast clocks to the µProcessor.

The internal voltage regulator at VRR terminal increases of 280mV typically. The stabilisation is depending of external loads (CVRR minimum = 100nF).
When switching off the RC Oscillator, first OscSwitch must be set to 0 and earliest in the following instruction EnRC can be cleared to 0. The internal voltage regulator decreases to its initial value.
An error in the CPU operation can result if the 2 sequences are not performed correctly.

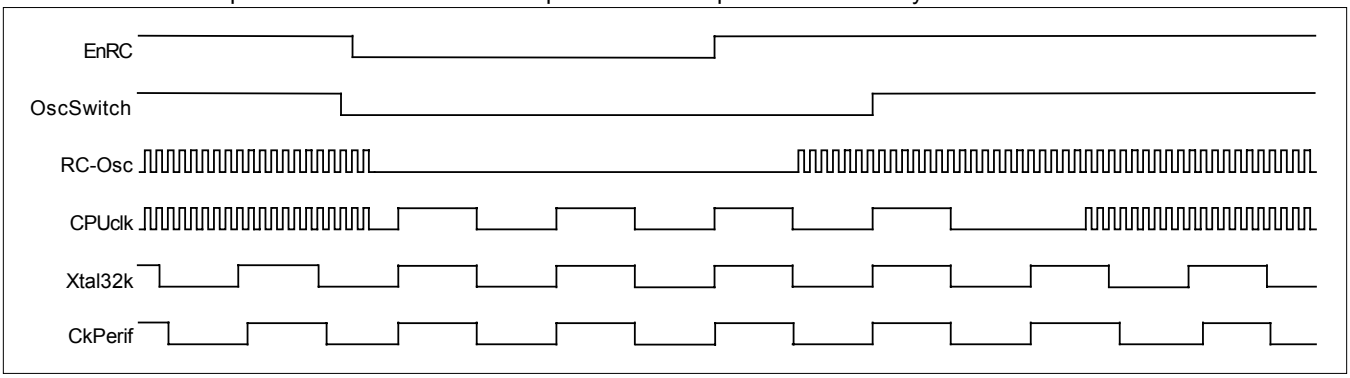


Fig.7: Clock Switching from RC-Oscillator to 32kHz and back

7. Prescaler

The prescaler is a 15 stages divider chain, which delivers clock signals for the peripheral circuits such as timer, frequency generator, debouncer, etc. The input is the 32768Hz system clock from Quartz Oscillator or external clock.
Note*:* if external clock is applied it should be also 32768Hz to keep timing specified in this specification, in other case all timing change relative to external clock compared to 32768Hz.

The system reset initialises the prescaler to all 0, except the 1s stage, which is set to 1.
The prescaler generates four interrupt requests: INT-TB1, INT-TB2, INT-TB3, INT-TB4.
The source is selected by Sel/INT8.

Interrupt	Sel/INT8	
	0	1
TB1	1Hz	1Hz
TB2	64Hz	8Hz
TB3	32Hz	16Hz
TB4	128Hz	64Hz

Both interrupts appear at the positive edge of the corresponding signal.
The first INT_TB1 occurs 1 sec after the end of the system reset.
The prescaler can be reset partially from 32Hz to 1Hz by writing "1" to "ResetCK" of HW-Ctl-2 (bit 0 at address H43). A read access to that bit gives always "0".
Note: this prescaler reset shortens the watchdog time out tWD.

The prescaler creates a clock signal for the clocked pull down at inputs, e.g. at port P1. This is a 512Hz signal with an active time of 31µs if OP-6A is chosen or 64µs at OP-6B.

7.1 Time Base Capture

The state of the prescaler stages 128Hz to 16Hz and 8Hz to 1Hz can be read by the CPU by a read access to address H55 (a write has no effect). The range selection is done by bit 3 of HW-Ctl-2, address H42 or H43. A "1" at this "SelTBCapHi" selects the range from 128Hz to 16Hz for read.
This time base capture capability is mostly designed for 4 bits application. The corresponding data are directly read from the prescaler. If two consecutive capture accesses are made to read the two ranges, the resulting data representation (8 bits) may not be coherent, due to a possible prescaler update event occuring to the 128 Hz stage plus its correlated carry to the following stages.

8. EM6635 Input / Output Ports

8.1 Input Port P1

The port P1 is a 4bits input port used to read the terminal logic levels P10 to P13 into the CPU.
The port is equipped with 4 debouncers, which can be enabled by signal "P1DebOn", commonly for all 4 bits. With debouncers active, any input level must be present glitch free for at least the debounce time tDEB=1.95ms, to be transferred to the debouncer output, which can be read by the CPU.
When "P1DebOn" is at "0" level, the port P1 inputs are directly passed to the debouncer outputs.

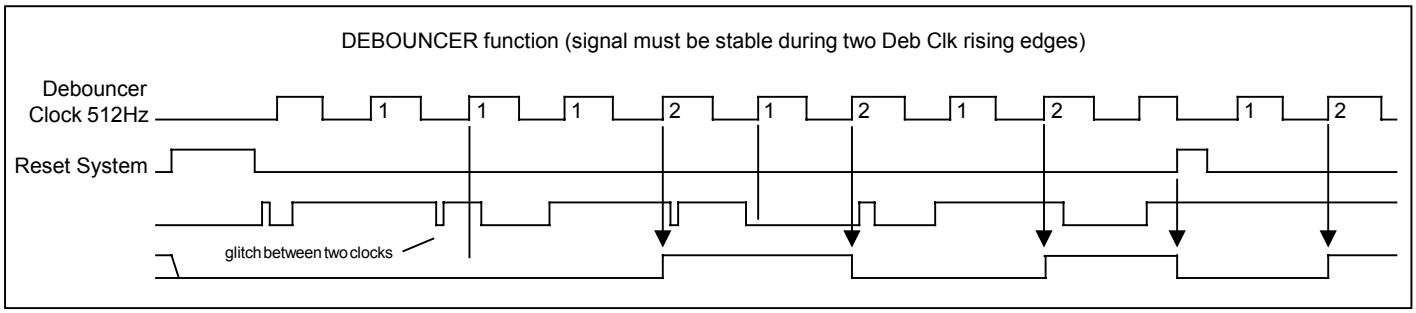


Fig.8: Debouncer function

The port P1 has several special functions assigned to its inputs:

8.1.1 Edge Detector

The port input P10 and P11 have edge detectors connected to the corresponding debouncer outputs. Both edge detectors create output signals of 488us at positive and negative edges. Each edge detector pulse from P10 or P11 input creates a pulse "M", which is the clock input for the event counter. Every change at P10 or P11 creates an "M" pulse.
Also, an interrupt "M" is generated by this signal
The P13 input is logically combined as "AND" with P22 and P23 input, then input into a debouncer, whose output creates an Input Reset if enabled.

8.1.2 Input Interrupt

The port P12 input (after debouncer) is connected to an edge detector, active at positive and negative edges. Its 488us output signal creates an interrupt P12 in register INT-Stat-2 (bit 0, address H66).
The port P13 input (after debouncer) is connected to an edge detector, active at positive and negative edges. Its 488us output signal creates an interrupt P13 in register INT-Stat-2 (bit 1, address H66).

8.1.3 Input Pull Down

Each P1 input has associated pulldown transistors. These NMOS transistors are activated with a 512Hz signal with the duration of 31us (OP-6A) or 62us (OP-6B). A "0" input level is additionally hold by the circuitry shown in fig.8:

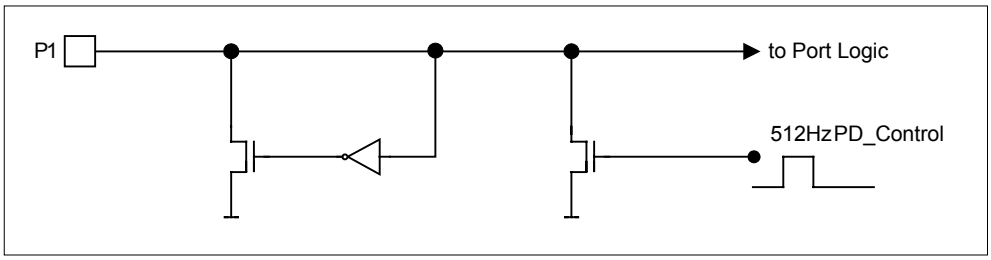


Fig.9: Port P1, P2 Input Pull Down

The pull down elements at port 1 can globally be disactivated by mask option OP-7B.

Note: Extra pull down transistors are active at this port during the CPURES signal.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Config2	45	69	W R	(DisInpRes) (DisInpRes)	(P5DebOn) (P5DebOn)	(P2DebOn) (P2DebOn)	P1DebOn P1DebOn
Port P1	47	71	R	P13	P12	P11	P10

8.2 Input Port 2

The port P2 is a 4bits input port used to read the terminal logic levels P20 to P23 into the CPU.
The port is equipped with 4 debouncers, which can be enabled by signal "P2DebOn" commonly for all 4 inputs. With debouncers active, any input level must be present glitchfree for at least the debouncer time tDEB =1.95ms, to be transferred to the debouncer output, which can be read by the CPU.
When "P2DebOn" is at "0" level, the port P2 input is directly passed to the debouncer outputs.

Port 2 Interrupt:
Each debouncer output of port 2 is connected to the input of a positive edge dedector. The 4 edge detector outputs are logically combined as OR to create the P2 interrupt signal INT-P2 (bit 1, address H68).
In this way, any valid positive transition at P2 input can create an interrupt if not masked.

The P22 and P23 inputs are combined logically as "AND" with P13 input and applied to a debouncer. The debounced signal can create an Input Reset if not disabled by "DisInpRes".
Each P2 input has associated pull down transistors. These NMOS transistors are activated with a 512 Hz signal with the duration of 31µs (OP-6A) or 62µs (OP-6B). A "0" input level is additionally hold by the circuitry shown in Fig. 8.
The pull down elements at port P2 can globally be disactivated by mask option OP-14B.

Note: Extra pull down transistors are active at this port during the CPURES signal.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Config2	45	69	W R	DisInpRes DisInpRes	(P5DebOn) (P5DebOn)	P2DebOn P2DebOn	(P1DebOn) (P1DebOn)
Port 2	48	72	R	P23	P22	P21	P20

8.3 Input/Output Port P3

The port P3 is a 4bit input/output port with high current drive capability, e.g. for watch motor driver.
The port direction is controlled by the "PIO43 Ctl" register at address H52. The bit "P3-Dir" (bit 0, address H52) defines the direction of P30 to P32 commonly, whereas "P33-Dir" (bit 2, address H52) defines the individual direction of P33. A "1" level of the direction bit configures the corresponding port to be output, a "0" level defines it as input.
If the port P3 is configured as output, a write access to the P3 data register (address H50) stores the data into the internal port data register and the data appear at the corresponding port terminals. The port data register is only written when the port bit is output.

If a port P3 bit is read when the port is output, the data comes from the port output register. When the port is input, the data is read from the port terminal (output buffer in high impedance). The data LSB is at bit 0, the MSB at bit 3.
After system reset, the direction is input, the output data register contains "0000".
At port P3, no pull up or pull down element is available during normal operation.
Note: Extra pull down transistors are active at this port during the CPURES signal.

8.3.1 Frequency Output

With mask option OP-18, the function of the output P33 can be modified directly or under CPU control. If OP-18A is chosen, the CPU can select with “ENFOut” set to “1”, that the port P33 is set to output, but disconnected from its data register. Instead, it is configured as frequency output.
The output frequency is defined by the serial clock selection bits "SelSIOClk0, “1" in SIO-Ctl1(bit 3, address H72), independent of the "EnSIO" state, which enables the serial interface, configurated at port P5.
If the frequency output is set to 32 kHz, the output signal is the system clock from the quartz oscillator. In this case, the duty cycle is subject to higher tolerances than in case of the other possible output frequencies. If option OP-18B is chosen, the output P33 is always output for Fout, independently of the setting “ENFOut”.

SelSIOClk1	SelSIOClk0	Frequency at Fout = P33
0	0	according to OP-8: 1kHz - 512Hz - 128Hz - 32Hz
0	1	32kHz
1	0	16kHz
1	1	4kHz

8.3.2 Synchron Mode (Special Motor Mode)

If timer 1 is set to Synchron Mode by "SynMode" = "1", the port P3 operates in a special way, optimised to facilitate driving of watch motors.
The port must be set to output by the "PIO43-Ctl" register bits "P3-Dir" and/or "P33-Dir". An eventually "EnFOut" configuration has priority over Synchron Mode setting for port P33.
The Synchron Mode can work with the P30 to P32 bits alone or together with P33, if this port is also set to output and not frequency output.

Function:
As long as timer1 is not actively counting (its "TimerOn" signal is "0"), all the selected port P3 outputs are in "1" state.
During active timer 1 counting, the selected P3 outputs correspond to the content of the port P3 output data register. The port state returns to all "1" after timer 1 has finished.
In this way, a predefined pattern loaded in the data output register appears synchronously with the timer 1 action for the programmed time at the P3 output, driving e.g. a stepper motor. (See also timer 1 description, Synchron Mode).

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Port P3	50	80	W	P33 (Fout)	P32	P31	P30
			R	P33 (Fout)	P32	P31	P30
PIO43 Ctl	52	82	W	(P43-Dir)	P33-Dir	(P4-Dir)	P3-Dir
			R	(P43-Dir)	P33-Dir	(P4-Dir)	P3-Dir

8.4 Input / Output Port P4

The port P4 is similar to port P3: it is also a 4bits input/output port with high current drive capability, e.g. for watch motor driver.

The port direction is controlled by the "PIO43 Ctl" register at address H52. The bit "P4-Dir" (bit 1 of address H52) defines the direction of P40 to P42 commonly, whereas "P43-Dir" (bit 3 of address H52) defines the individual direction of P43. A "1" level of the direction bit configures the corresponding port to be output, a "0" level defines it as input.
If the port P4 is configured as output, a write access to the P4 data register (address H51) stores the data into the internal port data register and the data appear at the corresponding port terminals.
The port data register is only written when the port bit is output.

If a port P4 bit is read when the port is output, the data comes from the port output register. When the port is input, the data is read from the port terminal (output buffer in high impedance). The data LSB is at bit 0, the MSB at bit 3.
After system reset, the direction is input, the output data register contains "0000".
At port P4, no pull up or pull down element is available during normal operation.
Note: Extra pull down transistors are active at this port during the CPURES signal.

8.4.1 Synchron Mode

As port P3, port P4 can be configured in Synchron Mode. But additionally to the setting of timer 1 in "SynMode", the bit "Mot3Mode" in "Config1" register (bit 3, address H44) must be set to "0".
In this configuration, the selected number of port outputs can apply the loaded data pattern during timer 1 action to the output terminals, as explained in port P3 description.
The maximum number of outputs is 9 (included P72), other possible configurations are 8, 7, 6, or 4, 3 using P3 only.
If "Mot3Mode" is set to "1", only port P3 is configured from "SynMode" of timer 1 as Synchron Mode output and P4 is normal input/output.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Config-1	44	68	W R	Mot3Mode Mot3Mode	(DisWD) (DisWD)	(EnFOut) (EnFOut)	SelINT8 SelINT8
Port P4	51	81	W R	P43 P43	P42 P42	P41 P41	P40 P40
PIO43 Ctl	52	82	W R	P43-Dir P43-Dir	(P33-Dir) (P33-Dir)	P4-Dir P4-Dir	(P3-Dir) (P3-Dir)

8.5 Input / Output Port P5

The port P5 is a 4bits input/output port with normal current drive capability outputs. It can be configured as a serial interface.

8.5.1 Parallel Mode

The direction of each port bit can be defined individually by the "PIO5 Ctl " register (address H54). A bit of this register set to "1" defines the corresponding port terminal as output.
If the port P5 is configured as output, a write access to the P5 data register (address H53) stores the data into the internal port data register and the data appear at the corresponding port terminals.
The port data register is only written when the port bit is output.

If a port P5 bit is read when the port is output, the data comes from the port output register. When the port is input, the data is read from the port terminal (output buffer in high impedance). The data LSB is at bit 0, the MSB at bit 3.
After system reset, the direction is input, the output data register contains "0000".

Note: Extra pull down transistors are active at this port during the CPURES signal.

As input, the port P5 is equipped with 4 debouncers, which can be enabled by signal "P5DebOn" (bit 2, address H45) commonly for all 4 bits. With debouncers active, the input level must be present glitch free for at least the debouncer time t_{DEB}=1.95ms, to be transferred to the debouncer output, which can be read by the CPU.
When "P5DebOn" is at "0" level, the port P5 inputs are directly passed to the debouncer outputs.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Port P5	53	83	W	P53	P52	P51	P50
			R	P53	P52	P51	P50
PIO5 Ctl	54	84	W	P53-Dir	P52-Dir	P51-Dir	P50-Dir
			R	P53-Dir	P52-Dir	P51-Dir	P50-Dir

8.5.2 Serial Interface Mode

The port P5 is configured as 4 wire serial port, if "EnSIO" (bit 1, address H73) is set to "1".
In this serial mode, the port P5 bits have following functions:

P53: serial clock input/output: SCK
P52: serial output: SOUT
P51: serial status input/output: RDY
P50: serial input: SIN

It is possible, to select by SW the serial clock frequency, the serial word length, the active clock edge, the output mode and RDY function. Pull down or pull up resistors can be activated by mask option OP-10.

General Description

For data input, a 5 to 8bit shift register converts the serial input data from the SIN terminal to a parallel format, which can be read by the CPU. The low nibble is accessible at address H70: "SIO Low-Data" (LSB at bit0) and the high nibble is at "SIO Hi-Data" at address H71.
For data output, the CPU loads data into the shift register in two steps (SIO Low-Data and SIO Hi-Data), which is then output serially to SOUT terminal.
It is possible to simultaneously shift data out to SOUT and to shift data in from SIN.
In the master mode, the serial clock is generated internally, corresponding to the selection done by "SIO-Ctl1" (address H72) and output to SCK.
In slave mode, an external clock is input to SCK.
The active clock edge is selected in "SIO Ctl2" by "NegEdg" bit 2, address H73.
The shift direction is always MSB-first.
The RDY signal controls the serial transmission or indicates to an external circuit, if the serial interface is ready for a new transmission. RDY is input in master mode and output in slave mode, if not otherwise configured by "SIO Ctl3" register.
As output, RDY can also be set to "1" by the CPU.
After data nibbles are loaded in " SIO Low-Data " and " SIO Hi-Data " registers, the CPU can start a serial transmission by setting the "RUN" bit3 at "SIO-Ctl2" (address H73) to "1". (By writing "0" to "RUN", a current transmission is stopped without interrupt.)
In slave mode, the RDY output becomes "1" until the transmission is completed. In master mode, the RDY is input. The serial interface waits until the RDY input becomes "1" and starts then the transmission. (All RDY level indications are given for direct input/output selection done in "SIO Ctl3" by SelRDYPol1, -0)

The CPU can read the "RUN" status (bit3 at SIO Ctl2), which is cleared to "0" by the serial port logic when the transmission has finished.

As master, the serial port logic generates the number of serial clocks SCK according to the selected word length (in SIO Ctl1: SelWL1, 0, address H72).
After the last serial clock SCK, an interrupt INT_SIO is generated (bit 0, address H68).
When slave, the external clocks applied to SCK are counted. When the defined number is reached, the transmission is stopped and interrupt INT-SIO is generated.
With "NegEdg" = "0" ("SIO Ctl2", bit2, address H73) the active SCK clock edge is positive, the shift register shifts at the negative edge. If "SelSynOut" is set to "1" (synchronised output mode), the output synchronisation is done with the positive clock edge. If "SelSynOut" is "0", the output SOUT is in direct output mode and changes with the negative clock edge as the shift register.
When "NegEdg" is set to "1", all above mentioned clock edges are inverted.

The SIO Low-Data and SIO High-Data register can only be read, if EnSIO is set to Hi.

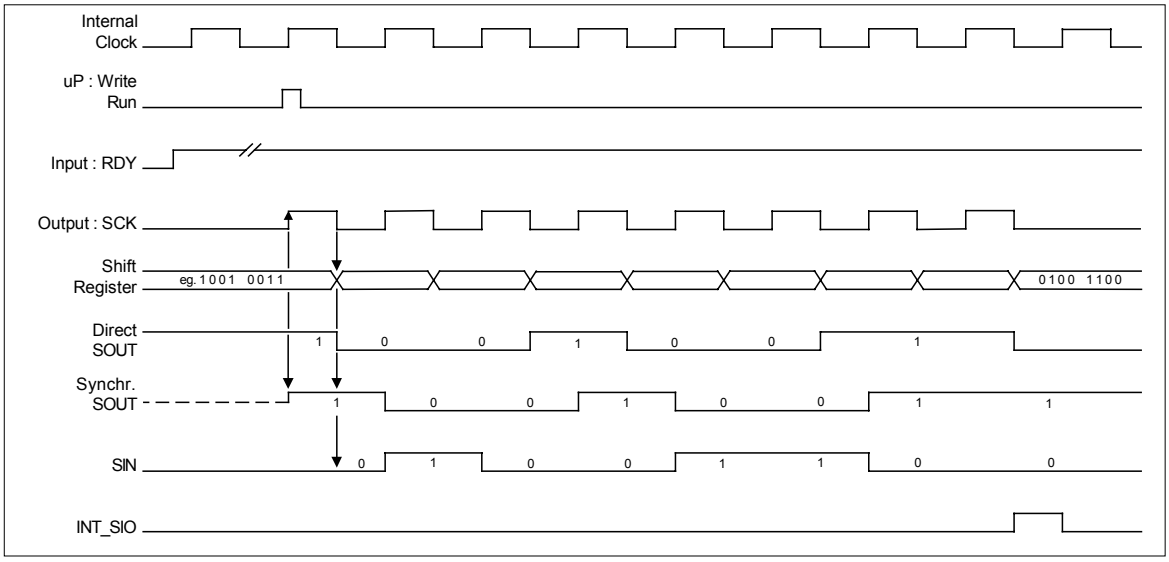


Fig.10A: Serial Interface Operation Timing in Master Mode, 8bit, positive clock

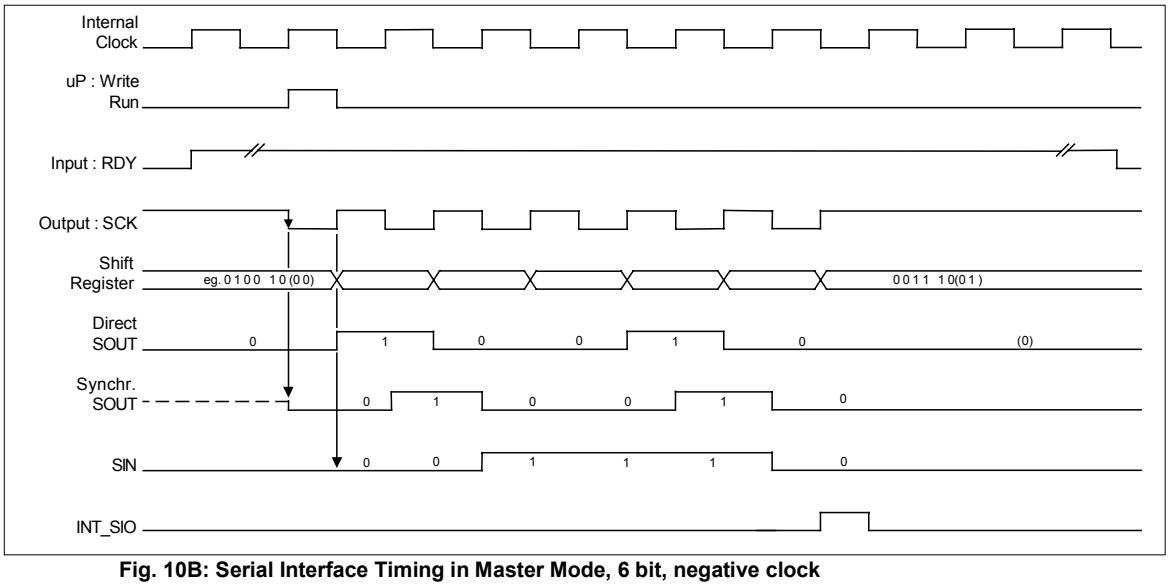


Fig. 10B: Serial Interface Timing in Master Mode, 6 bit, negative clock

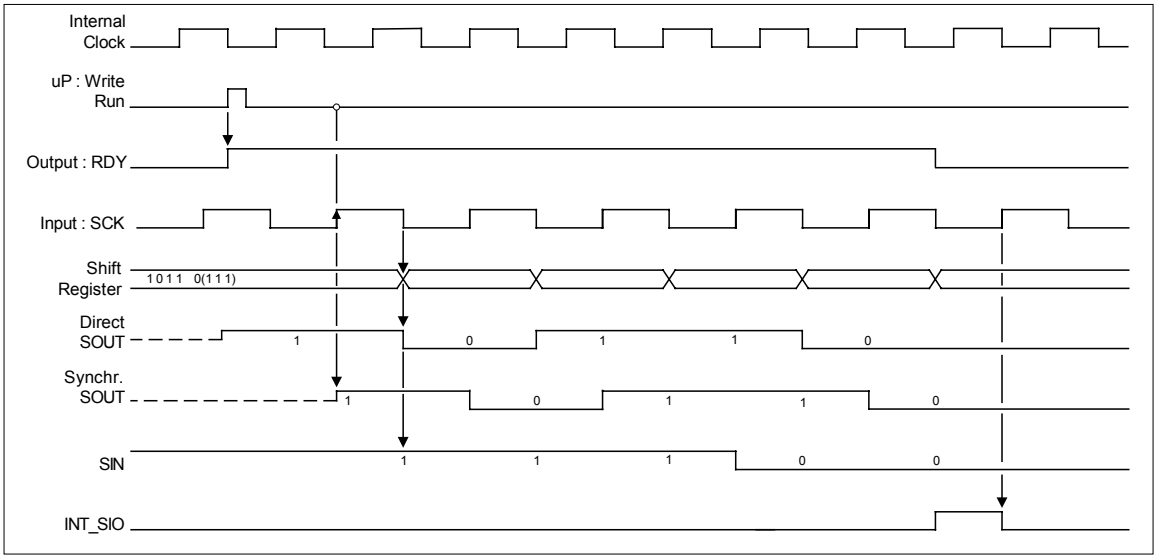


Fig. 10C: Serial Interface Timing in Slave Mode, 5 bit, positive clock

The register "SIO Ctl1" defines the serial clock frequency with "SelSIOClk1, 0" at bit 3, 2 and the serial word length with "SelWL1, 0" at bit 1, 0.

SelSIOClk1	SelSIOClk0	SCK Frequency	RDY	Fout
0	0	ext. clock: Slave Mode	Output	acc. Option
0	1	32kHz internal: Master Mode	Input	CK32K
1	0	16kHz internal: Master Mode	Input	CK16K
1	1	4kHz internal: Master Mode	Input	CK4K

SelWL1	SelWL0	Serial Word Length
0	0	8 bit
0	1	7 bit
1	0	6 bit
1	1	5 bit

The mode of port P5 and output mode of serial mode are defined by "SIO Ctl2", "EnSIO" and "SelSynOut" according to following table:

EnSIO	SelSynOut	Port 5 Mode
0	x	Parallel Input/output
1	0	Serial Port, direct Output
1	1	Serial Port, synchronized Output

With "SIO Ctl3", the mode of the RDY signal can be defined in multiple ways. The polarity of RDY output and input is selected with "SelRDYPol1, -0" (bit 1, 0 of address H74) according to following table:

SelRDYPol1	SelRDYPol0	RDY Polarity	
0	0	RDY is direct input	or direct output
0	1	RDY is inverted input	or direct output
1	0	RDY is direct input	or inverted output
1	1	RDY is inverted input	or inverted output

The bit "RDYisOutput" (bit2 of SIO Ctl3) forces the RDY-terminal to be output, regardless of master- or slave mode, when set to "1" level.
The "RDYactive" (bit3 of SIO Ctl3) allows the CPU to set RDY-output directly to "1". The RDY output is then a logical OR function of this bit and the value delivered from the serial logic control. RDY must be set to output by RDYisOutput = Hi.
If port P33 is configured as frequency output by "EnFOut" = "1", its frequency is the same as the serial clock in master mode and has the same polarity, if "NegEdg"is at "0".

8.5.3 Pull Down / Up Resistors at Port P5

For each port P5 terminal, a pull down or a pull up resistor can be activated by mask option OP-10 to OP-13.
Activated resistors are only connected if the port terminal is input.
Activation is valid for parallel and serial mode of the port P5.
Each mask option offers 3 choices: A: no resistor B: pull up resistor C: pull down resistor
The options can be individually defined for each terminal.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
SIO Low-Data	70	112	W	MSB Low Nibble	<----------	---------->	LSB Low Nibble
			R	MSB Low Nibble	<----------	---------->	LSB Low Nibble
SIO Hi-Data	71	113	W	MSB Hi Nibble	<----------	---------->	LSB Hi Nibble
			R	MSB Hi Nibble	<----------	---------->	LSB Hi Nibble
SIO Ctl1	72	114	W	SelSIOClk1	SelSIOClk0	SelWL1	SelWL0
			R	SelSIOClk1	SelSIOClk0	SelWL1	SelWL0
SIO Ctl2	73	115	W	RUN	NegEdg	EnSIO	SelSynOut
			R	RUN	NegEdg	EnSIO	SelSynOut
SIO Ctl3	74	116	W	RDYactive	RDYisOutput	SelRDYPol1	SelRDYPol0
			R	RDYactive	RDYisOutput	SelRDYPol1	SelRDYPol0

8.6 Input / Output Port P6

With the metal option OP-22B, the port P6 is a 4bits input/output port with normal current drive capability outputs.

The port direction is controlled by the "PIO67 Ctl" register at address H4C. The bit "P601-Dir" (bit 0, address H4C) defines the direction of P60, P61 and the bit "P623-Dir" (bit 1, address H4C) defines the direction of P62, P63. A "1" level of the direction bit configures the corresponding port to be output, a "0" level defines it as input.
If the port P6 is configured as output, a write access to the P6 data register (address H4A) stores the data into the internal port data register and the data appear at the corresponding port terminals. The port data register is only written when the port bit is output.
If a port P6 bit is read when the port is output, the data comes from the port output register. When the port is input, the data is read from the port terminal (output buffer in high impedance). The data LSB is at bit 0, the MSB at bit 3.
After system reset, the direction is input, the output data register contains "0000".

As input, the port P6 is equipped with 4 debouncers, which can be enabled by signal "P6DebOn" (bit 0, address H46) commonly for all 4 bits. With debouncers active, the input level must be present glitch free for at least the debouncer time t_{DEB} = 1.95ms, to be transferred to the debouncer output, which can be read by the CPU.
When "P6DebOn" is at "0" level, the port P6 inputs are directly passed to the debouncer outputs.

The port P6 input (after debouncer) is connected to an edge detector, active at positive edges. The 4 edge detector outputs are logically combined as OR to create the P6 interrupt signal INT-Stat-4 (bit 1, address H6A).
In this way, any valid positive transition at P6 input can create an interrupt if not masked.

Note: Extra pull down transistors are active at this port during the CPURES signal.

For each port P6 terminal, a pull down or a pull up resistor can be activated by mask option OP-24 to OP-27.
Activated resistors are only connected if the port terminal is input.
Each mask option offers 3 choices: A: no resistor B: pull up resistor C: pull down resistor
The options can be individually defined for each terminal.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Config3	46	70	W	x	x	(P7DebOn)	P6DebOn
			R	0	0	(P7DebOn)	P6DebOn
Port 6	4A	75	R	P63	P62	P61	P60
PIO67 Ctl	4C	76	W	(P72-Dir)	(P7-Dir)	P623-Dir	P601-Dir
			R	(P72-Dir)	(P7-Dir)	P623-Dir	P601-Dir

8.7 Input / Output Port P7

With the metal option OP-23B, the port P7 is a 2bits input/output port P70, P71 with normal current drive capability outputs. P72 input/output is high current drive capability for watch motor driver (metal option OP-21A), 5mA led driver (metal option OP-21B, OP-21C) or only high current drive capability (metal option OP-21D).

As port P3 or P4, P72 can be configured in Synchron Mode. But additionally to the setting of timer 1 in "SynMode", the bit "Mot3Mode" in "Config1" register (bit 3, address H44) must be set to "0". For more details refer to chapter 8.3 and 8.4

The port direction is controlled by the "PIO67 Ctl" register at address H4C. The bit "P701-Dir" (bit 2, address H4C) defines the direction of P70 to P71 commonly. A "1" level of the direction bit configures the corresponding port to be output, a "0" level defines it as input.
The bit "P72-Dir" (bit 3, address H4C) defines the direction of P72.
If P70, P71and P72 are configured as output, a write access to the P7 data register (address H4B) stores the data into the internal port data register and the data appear at the corresponding port terminals. The port data register is only written when the port bit is output.
If P70, P71 and P72 bits are read when the port is output, the data comes from the port output register. When the port is input, the data is read from the port terminal (output buffer in high impedance). The data LSB is at bit 0, the MSB at bit 2.
After system reset, the direction is input, the output data register contains "0000".
As input, P70 and P71 are equipped with 2 debouncers, which can be enabled by signal "P7DebOn" (bit 1, address H46) commonly for 2 bits. With debouncers active, the input level must be present glitch free for at least the debouncer time t_{DEB} = 1.95ms, to be transferred to the debouncer output, which can be read by the CPU.
When "P7DebOn" is at "0" level, P70 and P71 inputs are directly passed to the debouncer outputs.

P70, P71 inputs (after debouncer) are connected to an edge detector, active at positive edges. The 2 edge detector outputs are logically combined as OR to create the P7 interrupt signal INT-Stat-4 (bit 2, address H6A).
In this way, any valid positive transition at P70 or P71 input can create an interrupt if not masked.

Note: Extra pull down transistors are active at this port during the CPURES signal.

For P70, P71 terminal, a pull down or a pull up resistor can be activated by mask option OP-28 and OP-29.
Activated resistors are only connected if the port terminal is input.
Each mask option offers 3 choices: A: no resistor B: pull up resistor C: pull down resistor
The options can be individually defined for each terminal.

At P72, no pull up or pull down element is available during normal operation.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Config3	46	70	W R	x 0	x 0	P7DebOn P7DebOn	(P6DebOn) (P6DebOn)
Port 7	4B	75	R	0	P72	P71	P70
PIO67 Ctl	4C	76	W R	P72-Dir P72-Dir	P701-Dir P701-Dir	(P623-Dir) (P623-Dir)	(P601-Dir) (P601-Dir)

Note: If the terminal P72 is not connected or not used, it must be an output.
A "1" level of the direction bit "P72-Dir" (bit 3, address H4C) configures as output.
In other case an over consumption will occur.

8.7.1 Back Light function on P70 and P71

A special function of generating ELC and ELP clock can be attributed to P70 and P71 when selected and declared as outputs. Control bits for this function are in register Backlit.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Backlit	78	120	W R	Blout BLout	StartBL startBL	ELPcksel ELPcksel	ELCcksel ELCcksel

ELC is a signal of 256 Hz or 512 Hz with 25 % duty cycle. Selection is done by bit ELCcksel.
ELP is a signal of 8.192 kHz or 16.384 kHz with 75% duty cycle which is inserted between ELC signal when ELC is low. Frequency selection is done by ELPcksel.
Function is initiated by writing **StartBL** control bit to 1 and **Blout** must be set to 1 to dedicate P70 when declared as output to ELC output and P71 to ELP output. Start of a sequence is synchronized by 512 or 1024 Hz signal from prescaler and repeats until StartBL bit is cleared to 0 while Blout is still set to 1. For proper sequence end first StartBL must be cleared to 0 and only when sequence finish – final ELC positive pulse following the end of StartBL, Blout can be cleared to 0 or port changed to input.

Note: when StartBL is cleared to end the sequence with the next positive ELC pulse, ELPcksel and ELCcksel selection bits must not be cleared but must keep the same value as when StartBL was set. If not the rest of the sequence will have default timing 256Hz for ELC and 8192Hz for ELP signal !!
By default this function is not selected and P70, P71 are general I/O pins as described in chapter 8.7.

ELPcksel	ELCcksel	ELP freq [Hz]	ELC freq [Hz]
0	0	8192	256
0	1	8192	512
1	0	16384	256
1	1	16384	512

Table showing ELP and ELC frequency selection

Blout	P701-Dir	P70	P71
0	0	General Input	General input
0	1	General Output	General Output
1	0	General Input	General Input
1	1	Back light ELC Output	Back light ELP Output

Table showing P70, P71 function depending on Blout and P701-Dir control bits

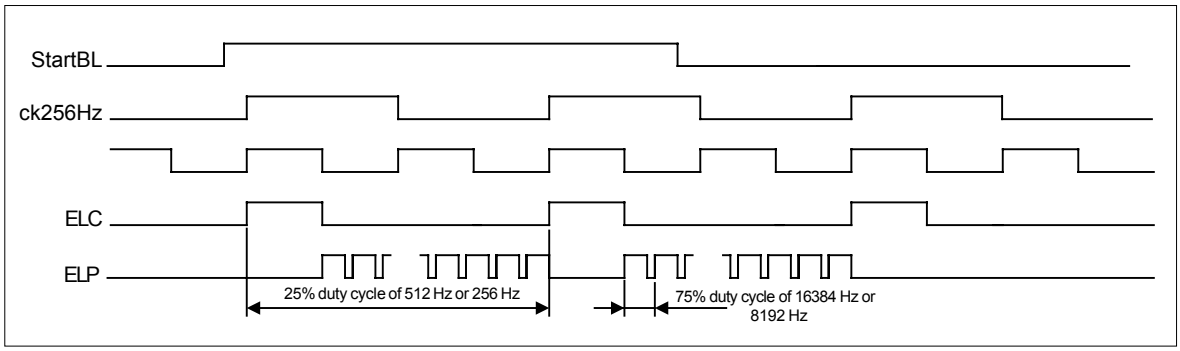


Fig. 10D: Back Light ELC and ELP signals in case where ELC is 256 Hz based.

In above picture it is shown that the sequence is started by setting StartBL to 1, together with ELPcksel and ELCcksel clock selection. Than it is synchronized to first rising edge of doubled frequency clock coming from the prescaler, that it starts with ELC 25% duty cycle signal and stops with one ELC positive pulse following the StartBL cleared to 0. Between ELC positive pulses (when ELC is low) is inserted ELP with 75% duty cycle of selected 16384 or 8192 Hz.

9. Timer 1

The timer 1 can operate in three modes: the Zero Stop, the Synchron Mode and the Auto Reload Mode.
The clock frequency can be selected by "SelT1F2" and "SelT1F1" control bits in "Timer1 Ctl" at address H56:

SelT1F2	SelT1F1	Timer 1 Clock Frequency
0	0	512 Hz
0	1	1024 Hz
1	0	2048 Hz
1	1	4096 Hz

During active counting down, in all modes, the CPU can change the timer clock frequency. The new frequency is immediately applied, so the remaining timer counts until zero will be generated according to the new frequency selection. Inaccuracy is added, because the transitory counter cycle is generated with parts from two different clock periods. Additionally, a parasitic clock transition may be generated depending on the actual prescaler clock signal levels.
The CPU writes divider data in two steps, first the higher 4bits into “Timer1 Hi-Data" (address H57) and then the lower 4bits into "Timer1 Low-Data" (address H58). This corresponds to an 8bit-timer.
The CPU can also write divider data in one step, only the lower 4 bits into "Timer1 Low-Data" (address H58). This corresponds to a 4bit-timer.
The timer contains an 8bits or a 4bits down counter, which can be loaded by the CPU via an autoreload register with “Timer1 Hi-Data" at address H57 (MSB at bit 3) and "Timer1 Low-Data" at address H58 (LSB at bit 0). The timer generates a “Timer1” interrupt (bit2, address H64) when it arrives at the all-zero-state of its counter. When a zero is loaded as data into the timer, and the timer is actively counting down, it is stopped, but no interrupt will occur.

9.1 Zero Stop Mode

If "SynMode" and "ARMode" are at "0", the timer1 is in Zero Stop Mode.
As soon as the CPU has written a non-zero value into “Timer1Hi-Data" and "Timer1 Low-Data", the timer1 starts counting down from this value with the selected clock frequency. When arrived at zero, the interrupt "Timer1" is generated.
The timer remains at the zero state until it is loaded again with data.
The timer period from CPU write access to "Timer1" interrupt is:
Load Value*Timer Clock Period - (0...1) Timer Clock Period
After a system reset, the timer is in Zero Stop Mode and in zero state.
If the timer 1 is reloaded by the CPU in Zero Stop mode, while it is counting, the actual counter state will be overwritten and a new counting down cycle starts with the new value loaded. No interrupt will be generated.

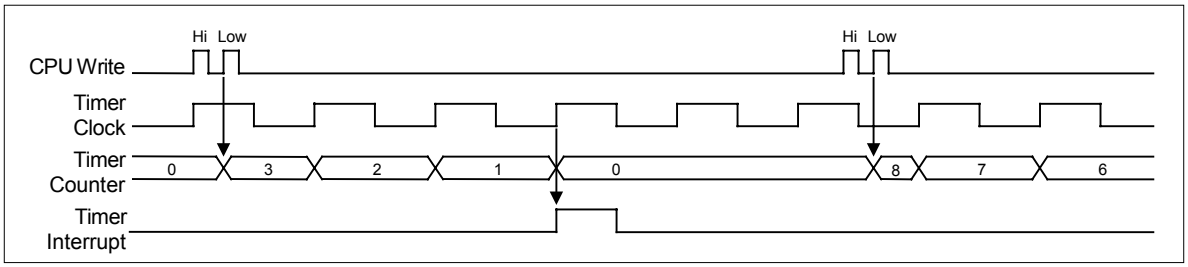


Fig.11: Timer 1 Timing in Zero Stop Mode

9.2 Synchron Mode

The timer 1 works in this special mode, when the "SynMode", bit3 of "Timer1 Ctl" is set to "1".
When the CPU has loaded non-zero data into the timer, the counter is not starting immediately. It waits to be triggered by the positive edge of the prescaler 64Hz signal. From this event on, it is counting down to zero and stops there.
When arrived at zero, the interrupt "Timer1" is generated.
During its counting down action, the timer generates a "TimerOn" signal, which is used in port P3, P4 and P72 (metal option OP21-A) to enable data output (see description of ports P3, P4 and P7).
The timer period from positive edge of 64 Hz signal to timer1 interrupt is:

Load Value*Timer Clock Period - 1/2 Timer Clock Period

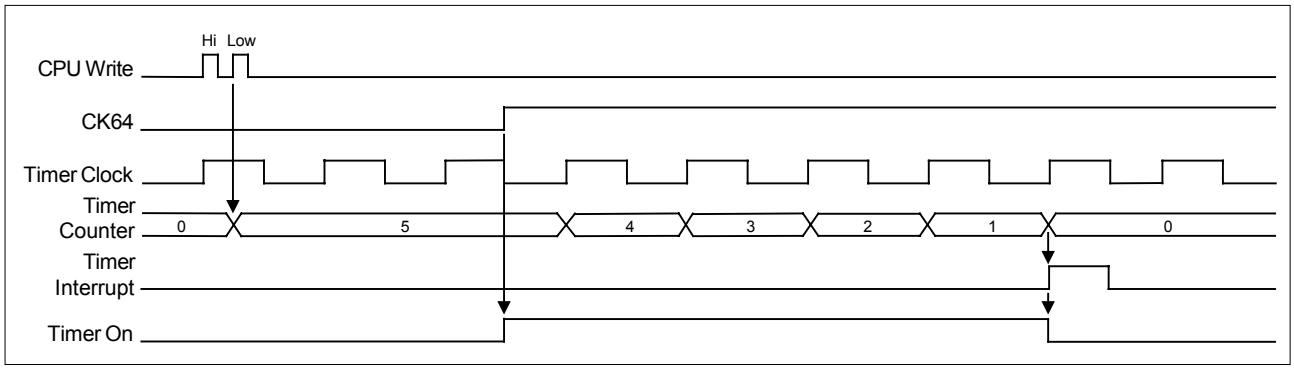


Fig.12: Timer 1 Timing in Synchron Mode

9.3 Auto Reload Mode

The timer 1 works in Auto Reload Mode, if the "ARMode", bit 2 of "Timer1 Ctl", address H56 is set to "1". The timer starts counting down, when a non-zero data is loaded into its 2 reload registers (address H57, "Timer1 Hi-Data" and address H58, "Timer1 Low-Data"). When the counter has arrived at zero state, a "Timer1" interrupt is generated. The counter is then automatically reloaded with the data stored in the reload register (previously written there by the CPU), and starts again to count down.
This sequence is repeated until the Auto Reload Mode is stopped by setting the "ARMode" bit to "0".
If the CPU reloads the timer while counting in Auto Reload mode, the actual sequence will be terminated normally. At the start of the next cycle, the new value is loaded into the counter and all following cycles are executed according to the new value loaded.
After setting "ARMode" to "0", the timer counts down to zero, generating an interrupt and stays then at zero. The Auto Reload Mode is only held by writing "0000" into the "Timer1 HI-Data" and the "Timer1Low-Data" reload registers.
The timer1 period in the Auto Reload Mode is (1+Load Value) * Clock Period, from interrupt to interrupt. The duration from CPU writes access to 1. Timer1 interrupt is LoadValue*Timer Clock Period - (0...1) Timer Clock Period
If an all-zero data is written into the reload register, no interrupt will be generated and the timer1 remains at this state until a non zero data is written into the reload register. Then, the described sequence starts again.
The "ARMode" and the "SynMode" can be combined: the two control bits "ARMode" and the "SynMode" (bits 2 and 3 of address H56) are set to "1". The timer 1 starts then synchronised by the 64Hz signal in Auto Reload Mode and ports P3, P4 and P72 (metal option OP21-A) are outputting data as described in 8.3, 8.4 and 8.7.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Timer1 Ctl	56	86	W R	SynMode SynMode	ARMode ARMode	SelT1F2 SelT1F2	SelT1F1 SelT1F1
Timer1 HI-Data	57	87	W R	MSB MSB	(hi nibble)		
Timer1 Low-Data	58	88	W R		(low nibble)		LSB LSB

10. Timer 2

The timer 2 can operate in two modes: The Zero Stop Mode as explained in timer1 description and the Auto Reload Mode. The clock frequency can be selected by "SelT2F2" and "SelT2F1" control bits in "Timer2 Ctl" at address H59:

SelT2F2	SelT2F1	Timer 2 Clock Frequency
0	0	4 Hz
0	1	16 Hz
1	0	64 Hz
1	1	256 Hz

The timer 2 has the same general structure as timer 1, see description there.

10.1 Zero Stop Mode

The operation in this mode is the same as for timer 1, only the CPU access address is H5A for "Timer2 Hi-Data", H5B for "Timer2 Low-Data" and H59 for "Timer2 Ctl".

10.2 Auto Reload Mode

This mode of timer2 is enabled, if the "ARMode", bit2 of "Timer2 Ctl", address H59 is set to "1".
The timer starts counting down, when a non-zero data is loaded into its 2 reload registers (address H5A, "Timer2 Hi-Data" and address H5B, "Timer2 Low-Data"). When the counter has arrived at zero state, a "Timer2" interrupt is generated (bit 3, address H64).
The counter is then automatically reload with the data stored in the reload register (previously written there by the CPU), and starts again to count down.
This sequence is repeated until the Auto Reload Mode is stopped by setting the "ARMode" bit to "0". The Auto Reload Mode is only hold by writing "0000" into the "Timer2 Hi-Data" and "Timer2 Low-Data" reload registers.
The timer 2 period in the Auto Reload Mode is the same as defined for timer1 in Auto Reload Mode, see there.
If an all-zero data is written into the 2 reload registers, no interrupt will be generated and the timer 2 remains at this state until a non-zero data is written into the 2 reload registers. Then, the described sequence starts again.

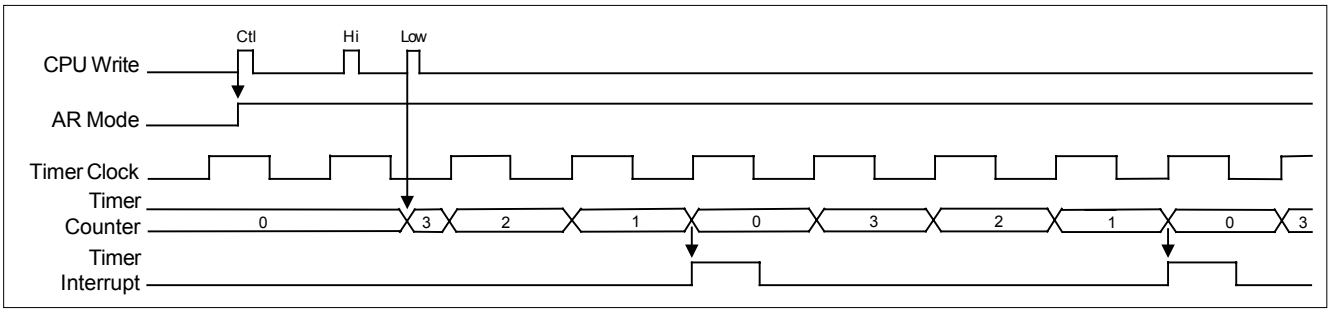


Fig.13: Timer 2 Timing in Auto Reload Mode

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Timer2 Ctl	59	89	W R	x 0	ARMode ARMode	SelT2F2 SelT2F2	SelT2F1 SelT2F1
Timer2 Hi-Data	5A	90	W R	MSB MSB	(hi nibble)		
Timer2 Low-Data	5B	91	W R		(low nibble)		LSB LSB

11. BCD counter/CHRONO

The EM6635 has an 8bits BCD counter or Chrono Block.
It contains a 100Hz generator, clocked from Prescaler, and a cascade of 2 BCD counters, which generate BCD-data for 1/100s and 1/10s digits.

The Chrono Block generates an interrupt BCD in register INT-Stat-4 (bit0, address H6A). The source of the interrupt is the 1/10s BCD counter overflow (transition from state “9” to “0”) or the corresponding transition of 1/100s BCD counter.
The mask bit BCD in register INT-Stat-4 can be reset by the CPU. A corresponding mask bit at high will enable the corresponding interrupt, a low level disables this interrupt (bit0, address H6B).

The CPU can start the chrono function by setting BCDRun in “BCDCtl” to high level (bit0, address H5C). This enables the 100Hz chrono clock and the BCD counters.
The CPU can stop the chrono counter by resetting this BCDRun to low level. By this, the clock of the counters is stopped, but the state of the counters is maintained, e.g. to be read later.
The CPU can reset the BCD counters by writing high to BCDRes in “BCD Ctl” (bit1, address H5C), independently of the actual mode of the BCD counters (counting or stopped).
The BCDRes is automatically reset after it has cleared the counters; a read access gives always a low level.
The CPU can read the state of the BCD counters in register BCD 1/100 while the counters are counting or when stopped. The 4bits of “BCD 1/100” register represent the 1/100s digit data and the 4 bits of “BCD 1/10” register represent the 1/10s digit data in BCD format.
The MSB’s of this data are at bit3 of “BCD 1/100” register (address H5D), respectively at bit3 of “ BCD 1/10” (address H5E).
The CPU can select an event each 100ms by setting this BCDEvent to high level in “BCD Ctl” (bit2, address H5C) or each second BCDEvent to low level.
The Chrono Block generates a carry flag when the counter changes from 99 to 00. The CPU can read the flag in register “BCD Ctl” (bit3, address H6B). State “1” indicates an increment of 1s. State “0” indicates no increment. When “1” is written, the BCDCarry is cleared. When “0” is written, no change occurs.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
BCD Ctl	5C	92	W R	BCDCarry BCDCarry	BCDEvent BCDEvent	BCDRes 0	BCDRun BCDRun
BCD 1/100	5D	93	- R	MSB <---------- BCD 1/100 ----------> LSB			
BCD 1/10	5E	94	- R	MSB <---------- BCD 1/10 ----------> LSB			

12. Event Counter

The EM6635 has a 3bits event counter, capable to count the "M" pulses, which are generated by input port P1 (see description of port P1). The counting direction is upwards. When the event counter arrives at "111" (= decimal 7), it stops counting and remains at this state.
The state of the event counter can be read by the CPU at any time by reading "Event Counter" at address H60, bits 2, 1 and 0; The bit3 is always read as "0".
A write access to this address H60 clears the event counter to "000", independent of the data value written.
After a system reset, the event counter is in state "000".

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
Event Counter	60	92	W R	0	(Clear Counter) MSB		LSB

13. Buzzer Output / Frequency Generator

The EM6635 is equipped with a buzzer output, which can drive a piezo buzzer via an external NPN transistor. An envelop control terminal allows to create a decay shape of the buzzer output signal.
The buzzer output is driven by a frequency generator, which consists of an 8bits programmable divider. The output signal has always a duty cycle of 50%. The input clock frequency of the programmable divider is the doubled system clock, i.e. 65536 Hz (with 32768Hz crystal). The settling time after the activation of the cell is typically 500us.

13.1 Functional Description

By system reset, "EnFGen" and "EnEnvelop" and the programmable divider data are cleared to zero.
The 8bits programmable divider and the buzzer output are enabled together by "EnFGen" set to "1" in "FGen Ctl" at address H63, bit 0.
The CPU writes divider data in two steps, first the lower 4bits into "FGen Low-Data" (address H61) and then the higher 4bits into "FGen Hi-Data" (address H62).
This 8bits data word is stored in an internal synchronisation register and transferred into the programmable divider if a current output signal period has finished, or directly when no output is generated until then. This is the case, if the frequency generator is loaded with H00. (This is a possibility to program a pause or "silence" without disabling the generator with "EnFGen".)
The lower 4bits have to be written first, because the write access to the higher 4bits (to "FGen Hi-Data") enables also the transfer of the 8bits data from the internal synchronisation register into the programmable divider.
The generated output frequency is CK / (data + 1) with CK = 65536Hz.
The frequency doubler is switched on with EnFGen of FGen Ctl at address H63, bit 0.
The divider range is from 2 to 256. As mentioned above, a H00 data produces no output frequency.

13.2 Envelop Control

An external capacitor CENV must be connected to the pad CENV to implement the envelop function.
The envelop function is activated by setting "EnEnvelop" to "1" (bit 1, address H63).
When set to "1", the capacitor starts to be charged from VSS to VBAT level.
The CENV terminal voltage controls an internal amplitude attenuator at the BZ output in such a way, that the BZ level is maximum (full swing) when CENV is at VSS level and at minimum (no output signal) when at VBAT level.
The attenuator response is non-linear. Therefore, after setting "EnEnvelop" to "1", a delay time tDDEC without attenuation is followed by the real decay time tDEC, during which the output amplitude is modulated to decay to zero.
(if CENV=330nF, tDDEC may be 5…30ms, tDEC may be 20…60ms, depending on external circuitry)
The capacitor CENV can be loaded with two different speeds. Bit 2 of FGen Ctl, "SelShort", if set to "1", selects the faster charge of capacitor CENV.
The impedance of the externally connected circuit at BZ output has an influence on the decay time tDEC. A lower impedance makes a longer decay time tDEC.
The generation of an output tone with envelop control is completely under SW control, with support of a timer 2 function. A possible sequence is shown in Fig.14:

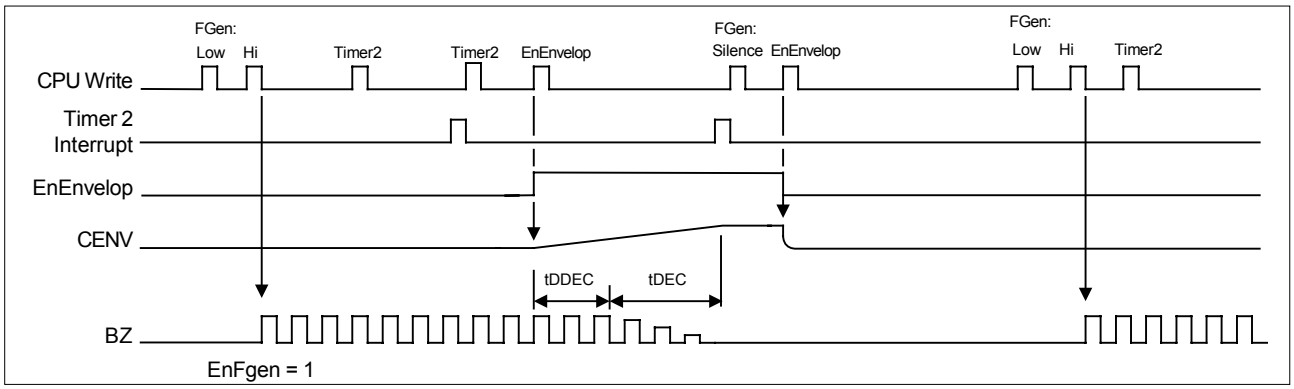


Fig.14: Example of BZ Output Tone Generation with Envelop Control

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
FGen Low-Data	61	97	W R		(low nibble)		LSB LSB
FGen Hi-Data	62	98	W R	MSB MSB	(high nibble)		
FGen Ctl	63	99	W R	x 0	SelShort SelShort	EnEnvelop EnEnvelop	EnFGen EnFGen

14. Supply Voltage Level Detector

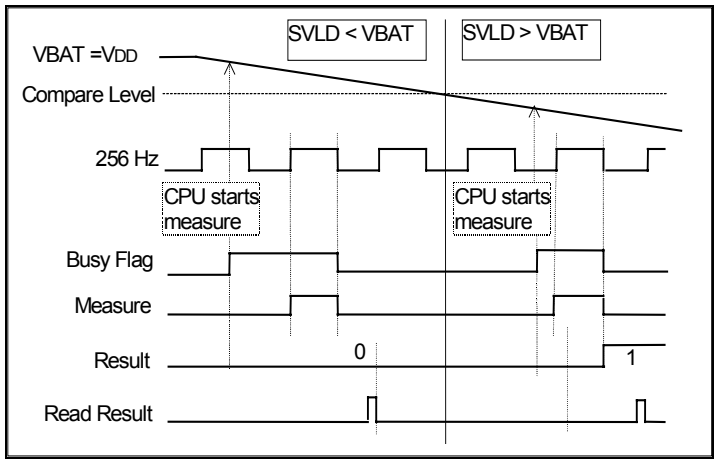
The EM6635 has a software configurable built-in Supply Voltage Level Detector (SVLD). Three levels can be defined between V_{DD}min+100mV and V_{DD}max-600mV.
The CPU can compare the supply voltage against a pre-selected value by writing the 2 bits **VLC0** and **VLC1** in the **SVLD** control register which also activates the compare measurement. Since the measurement is not immediate the busy flag remains high during the measurement and is automatically cleared low when the measurement is finished.

The actual measurement starts with the rising 256Hz edge following the SVLD command.
During the actual measurement (2 ms) the device will draw an additional 5 µA of IV_{DD} current. After the end of the measures the result is available by inspection of the bit **VldResult**.
If the result is read 0, then the power supply voltage was greater than the detection level value. If read 1, the power supply voltage was lower than the detection level value. During each read while **VldBusy=1** the **VldResult** is not guaranteed.

SVLD level selection

Evaluation voltage	VLC1	VLC0
not active	0	0
VL1	0	1
VL2	1	0
VL3	1	1

SVLD Timing Diagram



CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
SVLD	6C	108	W R	 VldResult	 VldBusy*	VLC1 VLC1	VLC0 VLC0

VldBusy*; Read value of VldResult is not guaranteed while VldBusy=1.

15. Interrupt Control

The EM6635 interrupt controller can handle 16 interrupt requests: 10 internal and 6 external.
The controller is organized in four 4bits parts: "INT-Stat1' to "INT-Stat4" and the corresponding mask control "INT-Msk1" to "INT-Msk4".
The assignment of the individual interrupt requests is shown in the CPU Access Format. ("INT-Stat4" and "INT-Msk4" contain really only hardware for 3 used interrupt requests, the BCD counter, the P6 interrupt and the P7 interrupt.

15.1 Functional Description

A positive edge of an interrupt source signal sets the corresponding status bit in the interrupt controller. All status flags are logically combined as "OR" to generate the CPU main interrupt request.
The status flags are readable to the CPU and can be cleared individually by writing "1" to the corresponding bit of "INT-Stat". The status flags are automatically reset by the read access.
After a system reset, all flags are at "0".
The CPU main interrupt request can be disabled by DisINT in "HW-Ctl-1" (bit1, address H40 or H41), when this bit is set to "1".
All interrupt requests can be masked by the "INT-Msk" register.
A "0" level at an interrupt mask bit inhibits the propagation of an interrupt request to the interrupt status register, so that the corresponding interrupt status bit is not set.
If a mask bit is set to "1" when the interrupt source signal is "1", the corresponding status bit will not be set.
Only a positive edge of an interrupt source can set the interrupt status.
If DisINT (bit 1, address H40 or H41) is reset to "0" (CPU main interrupt enabled) when an interrupt status bit is "1", a CPU interrupt will be generated.

CPU Access Format:

Register	Add Hex	Add Dec		bit3	bit2	bit1	bit0
HW-Ctl-1	40 (41)	64 (65)	W	x	SelINH	DisINT	x
INT-Stat1	64	100	W R	Clear Timer2	Clear Timer1	Clear INT-TB2	Clear INT-TB1
INT-Msk1	65	101	W R	Timer2 Timer2	Timer1 Timer1	INT-TB2 INT-TB2	INT-TB1 INT-TB1
INT-Stat2	66	102	W R	0 x	Clear M	Clear P13	Clear P12
INT-Msk2	67	103	W R	0 x	M M	P13 P13	P12 P12
INT-Stat3	68	104	W R	Clear INT_TB4	Clear INT_TB3	Clear INT-P2	Clear INT-SIO
INT-Msk3	69	105	W R	INT_TB4 INT_TB4	INT_TB3 INT_TB3	INT-P2 INT-P2	INT-SIO INT-SIO
INT-Stat4	6A	106	W R	X 0	Clear INT-P7	Clear INT-P6	Clear BCD
INT-Msk4	6B	107	W R	X 0	INT-P7 INT-P7	INT-P6 INT-P6	BCD BCD

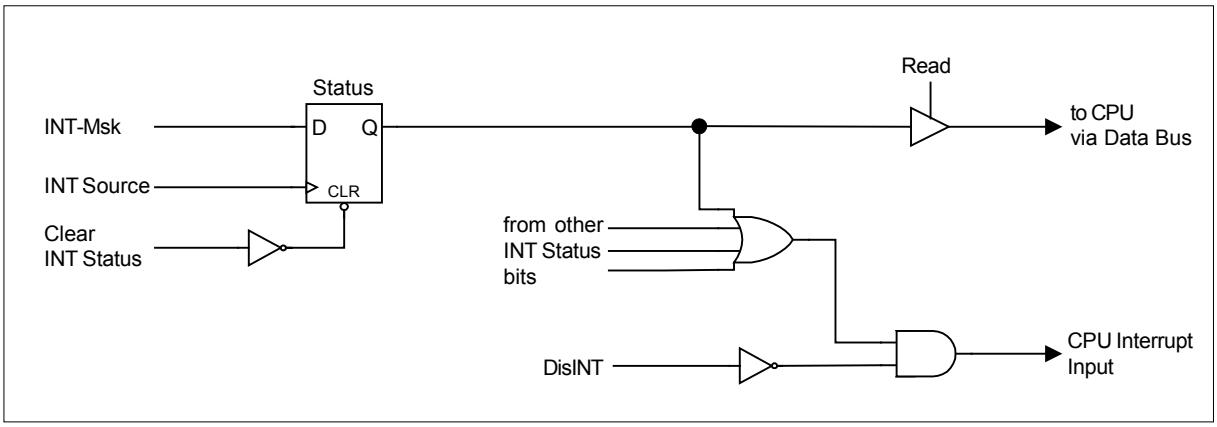


Fig.15: Interrupt Controller Principle

16. Peripheral Memory Map

Function	Add Hex	Add Dec		Init.	Bit 3	Bit 2	Bit 1	Bit 0
				b'3210				
RAM0,1,2,3	00…3F	0…63	R W	xxxx	Data3 Data3	Data2 Data2	Data1 Data1	Data0 Data0
HW-Ctl-1	40	64	R W	0000	0 x	0 x	DisINT DisINT	0 x
HW-Ctl-1 Bit Access	41	65	R W	0000	0 Set: 1/Clear: 0	0 x	DisINT DisINT	0 Reset WD
HW-Ctl-2	42	66	R W	0000	SelTBCapHi SelTBCapHi	0 x	0 x	0 x
HW-Ctl-2 Bit Access	43	67	R W	0000	SelTBCapHi Set: 1/Clear: 0	0 x	0 x	0 Reset CK
Config-1	44	68	R W	0000	Mot3Mode Mot3Mode	DisWD DisWD	EnFOut EnFOut	SelINT8 SelINT8
Config-2	45	69	R W	0000	DisInpRes DisInpRes	P5DebOn P5DebOn	P2DebOn P2DebOn	P1DebOn P1DebOn
Config-3	46	70	R W	0000	0 x	0 x	P7DebOn P7DebOn	P6DebOn P6DebOn
Port P1	47	71	R -	0000	P13	P12	P11	P10
Port P2	48	72	R -	0000	P23	P22	P21	P20
Special Data	49	73	R W	0000	0 x	0 x	0 x	0 x
Port P6 (if NO INH-Low)	4A	74	R W	0000	P63 P63	P62 P62	P61 P61	P60 P60
Port P7 (if NO INH-Hi) (if INH_Hi, only P72)	4B	75	R W	0000	0 x	P72 P72	P71 P71	P70 P70
PIO67 Ctl	4C	76	R W	0000	P72-Dir P72-Dir	P701-Dir P701-Dir	P623-Dir P623-Dir	P601-Dir P601-Dir
Port P3	50	80	R W	0000	P33 P33	P32 P32	P31 P31	P30 P30
Port P4	51	81	R W	0000	P43 P43	P42 P42	P41 P41	P40 P40
PIO43 Ctl	52	82	R W	0000	P43-Dir P43-Dir	P33-Dir P33-Dir	P4-Dir P4-Dir	P3-Dir P3-Dir
Port P5	53	83	R W	0000	P53 P53	P52 P52	P51 P51	P50 P50
as Serial IO:					SCK	SOUT	RDY	SIN
PIO5 Ctl	54	84	R W	0000	P53-Dir P53-Dir	P52-Dir P52-Dir	P51-Dir P51-Dir	P50-Dir P50-Dir
TB Capture	55	85	R -	1000	T1 (T16)	T2 (T32)	T4 (T64)	T8 (T128)
Timer1 Ctl (Mot)	56	86	R W	0000	SynMode SynMode	ARMode ARMode	SelT1F2 SelT1F2	SelT1F1 SelT1F1
Timer1 Hi-Data	57	87	R W	0000	MSB <---------- Timer 1 Data, Hi Nibble ----------> LSB MSB <---------- Timer 1 Data, Hi Nibble ----------> LSB			
Timer1 Low-Data	58	88	R W	0000	MSB <---------- Timer 1 Data, Low Nibble ----------> LSB MSB <---------- Timer 1 Data, Low Nibble ----------> LSB			
Timer2 Ctl (Buzzer)	59	89	R W	0000	0 x	ARMode ARMode	SelT2F2 SelT2F2	SelT2F1 SelT2F1
Timer2 Hi-Data	5A	90	R W	0000	MSB <---------- Timer 2 Data, Hi Nibble ----------> LSB MSB <---------- Timer 2 Data, Hi Nibble ----------> LSB			
Timer2 Low-Data	5B	91	R W	0000	MSB <---------- Timer 2 Data, Low Nibble ----------> LSB MSB <---------- Timer 2 Data, Low Nibble ----------> LSB			

Function	Add Hex	Add Dec		Init.	Bit 3	Bit 2	Bit 1	Bit 0
				b'3210				
BCD Ctl	5C	92	R W	0000	BCDCarry BCDCarry	BCDEvent BCDEvent	0 BCDRes	BCDRun BCDRun
BCD 1/100	5D	93	R -	0000	MSB <---------- BCD 1/100 ----------> LSB			
BCD 1/10	5E	94	R -	0000	MSB <---------- BCD 1/10 ----------> LSB			
Event Counter	60	96	R W	0000	0 MSB <------- Ev Counter Data ----------> LSB <---------- Write Access: Clear Event Counter ----------> LSB			
FGen Low-Data	61	97	R W	0000	MSB <---------- FGen Data, Low Nibble ----------> LSB MSB <---------- FGen Data, Low Nibble ----------> LSB			
FGen Hi-Data	62	98	R W	0000	MSB <---------- FGen Data, Hi Nibble ----------> LSB MSB <---------- FGen Data, Hi Nibble ----------> LSB			
FGen Ctl	63	99	R W	0000	0 x	SelShort SelShort	EnEnvelop EnEnvelop	EnFGen EnFGen
INT-Stat-1	64	100	R W	0000	Timer2 Clear	Timer1 Clear	INT_TB2 Clear	INT_TB1 Clear
INT-Msk-1	65	101	R W	0000	Timer2 Timer2	Timer1 Timer1	INT_TB2 INT_TB2	INT_TB1 INT_TB1
INT-Stat-2	66	102	R W	0000	0 x	M Clear	P13 Clear	P12 Clear
INT-Msk-2	67	103	R W	0000	0 x	M M	P13 P13	P12 P12
INT-Stat-3	68	104	R W	0000	INT_TB4 Clear	INT_TB3 Clear	INT_P2 Clear	INT-SIO Clear
INT-Msk-3	69	105	R W	0000	INT_TB4 INT_TB4	INT_TB3 INT_TB3	INT_P2 INT_P2	INT-SIO INT-SIO
INT-Stat-4	6A	106	R W	0000	0 x	INT_P7 Clear	INT_P6 Clear	BCD Clear
INT-Msk-4	6B	107	R W	0000	0 x	INT_P7 INT_P7	INT_P6 INT_P6	BCD BCD
SVLD	6C	108	R W	0000	RESULT x	BUSY x	VLC1 VLC1	VLC0 VLC0
RCOSC	6D	109	R W	(Note1)	0 x	ColdStart x	En RC En RC	Osc switch Osc switch
Index Low	6E	110	R W	xxxx	IXLow[3] IXLow[3]	IXLow[2] IXLow[2]	IXLow[1] IXLow[1]	IXLow[0] IXLow[0]
Index Hi	6F	111	R W	xxxx	0 x	IXHi[2] IXHi[2]	IXHi[1] IXHi[1]	IXHi[0] IXHi[0]
SIO Low-Data	70	112	R W	0000	MSB of Low Nibble <----------> LSB of Low Nibble MSB of Low Nibble <----------> LSB of Low Nibble			
SIO Hi-Data	71	113	R W	0000	MSB of Hi Nibble <----------> LSB of Hi Nibble MSB of Hi Nibble <----------> LSB of Hi Nibble			
SIO Ctl1	72	114	R W	0000	SelSIOClk1 SelSIOClk1	SelSIOClk0 SelSIOClk0	SelWL1 SelWL1	SelWL0 SelWL0
SIO Ctl2	73	115	R W	0000	RUN RUN	NegEdg NegEdg	EnSIO EnSIO	SelSynOut SelSynOut
SIO Ctl3	74	116	R W	0000	RDYactive RDYactive	RDYisOutput RDYisOutput	SelRDYPol1 SelRDYPol1	SelRDYPol0 SelRDYPol0
RAM Index	77	119	R W	0000	0, 1 0, 1	0, 1 0, 1	PageSel[1] PageSel[1]	PageSel[0] PageSel[0]
Backlit	78	120	R W	0000	Blout Blout	StartBL StartBL	ELPcksel ELPcksel	ELCcksel ELCcksel

Add 75, 76, 7E and 7F are used for EM test.

Note 1: the initialisation of the "RCOSC" register is depending on metal option (see chapter 6.2)

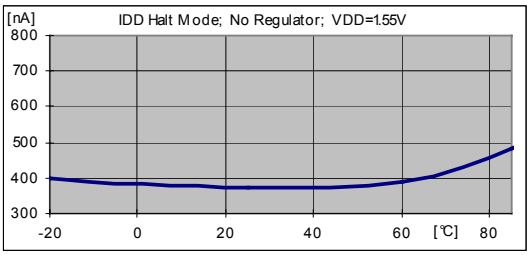
17. Mask Options of EM6635

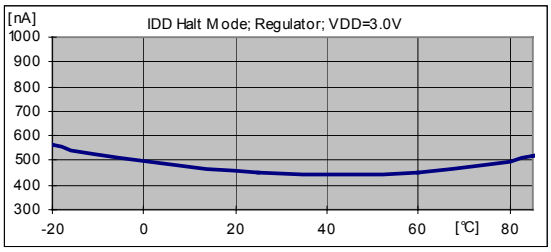
Option	Function	Select option
OP-1	A: Watchdog timer available B: no watchdog timer	
OP-2	A: 1s Cold Start Delay B: 0.75s Cold Start Delay C: 0.5s Cold Start Delay D: 0.25s Cold Start Delay E: no Cold Start Delay	
OP-3	A: POR available B: no POR	
OP-4	A: For EM only B: For EM only	
OP-5	A: For EM only B: For EM only	
OP-6	A: 31us Port P1 and P2 active Pulldown Time B: 62us Port P1 and P2 active Pulldown Time	
OP-7	A: Port P1 Pulldown is clocked B: no Port P1 Pulldown	
OP-8	A: 1024 Hz Fout Frequency when SIO in Slave Mode B: 512 Hz Fout Frequency when SIO in Slave Mode C: 128 Hz Fout Frequency when SIO in Slave Mode D: 32 Hz Fout Frequency when SIO in Slave Mode	
OP-9	A: Watchdog disabled by P22 AND P23 B: Watchdog independant of P22 AND P23	
OP-10	A: no Pull Down / Up at P50 = SIN B: Pull Up at P50 = SIN C: Pull Down at P50 = SIN (**obligatory** if OP-20 C is selected)	
OP-11	A: no Pull Down / Up at P51 = RDY B: Pull Up at P51 = RDY C: Pull Down at P51 = RDY	
OP-12	A: no Pull Down / Up at P52 = SOUT B: Pull Up at P52 = SOUT C: Pull Down at P52 = SOUT	
OP-13	A: no Pull Down / Up at P53 = SCK B: Pull Up at P53 = SCK C: Pull Down at P53 = SCK	
OP-14	A: Port 2: Pulldown is clocked B: Port 2: no Pulldown	
OP-15	A: Port P6 & P70, P71: Pulldown is clocked B: Port P6 & P70, P71: no clocked Pulldown	
OP-16	A: Voltage regulator is active B: no voltage regulator (VBAT = VRR)	
OP-17	A: Buzzer envelop control is enabled B: Buzzer envelop control is disabled	
OP-18	A: CPU controlled P33 function (with EnFOut) B: P33 is always FOut	
OP-19	A: Xtal Oscillator and RC Oscillator B: External clock and RC Oscillator	
OP-20	A: RC Oscillator active at system reset B: RC Oscillator not active at system reset C: Set P50 to high activate RC Oscillator at system reset	
OP-21	A: P72 output is High drive buffer for motor (Timer1) B: P72 output is 5mA (PMOS, LED connected to VSS) C: P72 output is 5mA (NMOS, LED connected to VDD) D: P72 output is High drive I/O	
OP-22	A: For EM only B: 4 I/O port 6	
OP-23	A: For EM only B: 2 I/O port P70 and P71	
OP-24	A: no Pull Down / Up at P60 B: Pull Up at P60 C: Pull Down at P60 D: For EM only	
OP-25	A: no Pull Down / Up at P61 B: Pull Up at P61 C: Pull Down at P61 D: For EM only	
OP-26	A: no Pull Down / Up at P62 B: Pull Up at P62 C: Pull Down at P62 D: For EM only	
OP-27	A: no Pull Down / Up at P63 B: Pull Up at P63 C: Pull Down at P63 D: For EM only	
OP-28	A: no Pull Down / Up at P70 B: Pull Up at P70 C: Pull Down at P70 D: For EM only	
OP-29	A: no Pull Down / Up at P71 B: Pull Up at P71 C: Pull Down at P71 D: For EM only	

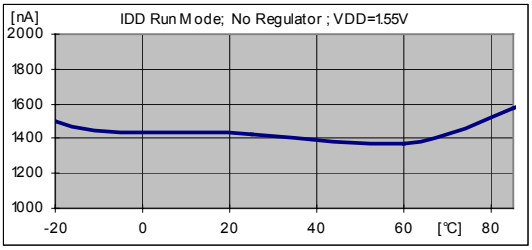
To select an option put a letter A, B, C, D or E in column **Select Option.**

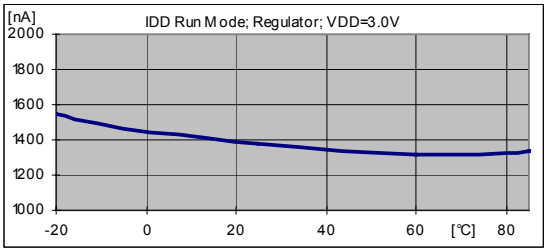
18. Temperature and Voltage Behaviors

18.1 IDD Current (Typical)

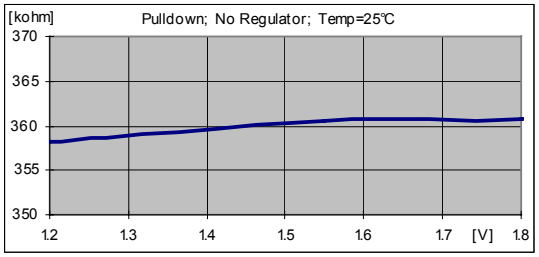


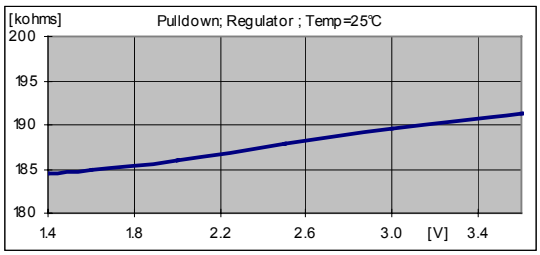


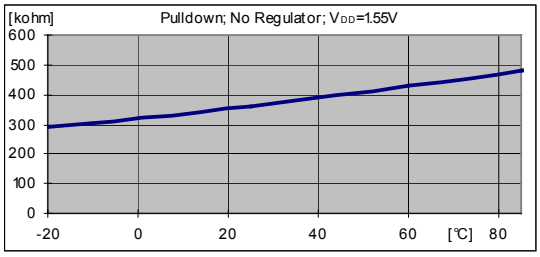


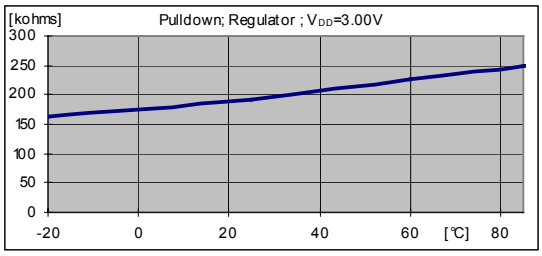


18.2 Pull-down Resistance (Typical)



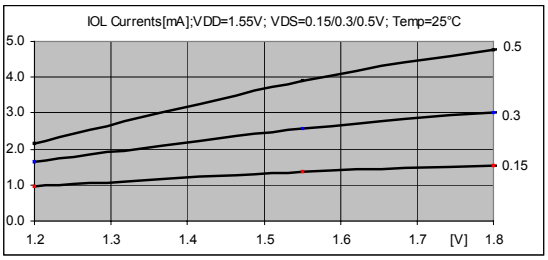


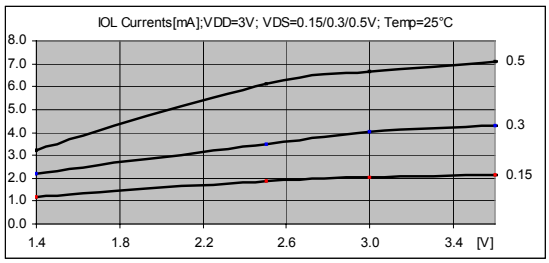


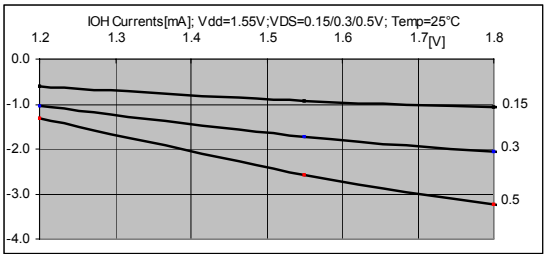


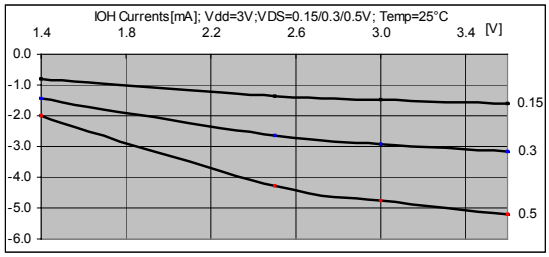
18.3 Output Currents (Typical)

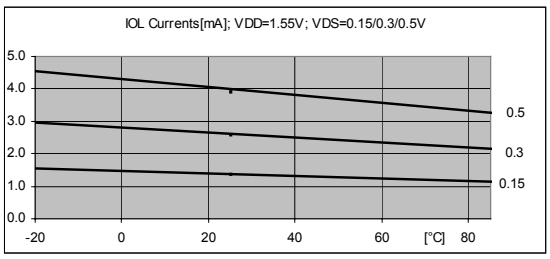
18.3.1 Port P5, P6, P70, P71 & P72 (OP-21B), Reset OUT

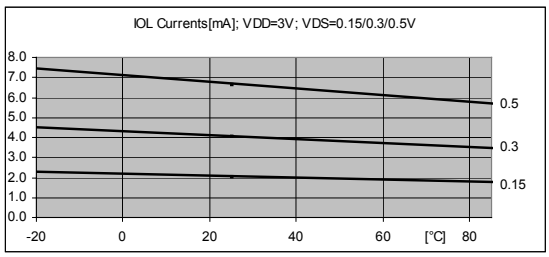


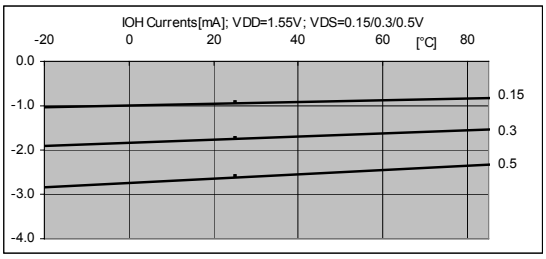


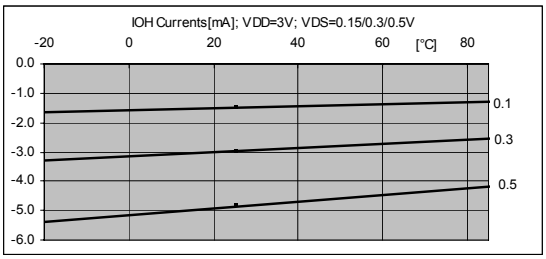




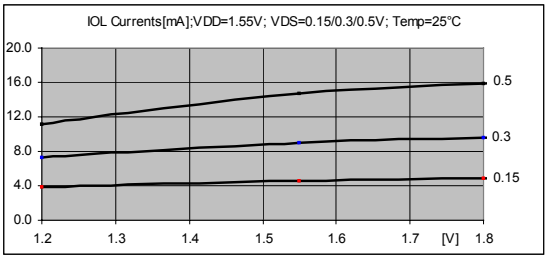


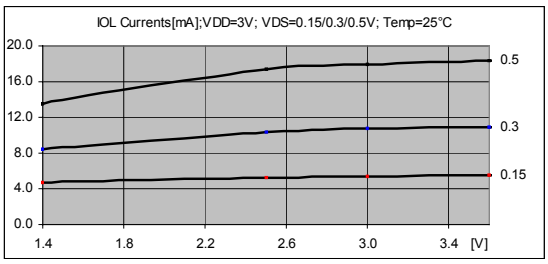


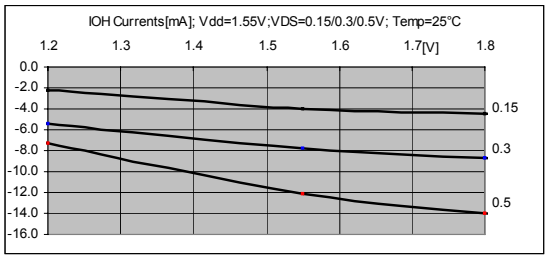


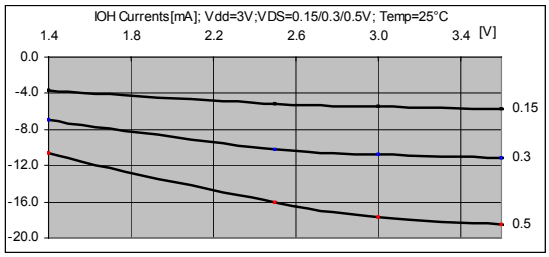


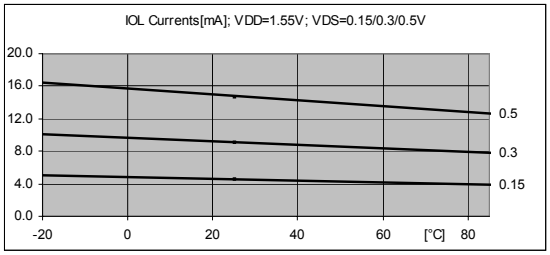
18.3.2 Port P3, P4 & P72 (OP-21A)

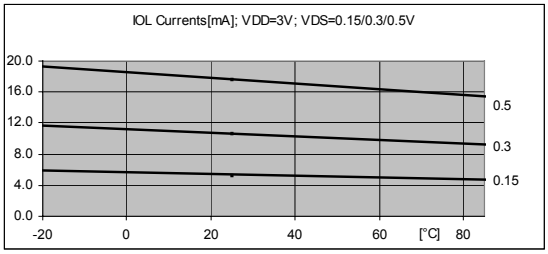


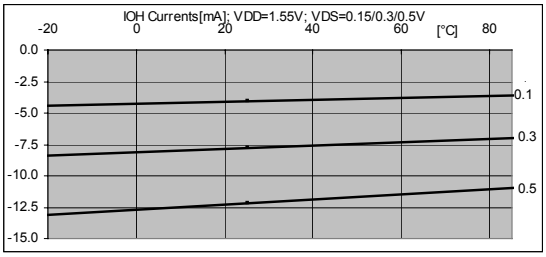


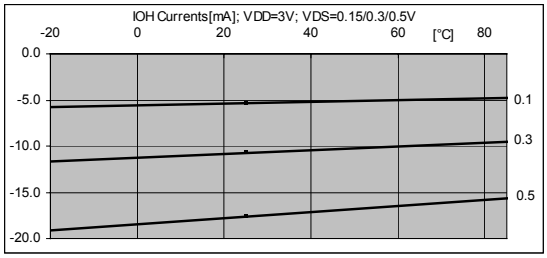












19. Electrical Specifications

19.1 Absolute maximum Ratings

	Min.	Max.	Unit
Power supply V_{DD}-V_{SS}	-0.2	+3.6	V
Input Voltage	V_{SS} -0.2	V_{DD} +0.2	V
Storage Temperature	-40	+125	°C
Electrostatic discharge to Mil-Std-883C method 3015.7 with ref. to V_{SS}	-2000	+2000	V
Maximum soldering conditions		10s x 250°C	

Stresses above these maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

19.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified, correct operation can only occur when all terminal voltages are kept within the supply voltage range.

19.3 Standard Operating Conditions

Parameter	MIN	TYP	MAX	Unit	Description
Temperature	-20	25	85	°C	
V_{DD} _Range1	1.6	3.0	3.6	V	with internal voltage regulator
V_{DD} _Range2	1.2	1.5	1.8	V	without internal voltage regulator
IV_{SS} max			300	mA	Maximum current out of V_{SS} Pin
IV_{DD} max			300	mA	Maximum current into V_{DD} Pin
V_{SS}		0		V	Reference terminal
CV_{RR} (Note2)	100			nF	regulated voltage capacitor
f_Q		32768		Hz	nominal frequency
R_{QS}		35		kOhm	typical quartz serial resistance
C_L		8.2		pF	typical quartz load capacitance
df/f		± 30		ppm	quartz frequency tolerance

Note 2: This capacitor filters switching noise from V_{DD} to keep it away from the internal logic cells. In noisy systems the capacitor should be chosen bigger than minimum value.

19.4 DC Characteristics - Power Supply

Conditions: V_{DD} =1.55V, T=+25°C, without internal voltage regulator (unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
ACTIVE supply current	(Note3,4) -20°C to +85°C (Note3,4)	IV_{DDA}		1.5	2.5 3.5	µA
ACTIVE supply current	at 250kHz (Note4) at 250kHz, -20°C to +85°C (Note4)	IV_{DDA2}		29	45 60	µA
HALT supply current	(Note3) -20°C to +85°C (Note3)	IV_{DDH}		0.4	0.8 1.0	µA
POR static level		V_{POR}	0.7	1.01	1.2	V
RAM data retention		V_{RD1}	1.0			V

Note 3: Active and standby current measurements are made with oscillator driven by an external square wave signal of 32.768kHz and an amplitude of V_{DD} voltage.
Note 4: For well defined current measurement, a special test-loop is installed in SW with successive write and read of two addresses. For this, 5 instructions must be reserved in the ROM code. This will be done at EM Microelectronic-Marin.

Conditions: V_{DD} =3.00V, T=+25°C, with internal voltage regulator (unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
ACTIVE supply current	(Note3,4) -20°C to +85°C (Note3,4)	IV_{DDA}		1.6	2.6 3.6	µA
ACTIVE supply current	at 500kHz (Note4) at 500kHz, -20°C to +85°C (Note4)	IV_{DDA2}		50	75 100	µA
HALT supply current	(Note3) -20°C to +85°C (Note3)	IV_{DDH}		0.4	0.8 1.0	µA
POR static level		V_{POR}	0.75	1.04	1.25	V
RAM data retention	-20°C to +85°C	V_{RD2}	1.2			V
Regulated voltage	Halt mode, no load	V_{REG}	1.2	1.4	1.7	V

Note 3: Active and standby current measurements are made with oscillator driven by an external square wave signal of 32.768kHz and an amplitude of V_{REG} voltage.

Note 4: For well defined current measurement, a special test-loop is installed in SW with successive write and read of two addresses. For this, 5 instructions must be reserved at the end of the ROM. This will be done at EM Microelectronic-Marin.

```
TESTLOOP:   STI     00H,    0AH     ;TEST LOOP
            LDR     1BH
            NXORX   FFH
            JPZ     TESTLOOP
            JMP     0
```

To stay in the testloop, these values must be written in the corresponding addresses before jumping in the loop. This is done at EM Microelectronic-Marin.

```
1BH:  0101b
32H:  1010b
6EH:  0010b
6FH:  0011b
```

Free space after last instruction: JMP 00H (0000)

Remark: empty space within the program are filled with NOP (FOFF).

19.5 Oscillator

Conditions: T=+25°C, (unless otherwise specified), 32kHz oscillator

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Temperature Stability	+15°C to +35°C	df/f x dT			0.3	ppm/°C
Voltage Stability (note 5)	V_{DD} = 1.4 to 1.6V	df/f x dU			5	ppm /V
Input Capacitor	Ref. on V_{SS}	C_{IN}	5.8	7	8.2	pF
Output Capacitor	Ref. on V_{SS}	C_{OUT}	10.7	12.5	14.3	pF
Transconductance	V_{Ddmin}, sinus 50mVpp	gm	2.5		15	µA/V
Oscillator start voltage	T_{START} < 10s	V_{START}	V_{DDmin}			V
Oscillator start time	V_{DD} = 1.55V	T_{START}			2	sec

Note5: Applicable only for the versions without the internal voltage regulator

Conditions: V_{DD} =1.55V, T=+25°C, (unless otherwise specified), 250kHz RC-Oscillator

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency		f_{RC}	-30%	250	+30%	kHz
Oscillation start voltage	T_{START} < 1ms	$V_{RCSTART}$	1.2			V
Oscillation start time					1	ms
Oscillation stop voltage				0.9		V

Conditions: V_{DD} =3.00V, T=+25°C, (unless otherwise specified), 500kHz RC-Oscillator

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency		f_{RC}	-30%	500	+30%	kHz
Oscillation start voltage	T_{START} < 1ms	$V_{RCSTART}$	1.4			V
Oscillation start time					1	ms
Oscillation stop voltage				1.1		V

External clock on Qout terminal (metal option OP-19 B)

Conditions: T=+25°C, (unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
External frequency				32.768	650	kHz
Pulldown active	V_{IN}=V_{DD}=3.00V	I_{PD}	2		8	µA
Pulldown active	V_{IN} =V_{DD}=1.55V	I_{PD}	0.5		2	µA

19.6 Supply Voltage Level Detector

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
	V_{DD} = 1.55V					
SVLD voltage Level1	mask option, -10 to +60°C	V_{SVLD1}	1.24	1.38	1.52	V
	V_{DD} = 3.00V					
SVLD voltage Level1	mask option, -10 to +60°C	V_{SVLD1}	2.55	2.80	3.05	V
SVLD voltage Level2	mask option, -10 to +60°C	V_{SVLD2}	2.28	2.50	2.72	V
SVLD voltage Level3	mask option, -10 to +60°C	V_{SVLD3}	1.46	1.60	1.74	V
Temperature coefficient	0 to +50°C			< ±0.1		mV/°C

19.7 DC Characteristics Input / Output

Conditions: -20°C to +85°C (unless otherwise specified)

V_{DD} =1.55V means; measures without voltage regulator, V_{DD} =3.00V means; measures with voltage regulator

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Input Low Voltage	Port in Input Mode					
Port P1, P2, P3, P4, P5		V_{IL}	V_{SS}		$0.2V_{DD}$	V
P6 & P70, P71		V_{IL}	V_{SS}		$0.2V_{DD}$	V
RESETIN		V_{IL}	V_{SS}		$0.1V_{DD}$	V
QIN with Regulator		V_{IL}	V_{SS}		$0.1V_{REG}$	V
QIN without Regulator		V_{IL}	V_{SS}		$0.1V_{DD}$	V
QOUT (note 6) (OP-19A)						
Input High Voltage	Port in Input Mode					
Port P1, P2, P3, P4, P5		V_{IH}	$0.8V_{DD}$		V_{DD}	V
P6 & P70, P71		V_{IH}	$0.8V_{DD}$		V_{DD}	V
RESETIN		V_{IH}	$0.9V_{DD}$		V_{DD}	V
QIN with Regulator		V_{IH}	$0.9V_{REG}$		V_{REG}	V
QIN without Regulator		V_{IH}	$0.9V_{DD}$		V_{DD}	V
QOUT (note 6) (OP-19A)						
Input Current	**V_{DD} = 1.55V**					
P1, P2	Pull Down activated, 25°C	I_{PD}	0.5		2	µA
P5 Rpull=330k,metal option (note 7)	if Pull Down, V_{IN} = V_{DD}, 25°C if Pull Up, V_{IN} = V_{SS}, 25°C	I_{PD} I_{PU}	2 -10		10 -2	µA µA
P6 & P7 (OP-22B) Rpull=330k,metal option (note 7)	if Pull Down, V_{IN} = V_{DD}, 25°C if Pull Up, V_{IN} = V_{SS}, 25°C	I_{PD} I_{PU}	2 -10		10 -2	µA µA
RESETIN (Rpulldown=20k)	V_{IN} = V_{DD}, 25°C			75		µA
TEST, TCK, TESTRC	V_{IN} = V_{DD}, 25°C			340		µA
Cold Start Pull Down Input Current P1 to P5	Reset Out is active, 25°C	I_{PD}		0.5	1	mA
Input Current	**V_{DD} = 3.00V**					
P1, P2	Pull Down activated, 25°C	I_{PD}	2		8	µA
P5 Rpull=160k,metal option (note 7)	if Pull Down, V_{IN} = V_{DD}, 25°C if Pull Up, V_{IN} = V_{SS}, 25°C	I_{PD} I_{PU}	8 -40		40 -8	µA µA
P6 & P7 (OP-22B) Rpull=160k,metal option (note 7)	if Pull Down, V_{IN} = V_{DD}, 25°C if Pull Up, V_{IN} = V_{SS}, 25°C	I_{PD} I_{PU}	8 -40		40 -8	µA µA
RESETIN (Rpulldown=20k)	V_{IN} = V_{DD}			150		µA
TEST, TCK, TESTRC	V_{IN} = V_{DD}			340		µA
Cold Start Pull Down Input Current P1 to P5	Reset Out is active, 25°C	I_{PD}		0.5	1.5	mA
Output Low Current	**V_{DD} = 1.55V**					
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.08V	I_{OL}		-2.4	-1.0	mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.15V	I_{OL}		-4.5		mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.3V	I_{OL}		-9		mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.5V	I_{OL}		-14		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.15V	I_{OL}		-1.3		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.3V	I_{OL}		-2.5		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.5V	I_{OL}		-3.8		mA
BZ	V_{OL} = 0.15V	I_{OL}		-140	-75	µA

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Output Low Current	**V_{DD} =3.00V**					
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.08V	I_{OL}		-2.8	-1.0	mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.15V	I_{OL}		-5		mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.3V	I_{OL}		-10		mA
Ports P3, P4, P72(OP-21 A, D)	V_{OL} = 0.5V	I_{OL}		-17		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.15V	I_{OL}		-2		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.3V	I_{OL}		-4		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OL} = 0.5V	I_{OL}		-6.5		mA
BZ	V_{OL} = 0.15V	I_{OL}		200	-75	µA
Output High Current	**V_{DD} = 1.55V**					
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.12V	I_{OH}	1.0	3.3		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.15V	I_{OH}		4		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.3V	I_{OH}		7.7		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.5V	I_{OH}		12		mA
Port P5, P6 & P7(OP-22B) , ResetOut	V_{OH} = V_{DD}–0.15V	I_{OH}		0.9		mA
Port P5, P6 & P7(OP-22B) , ResetOut	V_{OH} = V_{DD}–0.3V	I_{OH}		1.7		mA
Port P5, P6 & P7(OP-22B) , ResetOut	V_{OH} = V_{DD}–0.5V	I_{OH}		2.5		mA
BZ	V_{OH} = V_{DD}–0.15V	I_{OH}	100	200		µA
Output High Current	**V_{DD} = 3.00V**					
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.12V	I_{OH}	1.0	4.2		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.15V	I_{OH}		5.3		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.3V	I_{OH}		10		mA
Ports P3, P4, P72(OP-21A, D)	V_{OH} = V_{DD}–0.5V	I_{OH}		17		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OH} = V_{DD}–0.15V	I_{OH}		1.45		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OH} = V_{DD}–0.3V	I_{OH}		2.9		mA
Port P5, P6 & P7(OP-22B), ResetOut	V_{OH} = V_{DD}–0.5V	I_{OH}	0.1	4.7		mA
BZ	V_{OH} = V_{DD}–0.15V	I_{OH}	100	250		µA
Output current	**V_{DD} = 2.40V**					
P72 (OP-21 C)	V_{OL} = 0.13V	I_{OL}		-8	-5	mA
P72 (OP-21 B)	V_{OH} = V_{DD}–0.15V	I_{OH}	5	9		mA

Note 6: QOUT (OSC2) is used only with Quartz

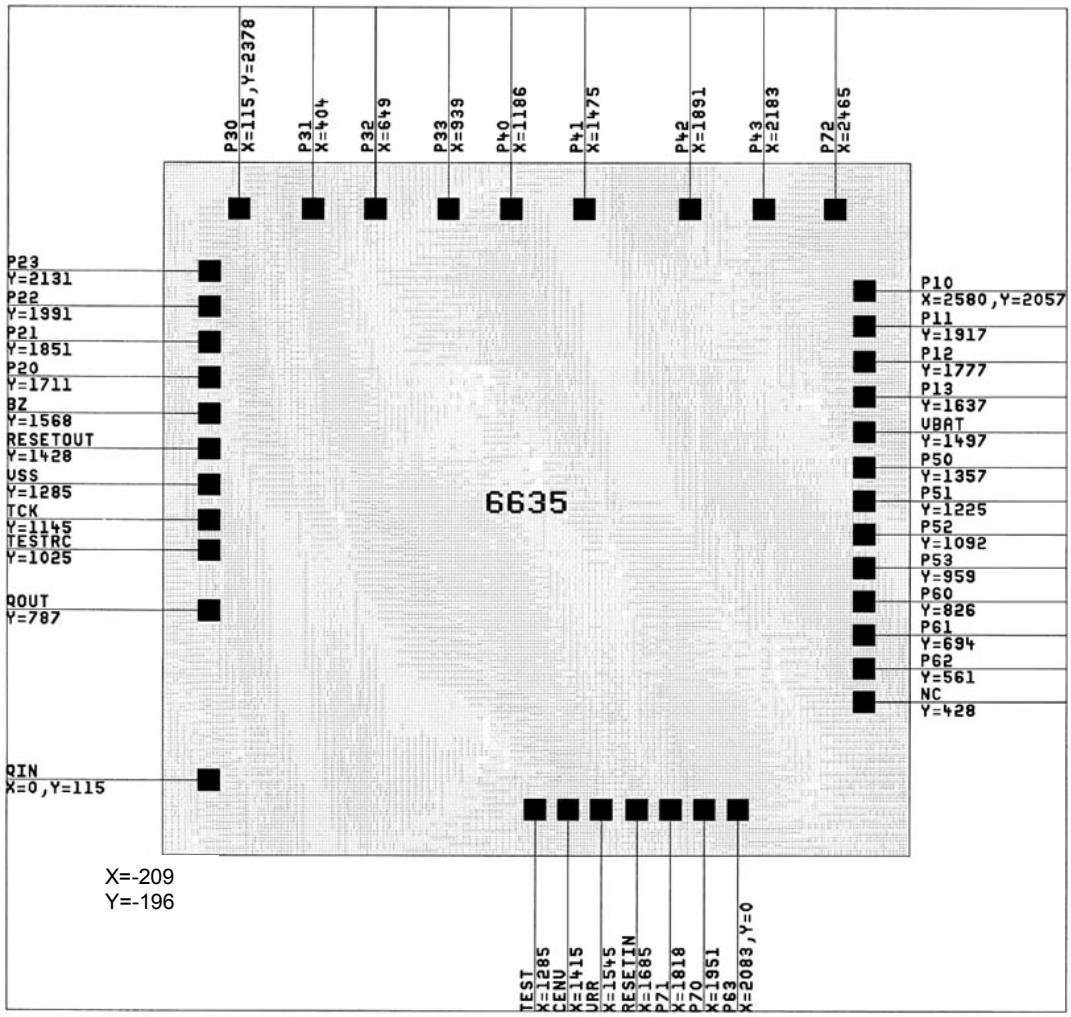
Note 7: The resistor value can be programmable by metal mask (20k to 360k by step of 20k). The value must be checked and agreed by EM Microelectronic-Marin.

19.8 AC Characteristics at Inputs

Conditions: T= +25°C (unless otherwise specified), f_{OSC} = 32768 Hz
V_{DD} =1.55V means; measures without voltage regulator
V_{DD}=3.00V means; measures with voltage regulator

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Input Pull-down activation						
Time at P1, P2	mask option	t_{PD}	31		62	µs
frequency		t_{PD}		512		Hz
Input Pull-down Current	**V_{DD} = 1.55V**					
Pull Down Mean Input Current at P1, P2	t_{PD} = 30.5µs	I_{PD}	8		32	nA
Pull Down Mean Input Current at P1, P2	t_{PD} = 61µs	I_{PD}	16		64	nA
NMOS-Holder Low Current at P1, P2	V_{IN} = 0.3V	IH_{LO}	10		50	µA
External contact resistance	(to fight pull down)	R_{CO}			20	kΩ
Input Pull-down Current	**V_{DD} = 3.00V**					
Pull Down Mean Input Current at P1, P2	t_{PD} = 30.5µs	I_{PD}	32		128	nA
Pull Down Mean Input Current at P1, P2	t_{PD} = 61µs	I_{PD}	64		256	nA
NMOS-Holder Low Current at P1, P2	V_{IN} = 0.3V	IH_{LO}	5		70	µA
External contact resistance	(to fight pull down)	R_{CO}			60	kΩ
Duty cycle at FOUT		DC_{FO}		50		%
Frequency SCL	Slave Mode	f_{SCL}	100			kHz

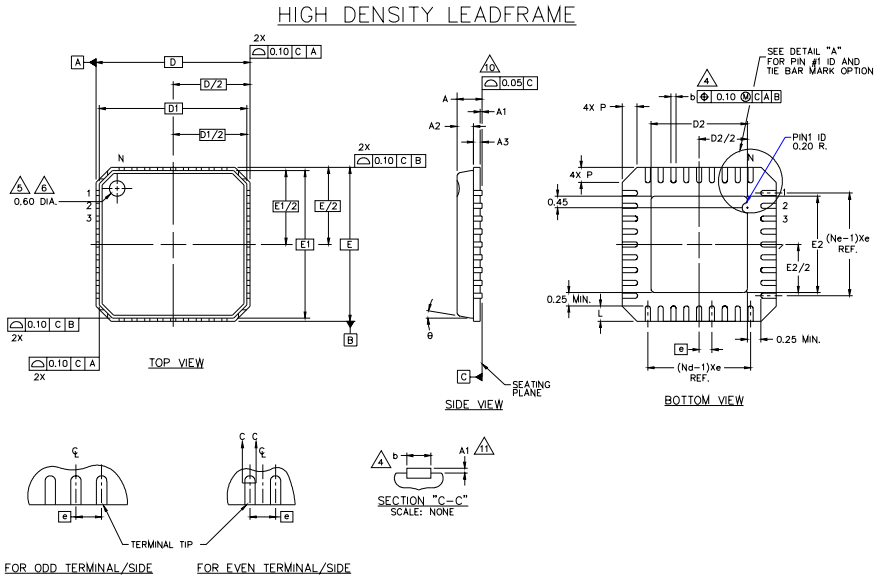
20. Pad Location Diagram



X = 3.00mm Y = 2.77mm

21. Package Information

MLF2, 40 LEAD, 6 x 6 mm BODY



SYMBOL	PITCH VARIATION A			NOTE	PITCH VARIATION B			NOTE	PITCH VARIATION C			NOTE	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
e		0.80 BSC				0.65 BSC				0.50 BSC				0.50 BSC		
N		20		3		28		3		36		3		40		3
Nd		5		3		7		3		9		3		10		3
Ne		5		3		7		3		9		3		10		3
L	0.50	0.60	0.75		0.50	0.60	0.75		0.50	0.60	0.75		0.30	0.40	0.50	
b	0.28	0.33	0.40	4	0.23	0.28	0.35	4	0.18	0.23	0.30	4	0.18	0.23	0.30	4
Q	0.30	0.40	0.65	12	0.30	0.40	0.65	12	0.30	0.40	0.65	12	0.00	0.20	0.45	12
D2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: B			
E2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: B			
*** D2	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION: C			**
*** E2	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION			*	SEE EXPOSED PAD VARIATION: C			**
*** D3	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION: A			**
*** E3	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION			*	SEE MIXED RING PAD VARIATION: A			**

* NOT DESIGNED YET
** DESIGNED BUT NOT TOOLED UP
*** APPLIES TO MIXED RING PAD DESIGN ONLY

<STANDARD>

SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	A	3.55	3.70	3.85	3.55	3.70	3.85	
	B	3.95	4.10	4.25	3.95	4.10	4.25	

EXAMPLE ; WE CAN CALL VARIATION "BB" FOR 28 TERMINAL MLF2
WITH 4.10 mm X 4.10 mm NOMINAL EXPOSED PAD DIMENSION.
THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND
THE LATER ONE IS FOR EXPOSED PAD VARIATION.

<MIXED RING>

*** SYMBOLS		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED PAD VARIATIONS	C	2.95	3.10	3.25	2.95	3.10	3.25
SYMBOLS		D3			E3		
		MIN	NOM	MAX	MIN	NOM	MAX
MIXED RING PAD VARIATIONS	A	4.15	4.30	4.45	4.15	4.30	4.45

EXAMPLE ; WE CAN CALL VARIATION "DCA" FOR 40 TERMINAL MLF2
WITH 3.10 mm X 3.10 mm NOMINAL EXPOSED PAD DIMENSION,
AND WITH 4.30 mm X 4.30 mm NOMINAL EXPOSED MIXED RING PAD DIMENSION.
THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND
THE LATER ONES ARE FOR EXPOSED PAD AND MIXED RING PAD VARIATION.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		6.00 BSC		
D1		5.75 BSC		
E		6.00 BSC		
E1		5.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	12
*** K	0.20	0.30	0.40	
*** S	0.50	0.60	0.65	
*** J	0.60	1.00	1.50	

22. Ordering Information

Packaged Device:

EM6635 LF A - %%%

Package:
LF = 40 pin Micro Lead Frame

Delivery Form:
A = Stick

Customer Version:
customer -specific number
given by EM Microelectronic

Device in DIE Form:

EM6635 WS 11 - %%%

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WP = Waffle Pack

Thickness:
11 = 11 mils (280um), by default
27 = 27 mils (686um), not backlapped
(for other thickness, contact EM)

Customer Version:
customer-specific number
given by EM Microelectronic

Please contact EM Microelectronic-Marin S.A. for availability of MLF2 package.