3936

DMOS THREE-PHASE PWM MOTOR DRIVER

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} ..... **50 V**
Output Current, I_{OUT}..... **±3 A***
Logic Supply Voltage, V_{DD}..... **7.0 V**
Logic Input Voltage Range, V_{IN}
(t_W>30 ns)..... **-0.3 V to V_{DD} + 0.3 V**
(t_W<30 ns)..... **-1.0V to V_{DD} +1V**
Sense Voltage, V_{SENSE}..... **0.5 V**
Reference Voltage, V_{REF} ..... **V_{DD}**
Package Power Dissipation,
P_D ..... **3.9 W**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C**
Storage Temperature Range,
T_S..... **-55°C to +150°C**

***** Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

Designed for pulse-width modulated (PWM) current control of three-phase brushless dc motors, the A3936SED is capable of peak output currents to ± 3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control timing circuitry can be configured to operate in slow-, fast- and mixed-decay modes.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, and crossover current protection. Special power up sequencing is not required.

The A3936 is supplied in a 44-pin plastic PLCC with a copper batwing tabs (suffix 'ED'). The power tabs are at ground potential and need no electrical isolation. This device is also available in a lead-free version (100% matte tin leadframe).

Features

- ±3 A, 50 V Continuous Output Rating
- Low $r_{DS(on)}$ Outputs (typically 500 mΩ source, 315 mΩ sink)
- Configurable Mixed, Fast and Slow Current-Decay Modes
- Synchronous Rectification for Low Power Dissipation
- Internal UVLO and Thermal Shutdown Circuitry
- Crossover-Current Protection
- Tachometer Output for External Speed Control Loop

Always order by complete part number

Part Number	Package
A3936SED	44-pin PLCC
A3936SED-T	44-pin PLCC, Lead-free

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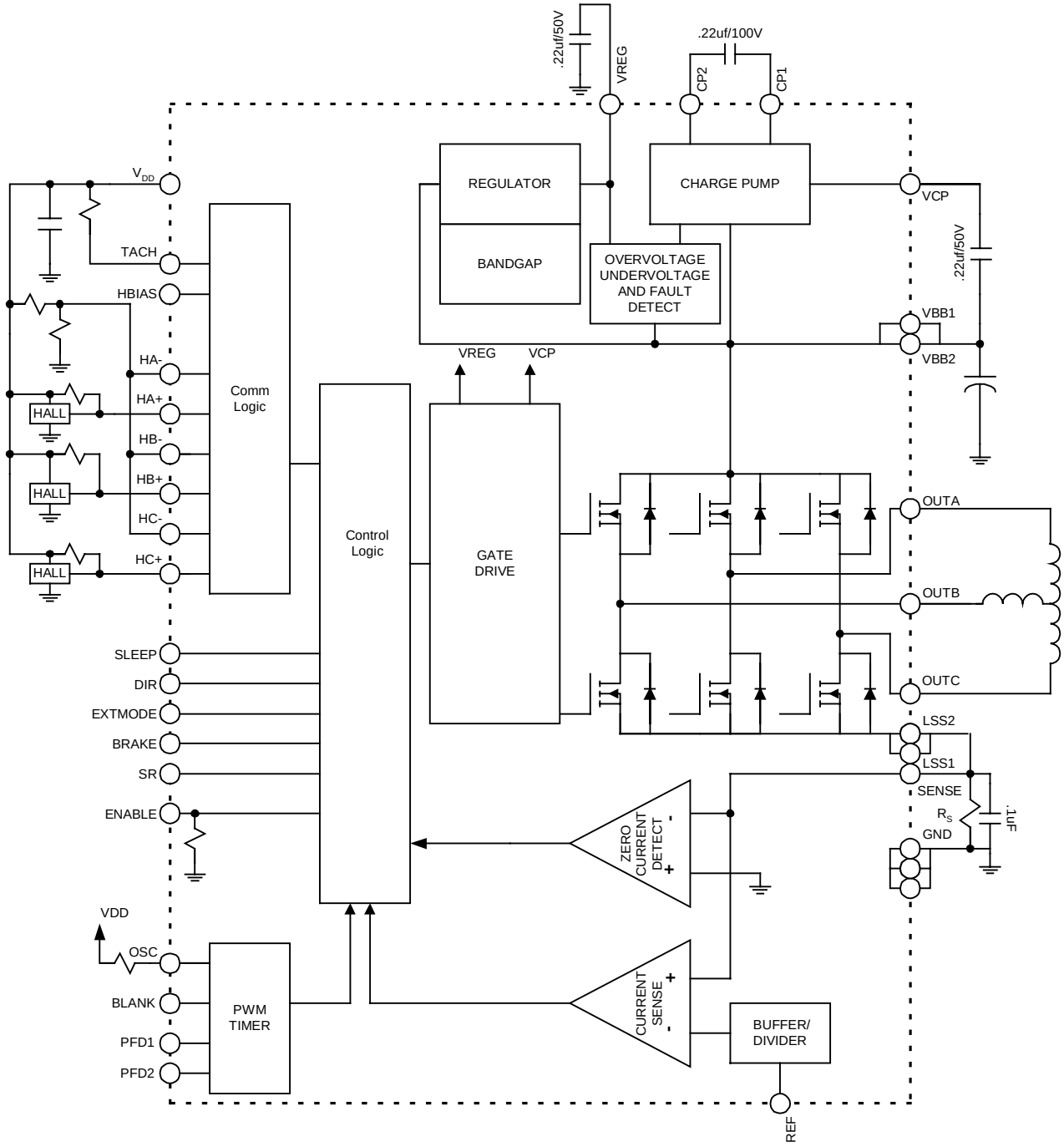
FUNCTIONAL BLOCK DIAGRAM



3936 Three Phase PWM Motor Driver

ELECTRICAL CHARACTERISTICS at T_J = +25°C, VBB = 50 V, V_{DD} = 5.0 V, f_{PWM} < 50KHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	VBB	Operating	9	–	50	V
		During Sleep Mode	0		50	V
Output Leakage Current	I_{DSS}	$V_{OUT} = V_{BB}$	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<–1.0	-20	µA
Output On Resistance	R_{DSON}	Source Driver, I_{OUT} = -3A	–		.55	Ω
		Sink Driver, I_{OUT} = 3A	–		.35	Ω
Body Diode Forward Voltage	V_F	Source Diode, I_F = -3A	–	–	1.4	V
		Sink Diode, I_F = 3A	–	–	1.3	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	4	7	mA
		Charge Pump On, Outputs Disabled	–	2	5	mA
		Sleep Mode	–	–	20	uA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz		–	10	mA
		Outputs Off		–	8	mA
		Sleep Mode (Inputs below .5V)			100	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		V_{DD}*.5	–	–	V
	$V_{IN(0)}$		–	–	V_{DD}*.2	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$*.5	-20	<1.0	20	µA
(except ENABLE)	$I_{IN(0)}$	$V_{IN} = V_{DD}$*.2	-20	<-1.0	20	µA
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$*.5	–		100	µA
ENABLE Input	$I_{IN(0)}$	$V_{IN} = V_{DD}$*.2	–		30	µA
Internal Oscillator	f_{OSC}	OSC shorted to GND	3	4	5	MHz
		R_{OSC}= 51K	3.4	4	4.6	MHz

ELECTRICAL CHARACTERISTICS at T_J = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, f_{PWM} < 50KHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic						
Buffer Input Offset Volt.	V_{IO}			±10		mV
V_{REF} Input Voltage Range		Operating	0.0	–	V_{DD}	V
Reference Input Current	I_{REF}	$V_{REF} = V_{DD}$,V_{BB}=0 to 50V	-.5	0	0.5	µA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V		±5		mV
G_M Error	V_{ERR}	$V_{REF} = V_{DD}$	-4		4	%
	(Note 3)	V_{REF} = .5V	-14		14	%
Propagation Delay Times	tpd	50% TO 90%, SR Enabled				
		PWM CHANGE TO SOURCE ON	600	750	1000	ns
		PWM CHANGE TO SOURCE OFF	50	150	350	ns
		PWM CHANGE TO SINK ON	600	750	1000	ns
		PWM CHANGE TO SINK OFF	50	100	150	ns
Crossover Delay	t_{COD}	SR Enabled	300	600	1000	ns
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold		Rising V_{DD}	2.45	2.7	2.95	V
UVLO Hysteresis			0.05	0.10	–	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device pin.
3. $V_{ERR} = ((V_{REF}/10) – V_{SENSE})/(V_{REF}/10)$

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V f_{PWM} < 50KHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Hall Logic						
Hall Input Current	I_{HALL}	V_{IN} = 1.2V	-1	0	1	µA
Common Mode Input Range	VCMR		.3		2.5	V
AC Input Voltage Range	V_{HALL}		.120			Vp-p
Hysteresis	V_{HYS}	T_A= -20 to 85 deg C.	10		30	mV
Pulse Reject Filter			3	5.5	8	µs
Hall Bias Output Sat Voltage	V_{HB}	I_{OUT}=40mA, T_A= -20 to 85 deg C.		.4	.5	V
	I_{HB}				40	mA
Tach Output	V_{OL}	I_{OUT}= 500uA			.5	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device pin.

Commutation Truth Table

	120 spacing				Outputs		
	HA	HB	HC	DIR	OUTA	OUTB	OUTC
1	+	-	+	FOR	HI	LO	Z
2	+	-	-	FOR	HI	Z	LO
3	+	+	-	FOR	Z	HI	LO
4	-	+	-	FOR	LO	HI	Z
5	-	+	+	FOR	LO	Z	HI
6	-	-	+	FOR	Z	LO	HI
1	+	-	+	REV	LO	HI	Z
2	+	-	-	REV	LO	Z	HI
3	+	+	-	REV	Z	LO	HI
4	-	+	-	REV	HI	LO	Z
5	-	+	+	REV	HI	Z	LO
6	-	-	+	REV	Z	HI	LO
	-	-	-	X	Z	Z	Z
	+	+	+	X	Z	Z	Z

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Functional Description

VREG. The VREG pin should be decoupled with a 0.22 µF capacitor to ground. This supply voltage is used to run the sink side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Charge Pump. The Charge Pump is used to generate a supply above VBB to drive the source side DMOS gates. A 0.22 uF ceramic monolithic capacitor should be connected between CP_1 and CP_2 for pumping purposes. A 0.22 uF ceramic monolithic capacitor should be connected between V_{CP} and VBB to act as a reservoir to run the high side DMOS devices. The V_{CP} Voltage is internally monitored and in the case of a fault condition the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on V_{CP} or V_{REG}, the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the UVLO circuit disables the drivers.

Current Regulation. Load current is regulated by an internal fixed off time PWM control circuit. When the outputs of the DMOS H-bridge are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{TRIP} = V_{REF}/(10*R_{SENSE})$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off time period. The current path during recirculation is determined by the configuration of slow/mixed decay mode and the synchronous rectification control setting.

Enable Logic. The Enable input terminal allows external PWM. ENABLE high turns ON the selected sink-source pair, enable low switches off the appropriate drivers and the load current decays. If the ENABLE pin is held high, the current will rise until it reaches the level set by the internal current control circuit.

ENABLE	Outputs
0	Source Chopped
1	ON

Extmode Logic. When using external PWM current control, the EXTMODE input determines the current path during the chopped cycle. With EXTMODE set low, fast decay mode, both the source and sink drivers are chopped OFF during the decay time (ENABLE=0). With EXTMODE high, slow decay mode, only the source driver turns off during the current decay time.

EXTMODE	Decay
0	Fast
1	Slow

Sleep Mode. The input pin SLEEP is dedicated to put the device into a minimum current draw mode. When asserted low, all circuits are disabled.

Fixed Off-Time. The 3936 is set for a fixed off time of 96 counts of the internal oscillator, typically 24 µs with 4Mhz oscillator.

Internal Current Control Mode. Input pins PFD1 and PFD2 determine the current decay method after an overcurrent event is detected at sense input. In slow decay mode both sink side drivers are turned on for the fixed off time period. Mixed decay mode starts out in fast decay mode for the selected percentage of the fixed off time, and then is followed by slow decay for the rest of the period.

PFD2	PFD1	% t_{OFF}	Decay
0	0	0	Slow
0	1	15	Mixed
1	0	48	Mixed
1	1	100	Fast

PWM Blank Timer. When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the sense comparator is blanked. The blank timer runs after the off time counter to provide the blanking function. The blank timer is reset when ENABLE is chopped or DIR is changed. For external PWM control, a DIR change or ENABLE ON will trigger the blanking function. The duration is adjusted by control input BLANK.

BLANK	t_{BLANK}
0	$6/f_{OSC}$
1	$12/f_{OSC}$

Brake. Logic high to the brake terminal activates the brake function, logic low allows normal operation. Brake will turn all three sink drivers ON and effectively shorts out the motor generated BEMF. It is important to note that the internal PWM current control circuit will not limit the current when braking, since the current does not flow through the sense resistor. The maximum current can be approximated by V_{BEMF}/R_L. Care should be taken to insure that the maximum ratings of the device are not exceeded in worse case braking situations of high speed and high inertial loads.

Oscillator. The PWM timer is based on an internal oscillator set by a resistor connected from the OSC terminal to V_{DD}. Typical value of 4Mhz is set with 51k resistor.

$$F_{OSC} = 204E9/R_{OSC}.$$

Tach. A tachometer signal is available for speed measurement. This open collector output toggles at each Hall transition.

Synchronous Rectification. Logic high applied to the SR terminal enables synchronous rectification. When a PWM off cycle is triggered, either by an ENABLE chop command or internal fixed off time cycle, load current will recirculate according to the decay mode selected by control logic. The A3936 synchronous rectification feature will turn on the appropriate MOSFET(s)during the current decay and effectively short out the body diodes with the low Rdson driver. This will lower power dissipation significantly and can eliminate the need for external schottky diodes.

Reversal of load current is prevented by turning off synchronous rectification when a zero current level is detected.

Terminal List

Pin No.	Pin Name	Pin Description
1	GND	
2	GND	
3	HA+	Hall input
4	HA-	Hall input
5	HB+	Hall input
6	HB-	Hall input
7	HC+	Hall input
8	HC-	Hall input
9	V_{DD}	Logic Supply Voltage
10	REF	G_m Reference Input Voltage
11	GND	
12	GND	
13	GND	
14	BRAKE	Logic Input
15	SENSE	Sense Resistor Connection
16	SR	Logic Input (Disabled = Low, Active SR = High)
17	OUTA	DMOS H – Bridge A
18	HBIAS	Connection for hall element neg side
19	VBB1	Load Supply Voltage
20	LSS1	Low Side Source connection
21	OUTB	DMOS H – Bridge B
22	GND	
23	GND	
24	GND	
25	LSS2	Low Side Source connection
26	VBB2	Load Supply Voltage
27	TACH	Speed output
28	OUTC	DMOS H – Bridge C
29	V_{CP}	Reservoir Capacitor Terminal
30	CP1	Charge Pump Capacitor Terminal
31	CP2	Charge Pump Capacitor Terminal
32	SLEEP	Logic input for SLEEP mode
33	GND	
34	GND	
35	GND	
36	OSC	Oscillator Terminal
37	V_{REG}	Regulator decoupling Terminal
38	DIR	Logic Input
39	ENABLE	Logic Input
40	EXTMODE	Logic Input
41	BLANK	Logic Input
42	PFD2	Logic Input
43	PFD1	Logic Input
44	GND	Power Ground Tab

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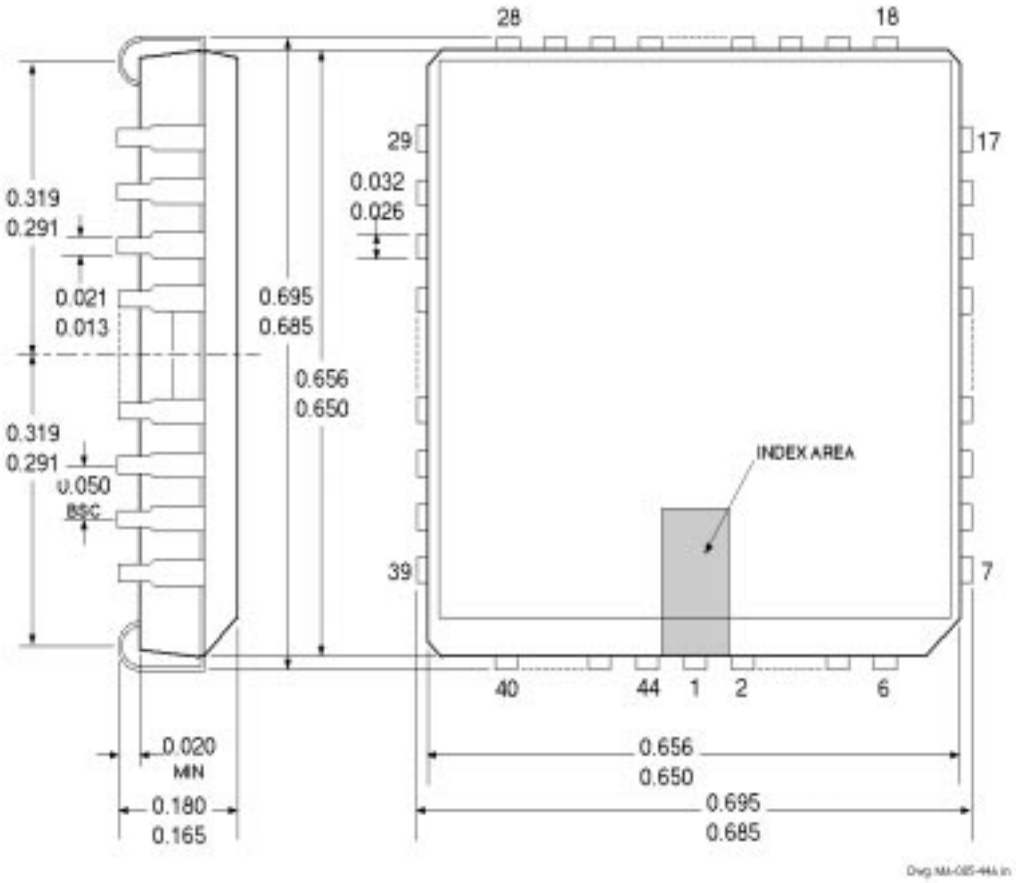
28
18
29
17
0.032
0.026
0.319
0.291
0.021
0.013
0.695
0.685
0.656
0.650
0.319
0.291
0.050
BSC
INDEX AREA
39
7
40
44
1
2
6
0.020
MIN
0.180
0.165
0.656
0.650
0.695
0.685