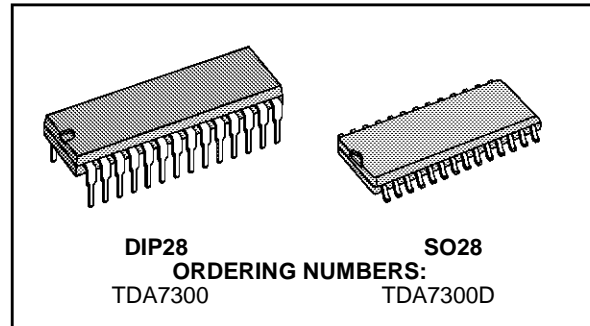


**DIGITAL CONTROLLED STEREO AUDIO PROCESSOR**

- SINGLE SUPPLY OPERATION
- FOUR STEREO INPUT SOURCE SELECTION
- MONO INPUT
- TREBLE, BASS, VOLUME, AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



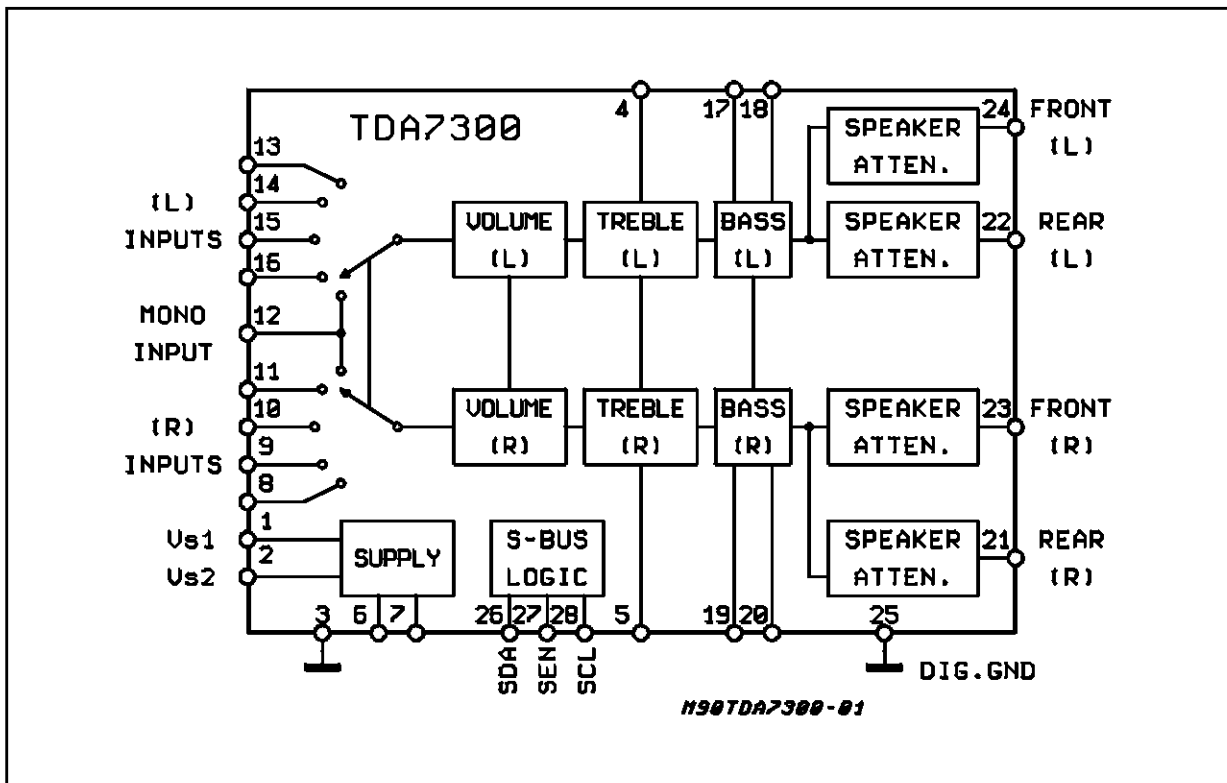
processor for high quality audio applications in car radio and Hi-Fi systems.

Control is accomplished by serial bus microprocessor interface. The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers. The results are: low noise, low distortion and high dynamic range.

**DESCRIPTION**

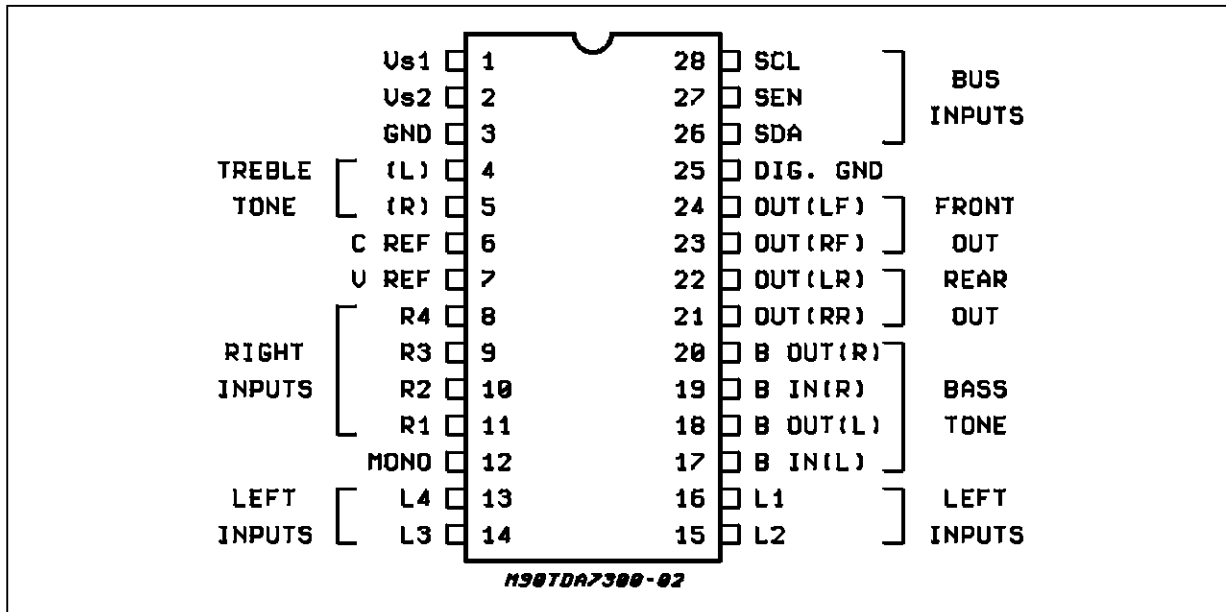
The TDA7300 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor.

**BLOCK DIAGRAM**



## TDA7300

### PIN CONNECTION (Top view)



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	Supply Voltage ( $V_{S1}$ )	18	V
$T_{amb}$	Operating Ambient Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature	-40 to 150	°C

### THERMAL DATA

Symbol	Description	SO28	DIP28	Unit
$R_{th\ j-pins}$	Thermal Resistance Junction-pins	85	65	°C/W

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^\circ\text{C}$ ,  $V_{S1} = 12\text{V}$  or  $V_{S2} = 8.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  and  $R_g = 600\Omega$ ,  $f = 1\text{KHz}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

#### SUPPLY (1)

$V_{S1}$	Supply Voltage $V_{S1}$		10	12	16	V
$V_{S2}$	Supply Voltage $V_{S2}$		6	8.5	10	V
$I_{S2}$	Supply Current		15	30	40	mA
$V_{ref}$	Reference Voltage (pin 7)		3.5	4.3	5	V
SVR	Ripple Rejection at $V_{S1}$	$f = 300\text{Hz}$ to $10\text{KHz}$	80	97		dB
SVR	Ripple Rejection at $V_{S2}$	$f = 300\text{Hz}$ to $10\text{KHz}$	50	58		dB

#### INPUT SELECTORS

$R_i$	Input Resistance		30	45		$\text{K}\Omega$
$V_{IN\ max}$	Max. Input Signal	$GV = 0\text{dB}$ $d = 0.3\%$	1.5	2.2		$V_{rms}$
$IN_s$	Input Separation	$f = 1\text{KHz}$ (2)	90	100		dB
		$f = 10\text{KHz}$ (2)	70	80		dB
$V_i\ (DC)$	Input DC Voltage		3.5	4.3	5	V

**ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
--------	-----------	----------------	------	------	------	------

**VOLUME CONTROLS**

	Control Range			78		dB
$G_{max}$	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution	$G_V = -50$ to 10dB		2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB

**SPEAKER ATTENUATORS**

	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB

**BASS AND TREBLE CONTROL (3)**

	Control Range			$\pm 15$		dB
	Step Resolution			2.5	3.5	dB

**AUDIO OUTPUT**

$V_O$	Max. Output Voltage	$d = 0.3\%$	1.5	2.2		Vrms
$R_L$	Output Load Resistance		2			K $\Omega$
$C_L$	Output Load Capacitance				1	nF
$R_O$	Output Resistance			70	150	$\Omega$
$V_O(DC)$	DC Voltage Level		3	3.8	4.5	V

**GENERAL**

$e_{NO}$	Output Noise	BW = 22Hz to 22KHz, $G_V = 0$ dB		6	15	$\mu$ V
		Curve A $G_V = 0$ dB		4		
S/N	Signal to Noise Ratio	All gain = 0dB $V_O = 1$ Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	$f = 1$ KHz; $V_O = 1$ V; $G_V = 0$		0.01	0.1	%
	Frequency Response (-1dB)	$G_V = 0$	High Low	20	20	KHz Hz
$S_C$	Channel Separation left/right	$f = 1$ KHz		90	100	dB
		$f = 10$ KHz		70	80	

**BUS INPUTS**

$V_{IL}$	Input LOW Voltage				0.8	V
$V_{IH}$	Input HIGH Voltage		2.4			V
$V_O$	Output Voltage SDA Acknowledge	$I = 1.6$ mA			0.4	V
	Digital Input Current		-5		+5	$\mu$ A

**Notes:**

- (1) The circuit can be supplied either at  $V_{S1}$  or without the use of the internal voltage regulator at  $V_{S2}$ . The circuit also operates at a supply voltage  $V_{S1}$  lower than 10V. In this case the ripple rejection of  $V_{S2}$  is valid, because the voltage regulator saturates to a saturation voltage of about 0.8V.
- (2) The selected input is grounded thru the 2.2 $\mu$ F capacitor.
- (3) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be chosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

# TDA7300

Figure 1: Application Circuit

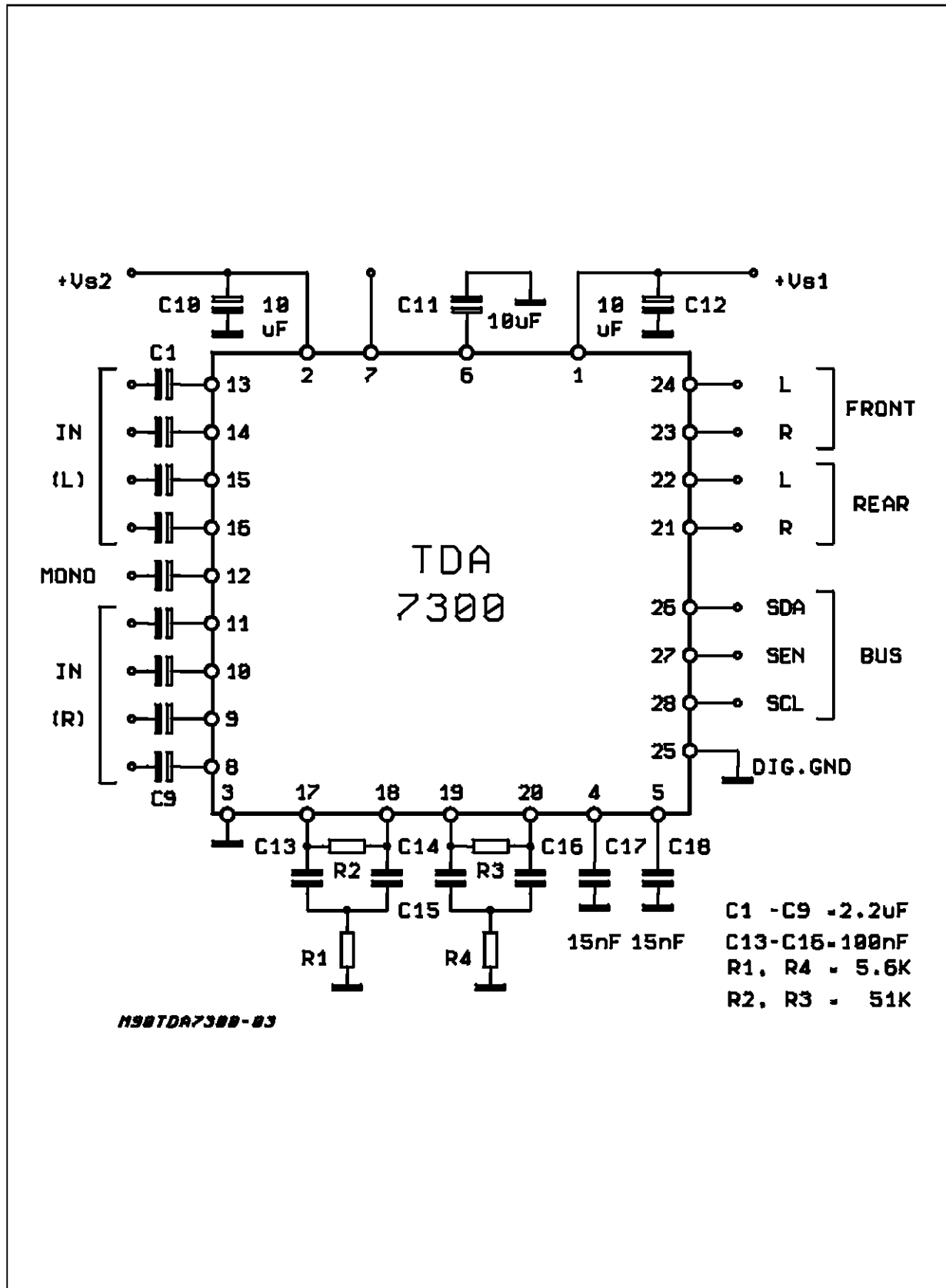


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

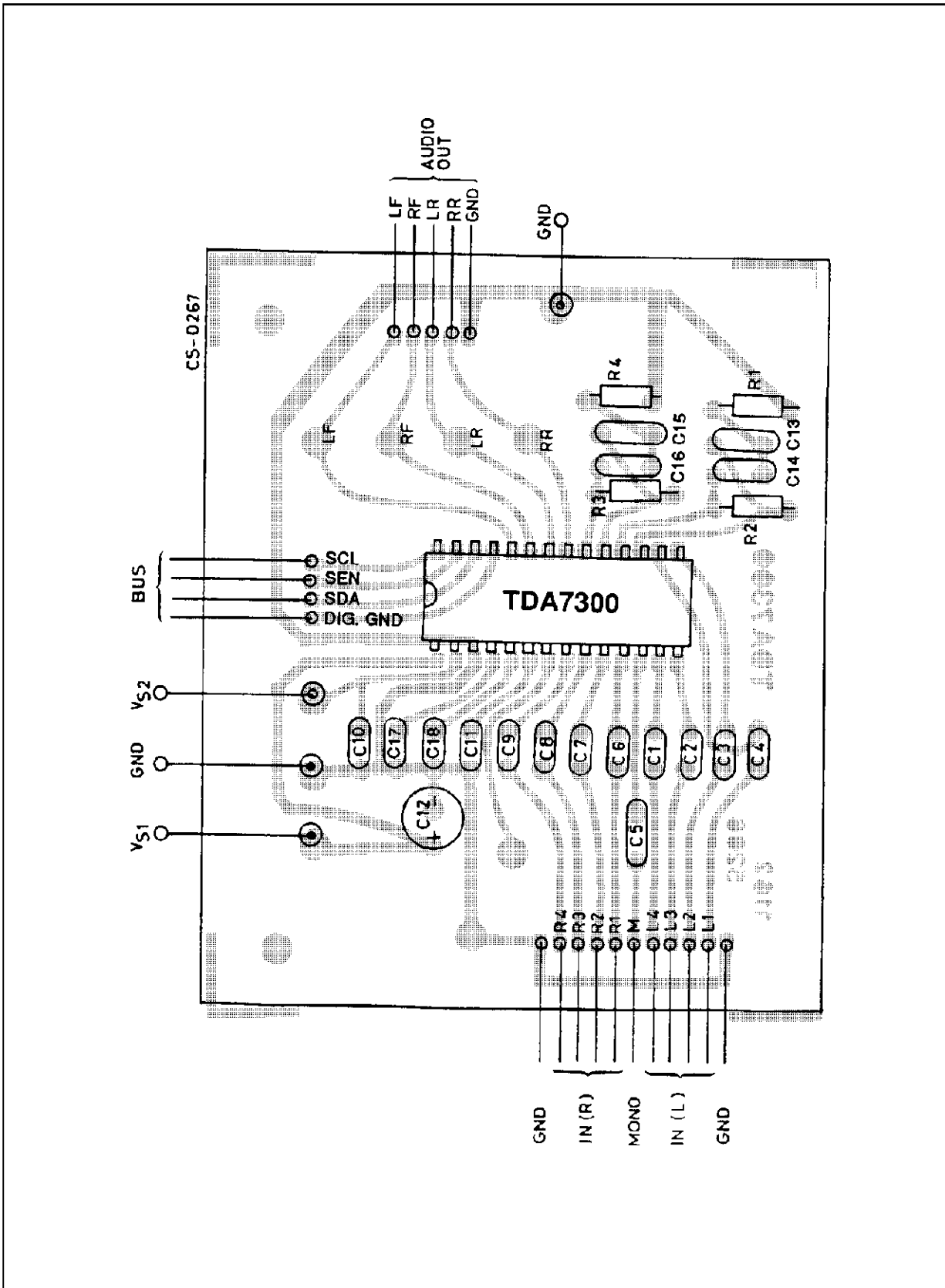


Figure 3: Total Output Noise vs. Volume Setting

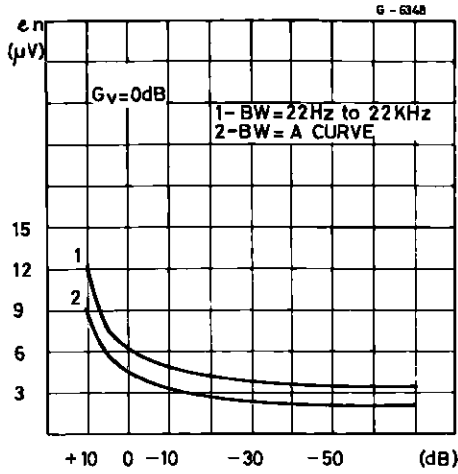


Figure 4: Signal to Noise Ratio vs. Volume Setting

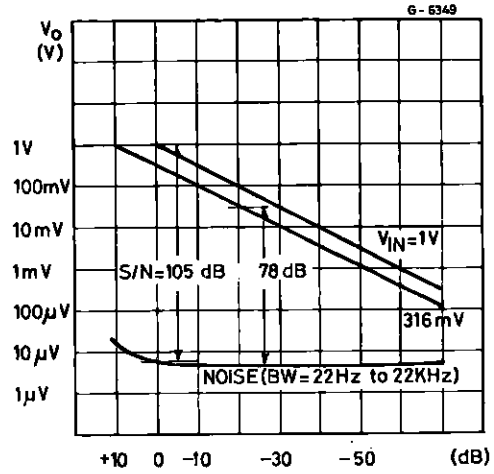


Figure 5: Distortion + Noise vs. Frequency

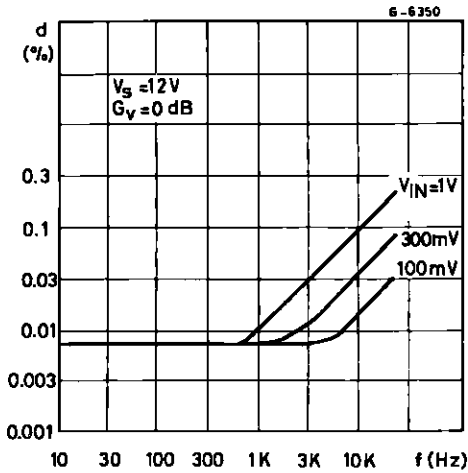


Figure 6: Distortion vs. Output Voltage

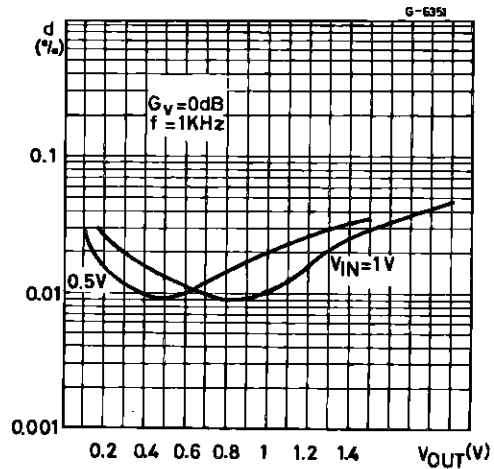


Figure 7: Distortion vs. Load Resistance

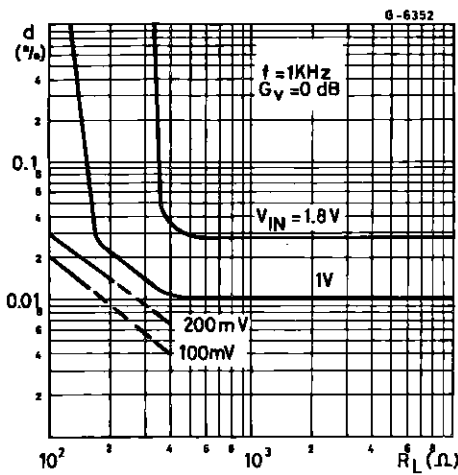
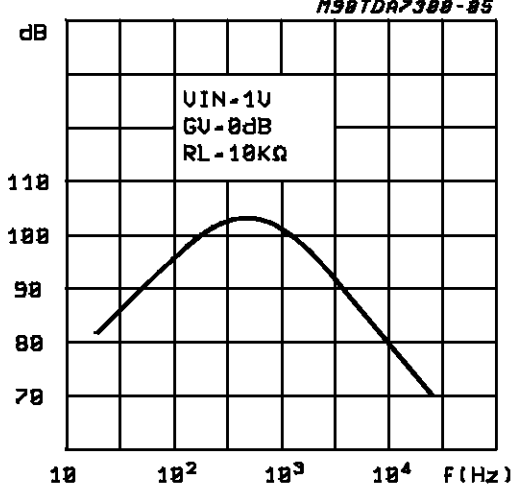
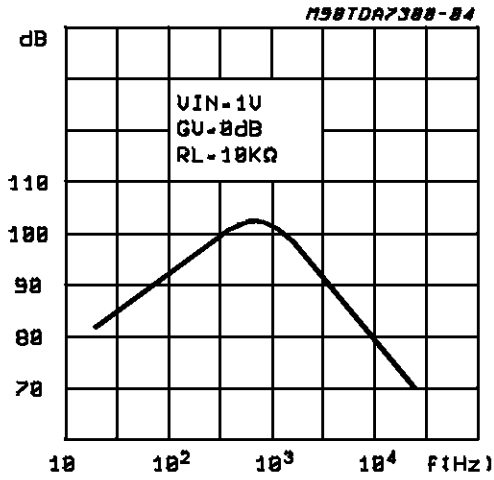


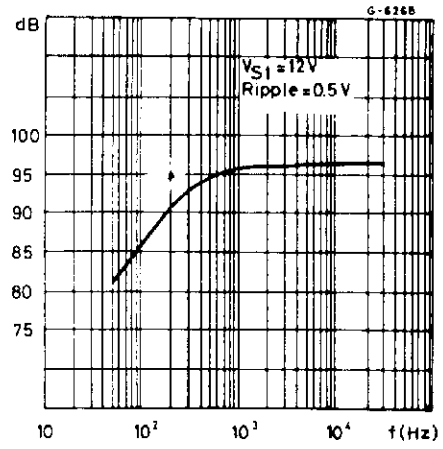
Figure 8: Channel Separation (L1 - R1) vs. Frequency



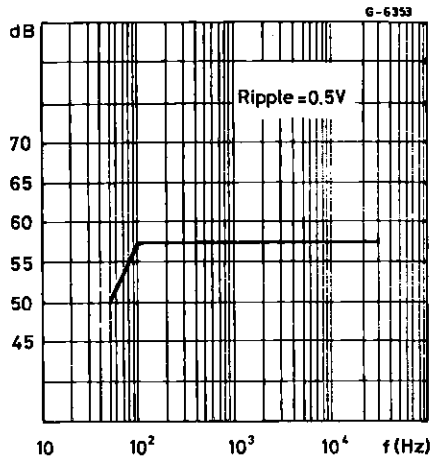
**Figure 9:** Input Separation (L1 - L2) vs. ( $V_{S1}$ ) Frequency



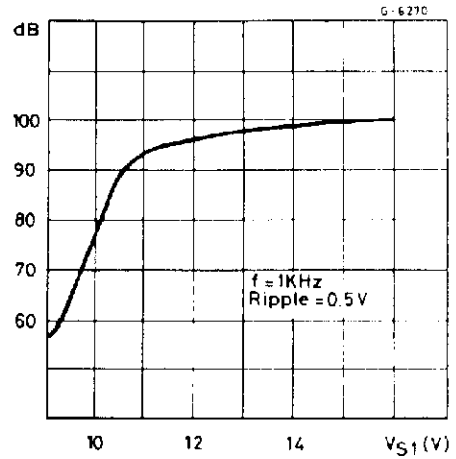
**Figure 10:** Supply Voltage Rejection ( $V_{S1}$ ) vs. Frequency



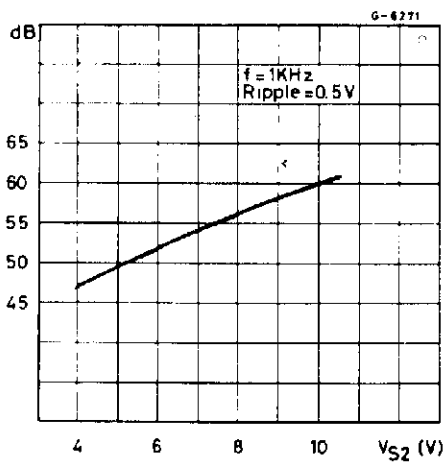
**Figure 11:** Supply Voltage Rejection ( $V_{S2}$ ) vs. Frequency



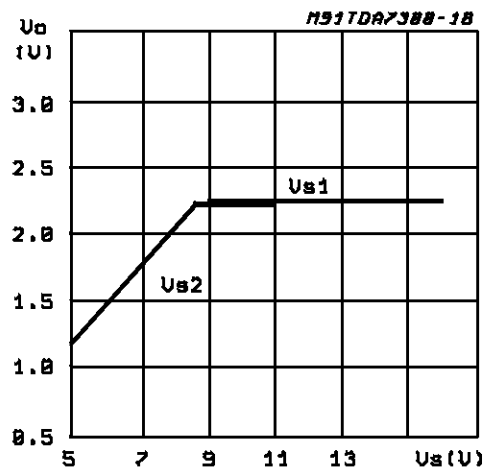
**Figure 12:** Supply Voltage Rejection vs.  $V_{S1}$



**Figure 13:** Supply Voltage Rejection vs.  $V_{S2}$



**Figure 14:** Clipping Level ( $V_{rms}$ ) vs. Supply Voltage



**APPLICATION INFORMATION**

**Volume Control Concept**

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.

The used concept, as shown in Fig. 15 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

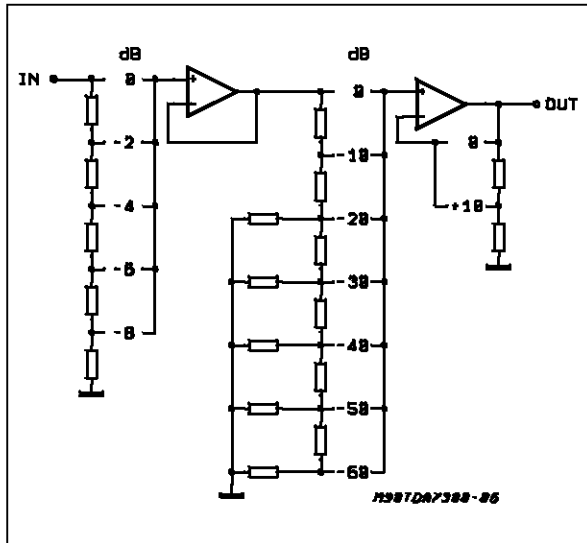
**Bass and Treble Control**

The principle operation of the bass control is shown in Fig. 16. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass. A typical curve is shown in Fig.19.

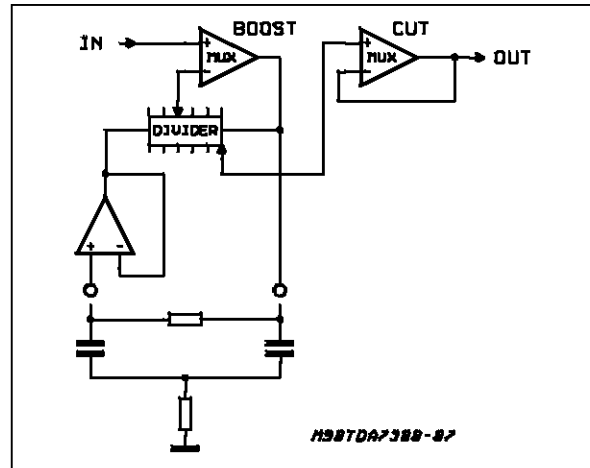
**Outputs**

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

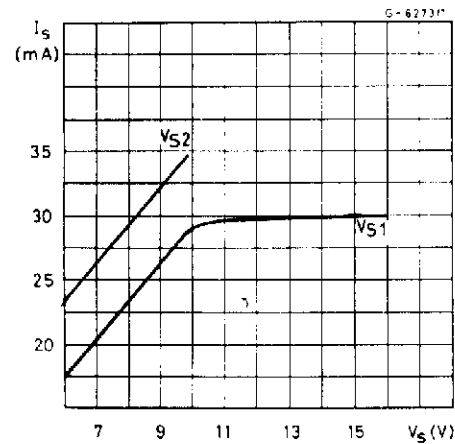
**Figure 15: Volume Control**



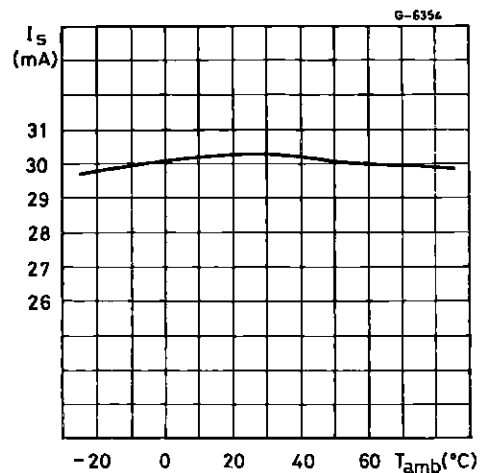
**Figure 16: Bass Control**



**Figure 17: Quiescent Current vs. Supply Voltage**



**Figure 18: Quiescent Current vs. Temperature**





APPLICATION INFORMATION (continued)

Figure 19: Typical Tone Response

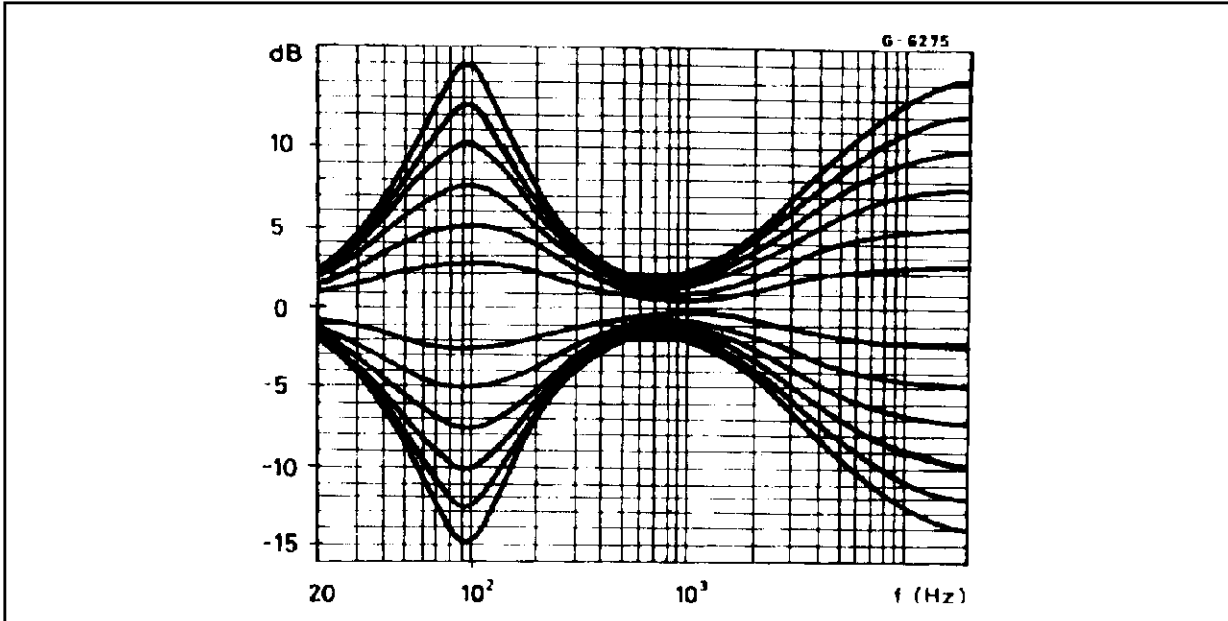
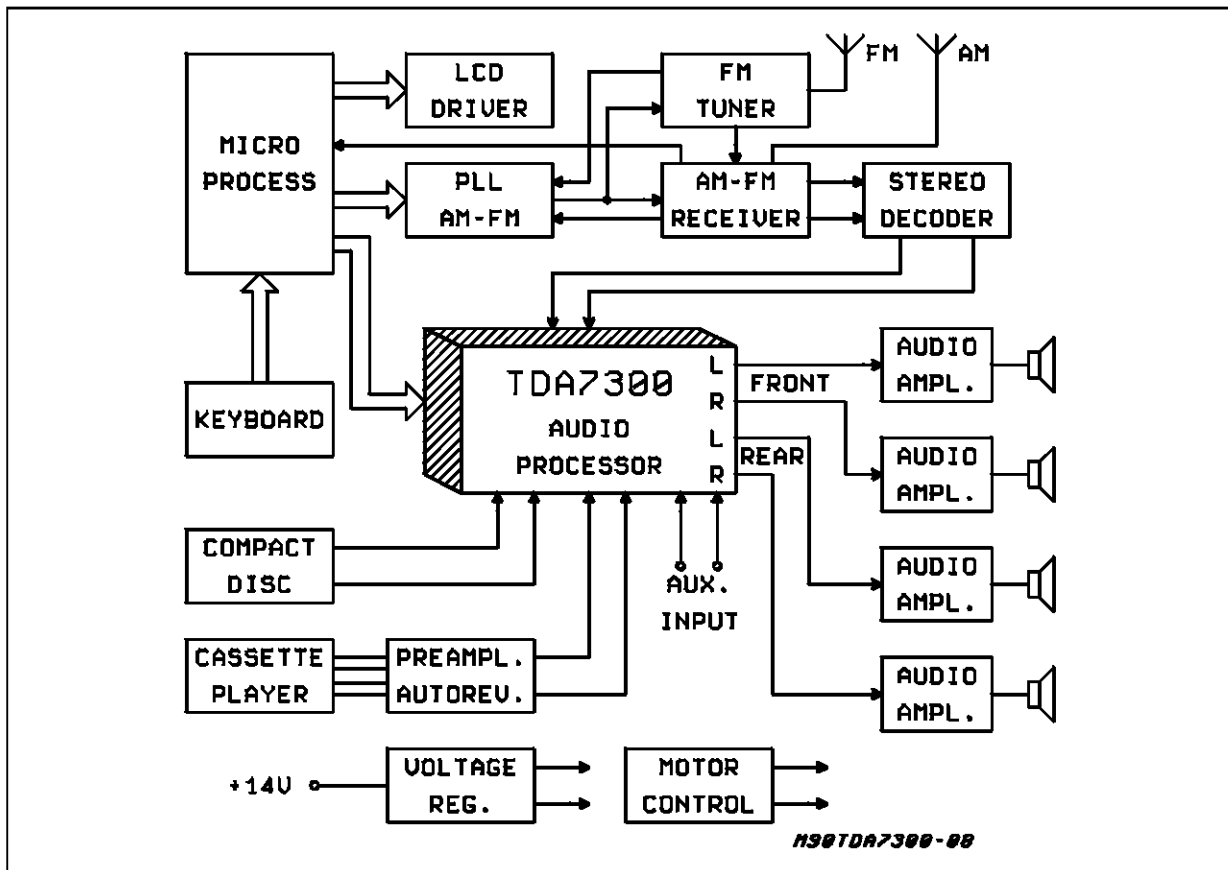


Figure 20: Complete Car-Radio System using Digital Controlled Audio Processor



**APPLICATION INFORMATION** (continued)

SERIAL BUS INTERFACE

**S-BUS Interface and I<sup>2</sup>C BUS Compatibility**

Data transmission from microprocessor to the TDA7300 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7300 appears as a standard I<sup>2</sup>C BUS slave.

According to I<sup>2</sup>C BUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors.

LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:

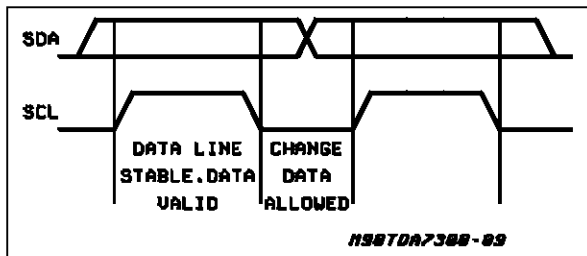
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 → 0 / 0 → 1) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

**Data Validity**

As shown in fig. 21, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

**Figure 21:** Data Validity on the I<sup>2</sup>C BUS



**Byte Format**

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

**Acknowledge**

The master (μP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 23). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

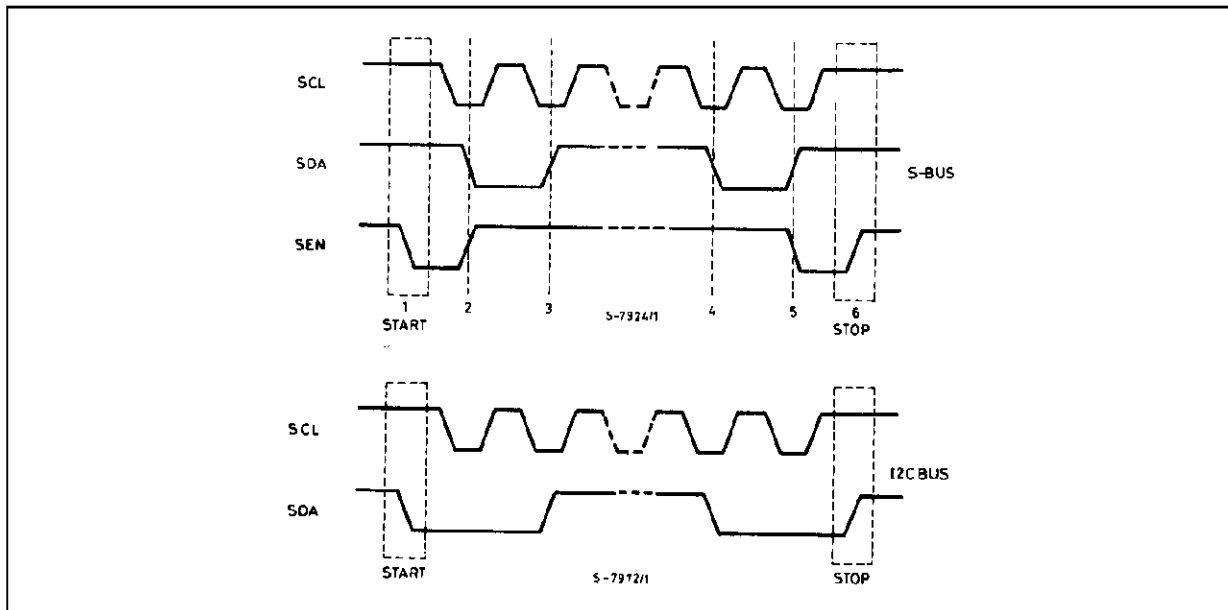
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

**Start and Stop Conditions**

I<sup>2</sup>C BUS:

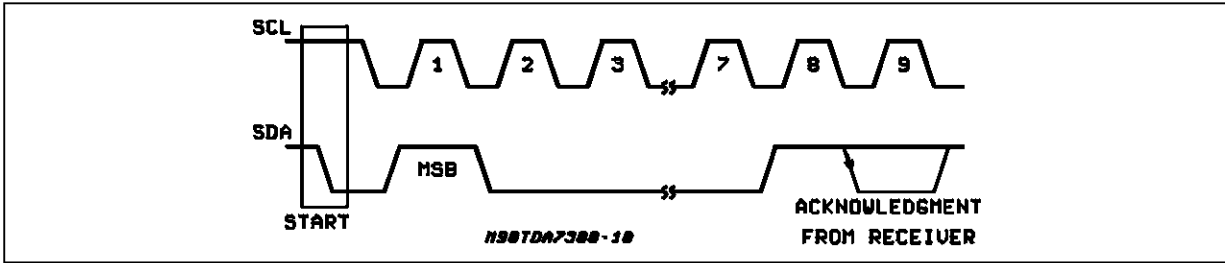
as shown in fig.22 a start condition is a HIGH to

**Figure 22:** Timing Diagram of S-BUS and I<sup>2</sup>C BUS



**APPLICATION INFORMATION** (continued)

**Figure 23:** Acknowledge on the I<sup>2</sup>C BUS



**Transmission without Acknowledge**

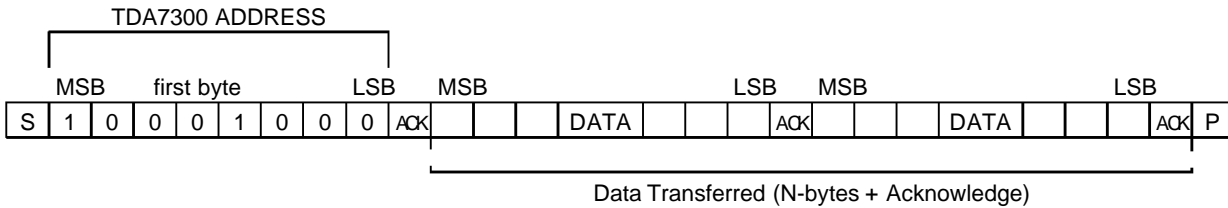
Avoiding to detect the acknowledge of the audio-processor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

**Interface Protocol**

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7300 address (the 8th bit of the byte must be 0). The TDA7300 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge  
 S = Start  
 P = Stop

MAX CLOCK SPEED 100kbits/s

**SOFTWARE SPECIFICATION**

Chip address (TDA7300 address)

1 0 0 0 1 0 0 0  
 MSB LSB

**DATA BYTES**

MSB	LSB							Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care  
 Ax = 2dB steps  
 Bx = 10dB steps  
 Cx = 2.5dB steps

**Status after power-on reset**

Volume	-68dB
Speaker	-38dB
Audio Switch	Mono
Bass	+2.5dB
Treble	+2.5dB

## TDA7300

### SOFTWARE SPECIFICATION (continued) DATA BYTES (detailed description)

#### VOLUME

MSB			LSB					
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB steps
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

#### SPEAKER ATTENUATORS

MSB			LSB					
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
		0	0					0
		0	1					-10
		1	0					-20
		1	1					-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

**SOFTWARE SPECIFICATION** (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB			LSB					
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Stereo 4
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

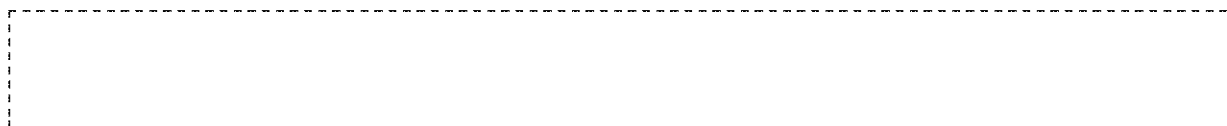
For example to set the stereo 2 channel the 8 bit string may be: 0 1 0 0 0 0 1

BASS AND TREBLE - Control Range of  $\pm 15$ dB (boost and cut) Steps of 2.5dB

0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	- 15
				0	0	0	1	- 15
				0	0	1	0	- 12.5
				0	0	1	1	- 10
				0	1	0	0	- 7.5
				0	1	0	1	- 5
				0	1	1	0	- 2.5
				0	1	1	1	- 0
				1	1	1	1	0
				1	1	1	0	2.5
				1	1	0	1	5
				1	1	0	0	7.5
				1	0	1	1	10
				1	0	1	0	12.5
				1	0	0	1	15
				1	0	0	0	15

C3 = Sign

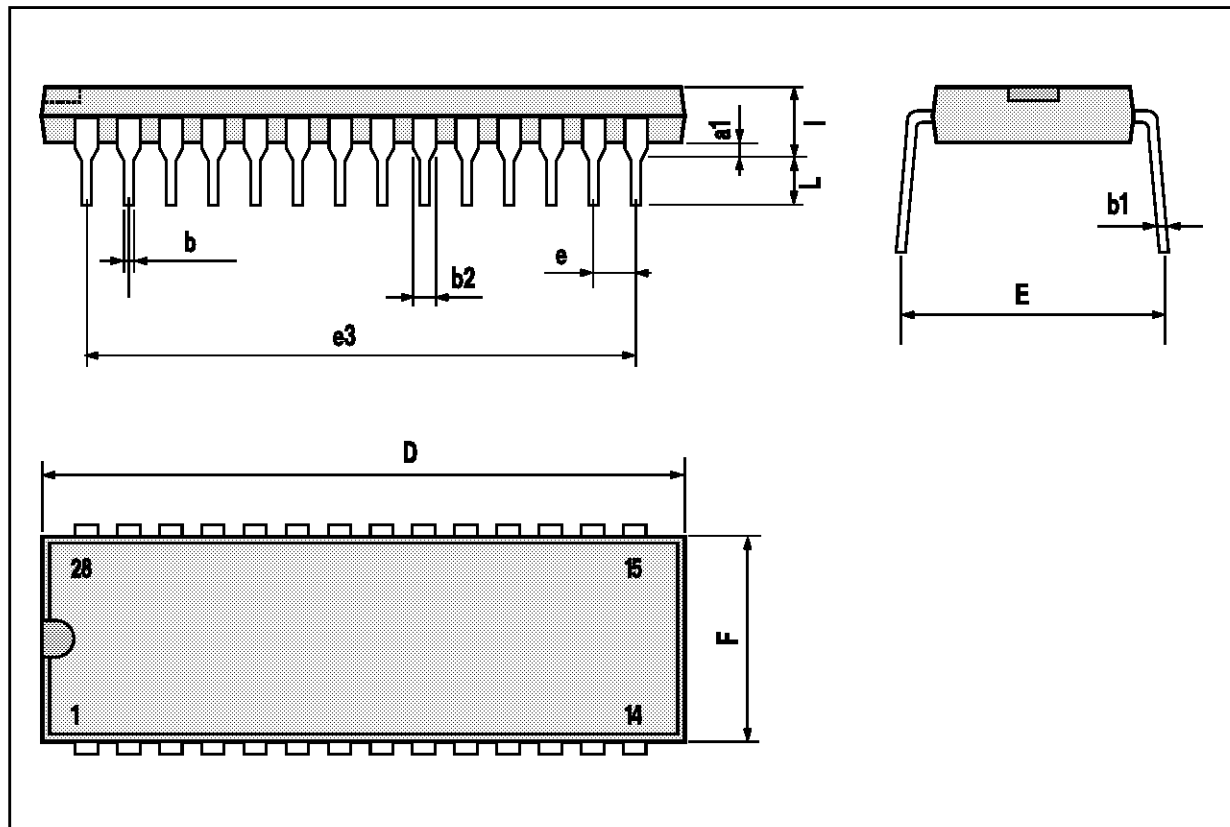
For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 1 0



# TDA7300

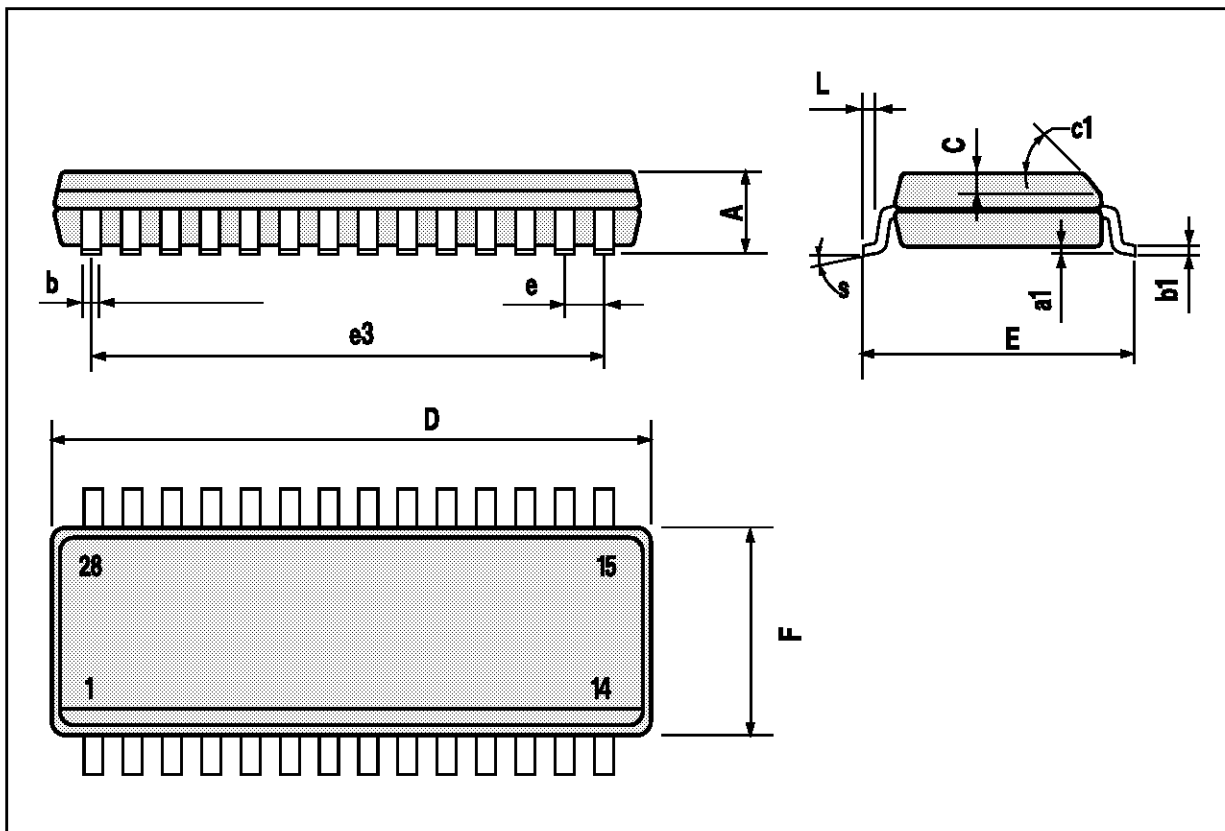
## DIP28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



## SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					



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