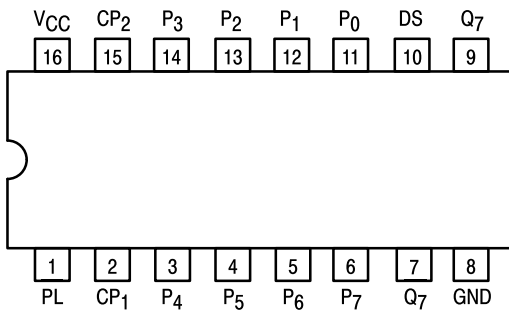




8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER

The SN54/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

CP₁, CP₂ Clock (LOW-to-HIGH Going Edge) Inputs
 DS Serial Data Input
 PL Asynchronous Parallel Load (Active LOW) Input
 P₀-P₇ Parallel Data Inputs
 Q₇ Serial Output from Last State (Note b)
 Q₇ Complementary Output (Note b)

LOADING (Note a)

	HIGH	LOW
CP ₁ , CP ₂	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
PL	1.5 U.L.	0.75 U.L.
P ₀ -P ₇	0.5 U.L.	0.25 U.L.
Q ₇	10 U.L.	5 (2.5) U.L.
Q ₇	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

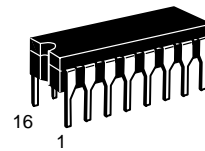
TRUTH TABLE

PL	CP		CONTENTS								RESPONSE
	1	2	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	P ₀	P ₁	P ₂	P ₃	P ₄	P ₅	P ₆	P ₇	Parallel Entry
H	L	↗	DS	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H	H	↗	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change
H	↗	L	DS	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H	↗	H	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change

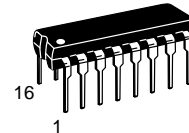
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

SN54/74LS165

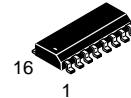
8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

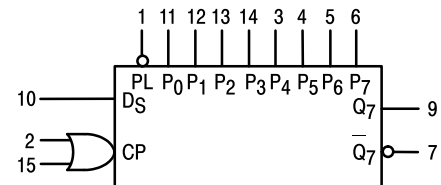


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXD SOIC

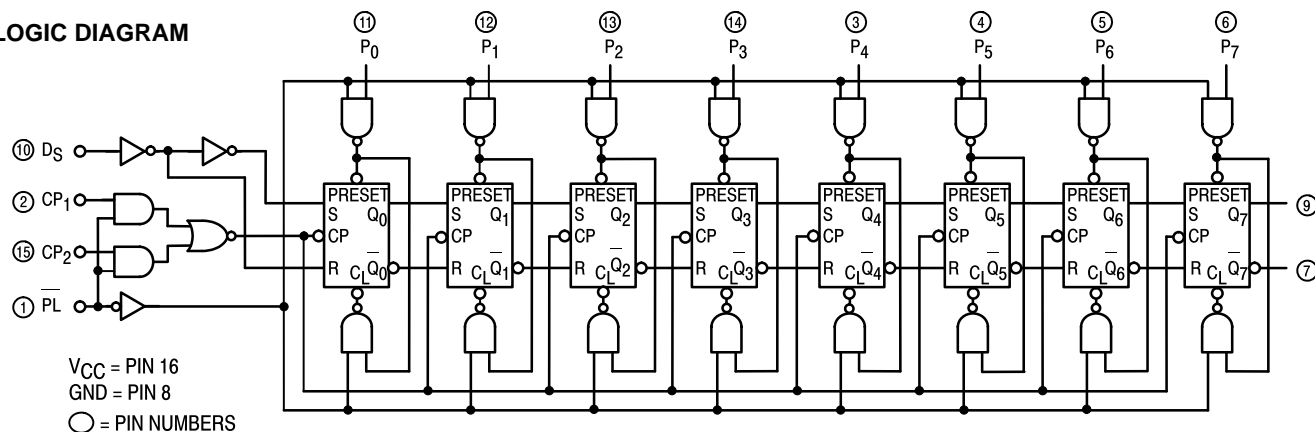
LOGIC SYMBOL



VCC = PIN 16
 GND = PIN 8

SN54/74LS165

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the PL signal is LOW. The parallel data can change while PL is LOW, provided that the recommended set-up and hold times are observed.

For clock operation, PL must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by

applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	$^{\circ}\text{C}$
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS165

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current Other Inputs PL Input			20 60	μA	V _{CC} = MAX, V _{IN} = 2.7 V
	Other Inputs PL Input			0.1 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Other Inputs PL Input			-0.4 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			36	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency	25	35		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay PL to Output		22 22	35 35	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to Output		27 28	40 40	ns	
t _{PLH} t _{PHL}	Propagation Delay P ₇ to Q ₇		14 21	25 30	ns	
t _{PLH} t _{PHL}	Propagation Delay P ₇ to Q ₇		21 16	30 25	ns	

SN54/74LS165

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	CP Clock Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
t_W	PL Pulse Width	15			ns	
t_S	Parallel Data Setup Time	10			ns	
t_S	Serial Data Setup Time	20			ns	
t_S	CP ₁ to CP ₂ Setup Time ¹	30			ns	
t_H	Hold Time	0			ns	
t_{rec}	Recovery Time, PL to CP	45			ns	

¹ The role of CP₁ and CP₂ in an application may be interchanged.

DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the PL pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

AC WAVEFORMS

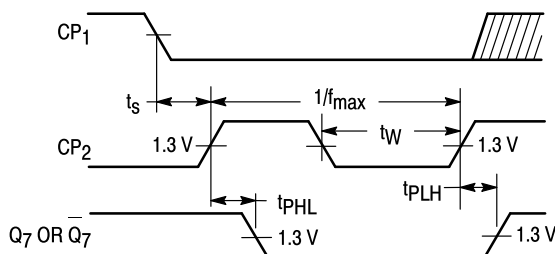


Figure 1

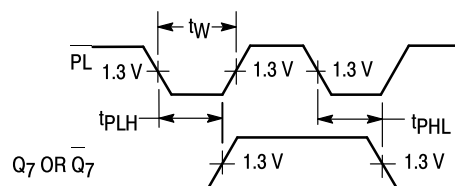


Figure 2

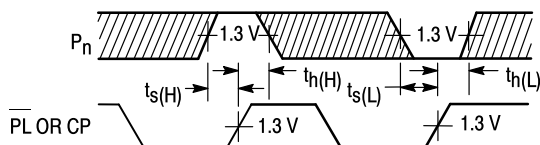


Figure 3

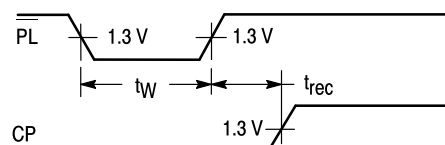
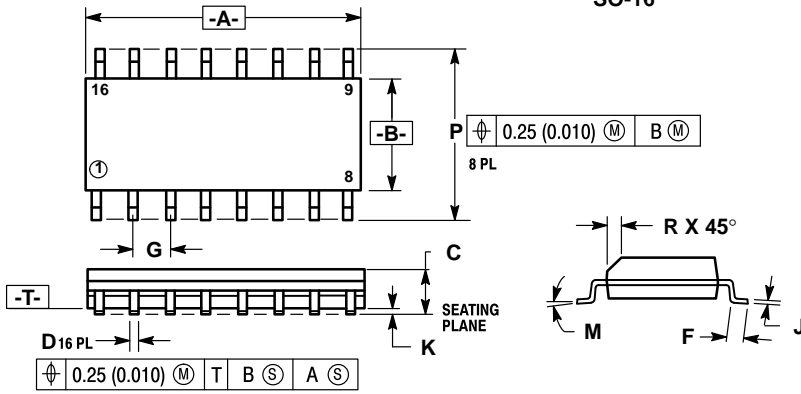


Figure 4

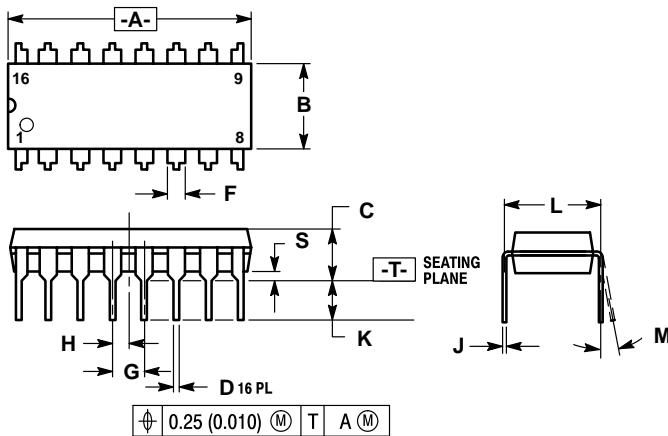
**Case 751B-03 D Suffix
16-Pin Plastic
SO-16**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

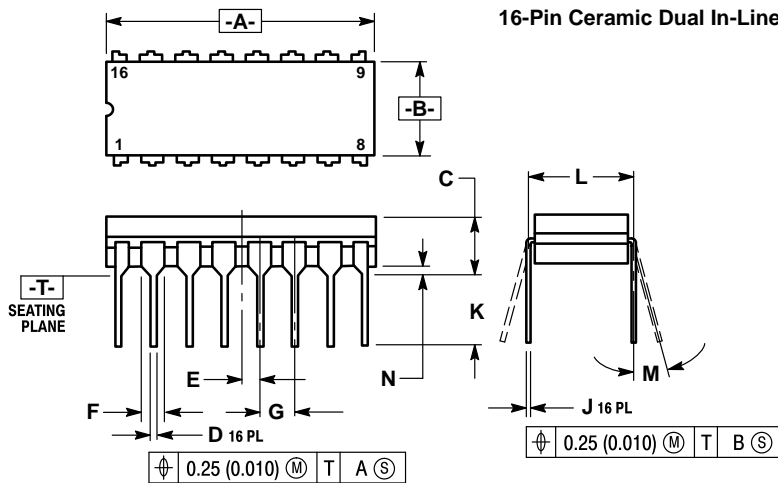
**Case 648-08 N Suffix
16-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.
 6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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