Contents

1. General Description

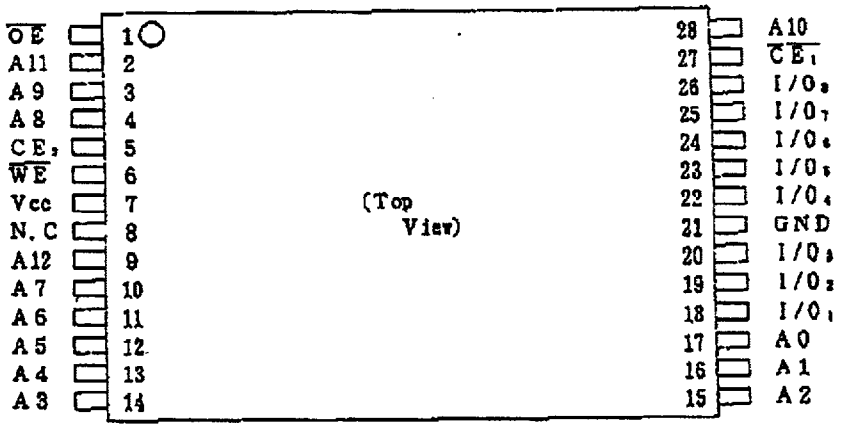
LH5168VT is a static RAM organized as 8,192word×8bit fabricated with a CMOS silicon gate process.
It's main features include:

Features

○Access time		200ns (MAX.)
○Current consumption	Operating	45mA (MAX.)
		10mA (t_{RC}, t_{WC}=1μs)
	Standby	1.0μA (MAX.)
	Data retention	0.2μA (V_{CC}=3V, Ta=25℃)
○Wide operating voltage range		2.7V~5.5V

○Fully static operation
○All input/output TTL compatible
○Three-state output
○Not designed or rated as radiation hardened
○28pin TSOP (TSOP28-P-0813) plastic package
○P-type bulk silicon
○Operating temperature is −10℃ to 70℃

2. Pin Configuration



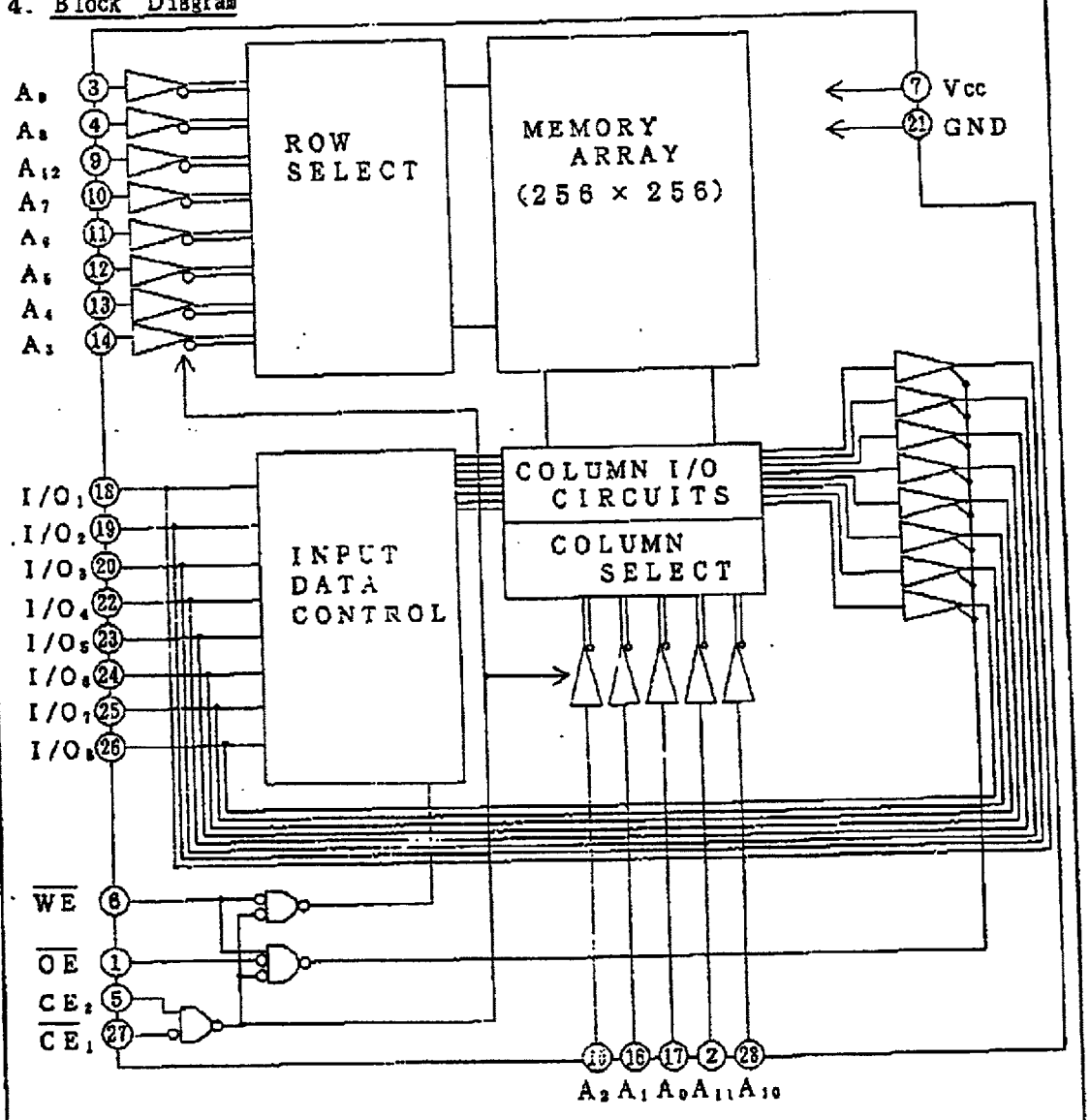
Pin Name	Signal
A_0 to A_{12}	Address input
$\overline{CE}_1$/CE_2	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground
N.C.	Non connection

3. Operating Mode

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	*	Standby	High impedance	Standby (I_{SB})
*	L	*	*			
L	H	L	*	Write	Data input	Operating (I_{CC})
L	H	H	L	Read	Data output	Operating (I_{CC})
L	H	H	H	Output disable	High impedance	Operating (I_{CC})

(* = H or L)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.3 to +7.0	V
Input voltage (*1)	V_{IN}	−0.3 (*2) to V_{CC}+0.3	V
Operating temperature	Topr	−10 to +70	℃
Storage temperature	Tstg	−65 to +150	℃

Note) *1. Maximum applicable voltage on any pin with respect to GND.
*2. -3.0V for pulse width≤50ns.

6. Recommended DC Operating Conditions

(T_a=−10℃ to +70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7		5.5	V
Input voltage	V_{IH}	V_{CC}−0.5		V_{CC}+0.3	V
(V_{CC}=2.7 to 3.6V)	V_{IL}	−0.3 (*3)		0.2	V
Input voltage	V_{IH}	2.2		V_{CC}+0.3	V
(V_{CC}=4.5 to 5.5V)	V_{IL}	−0.3 (*3)		0.8	V

Note) *3. -3.0V for pulse width≤50ns.

7. DC Electrical Characteristics

(T_a=−10℃ to +70℃, V_{CC}=2.7V to 5.5V)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}		−1.0	1.0	μA
Output leakage current	I_{LO}	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0 to V_{CC}		−1.0	1.0	μA
Operating Supply current	I_{CC}	$\overline{CE_1}$=0.2V, V_{IN}=0.2V or V_{CC}−0.2V, CE_2=V_{CC}−0.2V, Output open, V_{CC}=2.7V to 3.6V	t_{CYCLE}=200ns		20	mA
			t_{CYCLE}=1.0μs		8	
		$\overline{CE_1}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, CE_2=V_{IH}, Output open, V_{CC}=4.5V to 5.5V	t_{CYCLE}=200ns		45	
			t_{CYCLE}=1.0μs		10	
Standby current	I_{SB}	CE_2≦0.2V or $\overline{CE_1}$≧V_{CC}−0.2V (*4)	V_{CC}=2.7V to 3.6V		0.6	μA
			V_{CC}=4.5V to 5.5V		1.0	
	I_{SB1}	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}			5	mA
Output voltage	V_{OL}	I_{OL}=500μA, V_{CC}=2.7V to 3.6V			0.4	V
		I_{OL}=2.1mA, V_{CC}=4.5V to 5.5V			0.4	
	V_{OH}	I_{OH}=−500μA, V_{CC}=2.7V to 3.6V		V_{CC}−0.5		V
		I_{OH}=−1.0mA, V_{CC}=4.5V to 5.5V		2.4		

Note) *4. CE_2 should be ≧V_{CC}−0.2V or ≦0.2V.

8. AC Electrical Characteristics

Test Condition of AC Characteristics

Input pulse level	0.2V to V_{CC}−0.2V
Input rise/fall time	10ns
Input/Output timing level	1.5V
Output load	C_L (100pF) (*5)

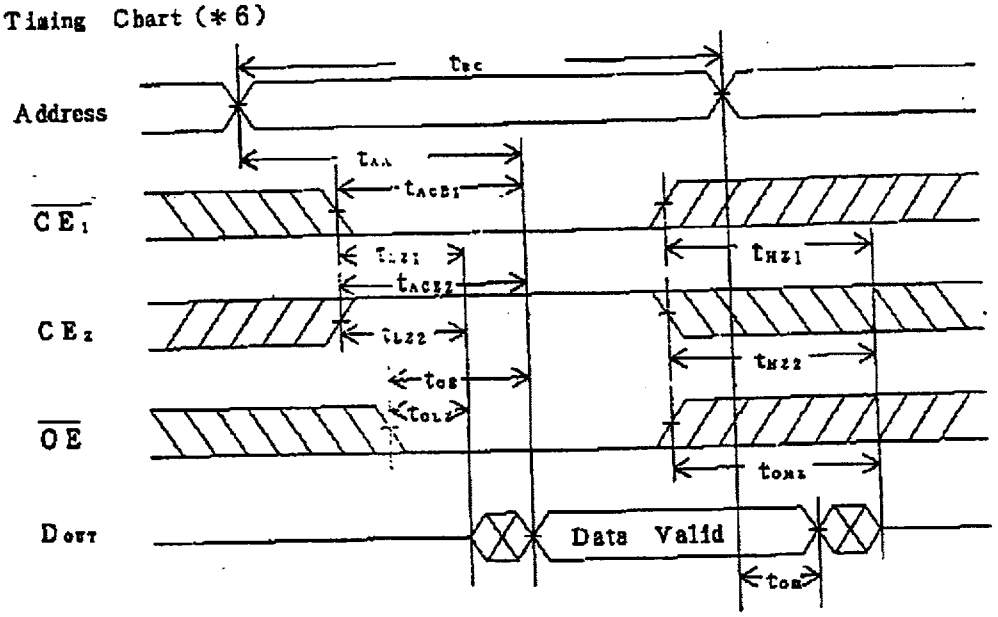
Note) *5. Including scope and jig capacitance.

Read cycle

(T_a = −10℃ to +70℃, V_{CC} = 2.7V to 5.5V)

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	200		ns
Address access time	t_{AA}		200	ns
$\overline{CE_1}$ access time	t_{ACS1}		200	ns
CE_2 access time	t_{ACS2}		200	ns
Output enable access time	t_{OE}		150	ns
Output hold time	t_{OH}	10		ns
$\overline{CE_1}$ Low to output in Low impedance	t_{LZ1}	20		ns
CE_2 High to output in Low impedance	t_{LZ2}	20		ns
$\overline{OE}$ Low to output in Low impedance	t_{OLZ}	10		ns
$\overline{CE_1}$ high to output in High impedance	t_{HZ1}	0	60	ns
CE_2 Low to output in High impedance	t_{HZ2}	0	60	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	40	ns

Timing Chart (*6)



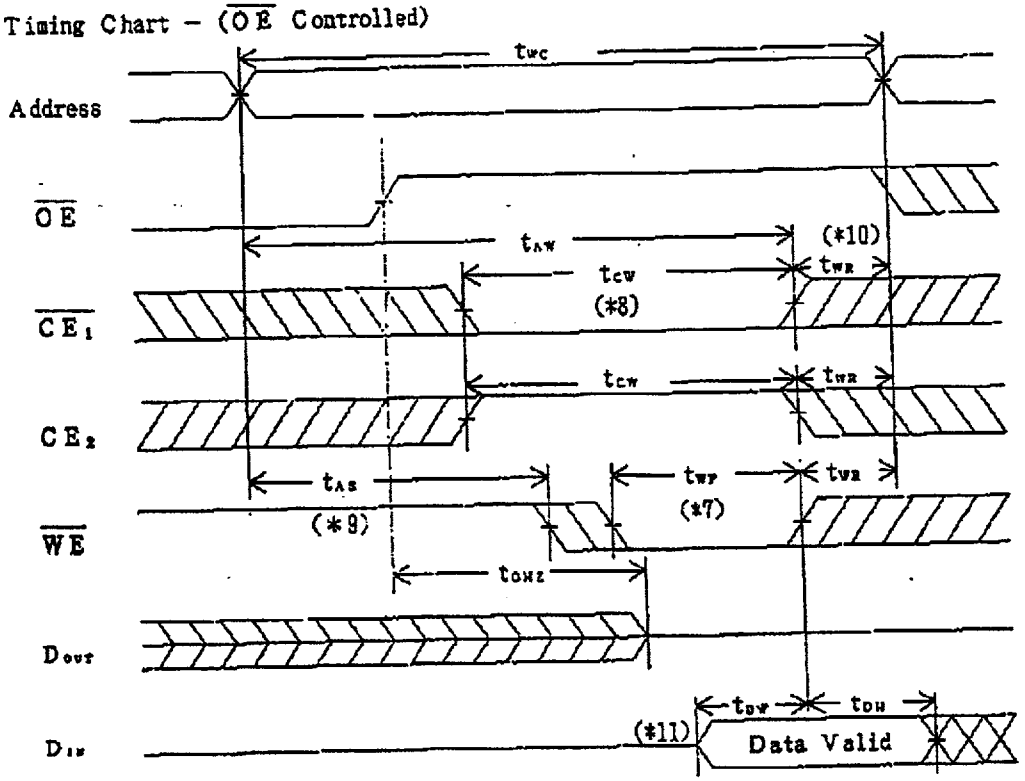
Note)*6. $\overline{WE}$ is 'High' level during the read cycle.

Write cycle

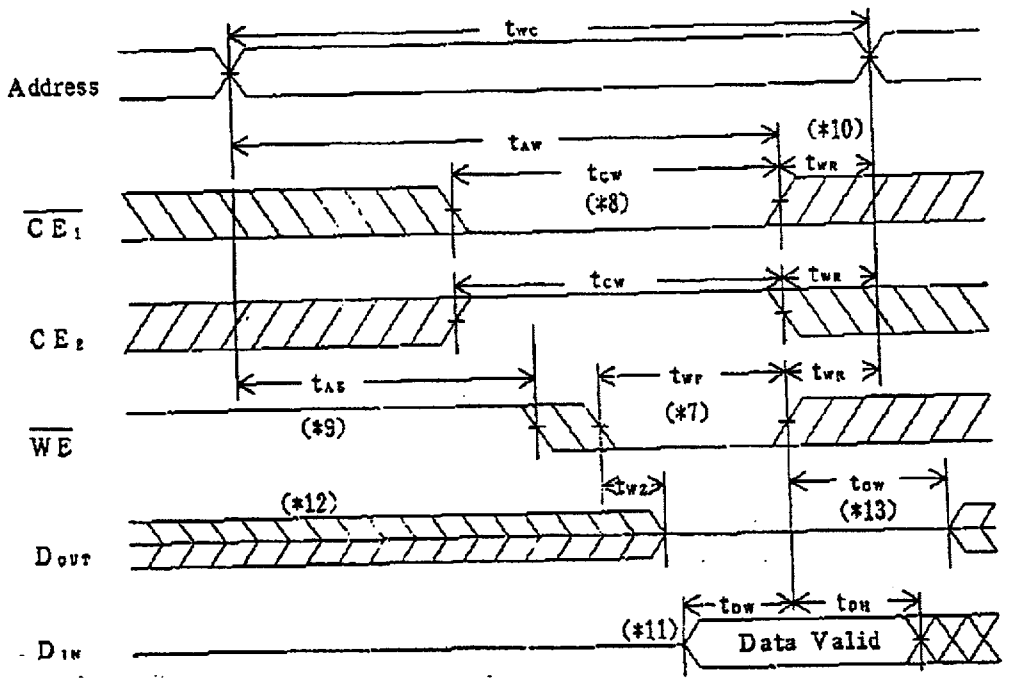
(T_a = −10℃ to +70℃, V_{CC} = 2.7 V to 5.5 V)

Parameter	Symbol	Min.	Max.	Unit
Write cycle time	t_{WC}	200		ns
$\overline{CE}$ Low to end of write	t_{CW}	180		ns
Address valid to end of write	t_{AW}	180		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	0		ns
Input data setup time	t_{DW}	100		ns
Input data hold time	t_{DH}	0		ns
$\overline{WE}$ High to output in Low impedance	t_{OW}	20		ns
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	60	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	40	ns

Timing Chart – ($\overline{OE}$ Controlled)



Timing Chart – ($\overline{OE}$ Low fixed)



Note) * 7. The writing occurs during a overlapping period of $\overline{CE_1}$='Low', CE_2='High' and $\overline{WE}$='Low' (t_{WP}).

* 8. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ Low transition or CE_2 High transition, to the time when the writing is finished.

* 9. t_{AS} is defined as the time from address change to writing start.

*10. t_{WR} is defined as the time from writing finish to address change.

*11. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

*12. If $\overline{CE_1}$ Low transition or CE_2 High transition occurs at the same time or after $\overline{WE}$ Low transition, the outputs will remain High impedance.

*13. If $\overline{CE_1}$ High transition or CE_2 Low transition occurs at the same time or before $\overline{WE}$ High transition, the outputs will remain High impedance.

9. Data Retention Characteristics

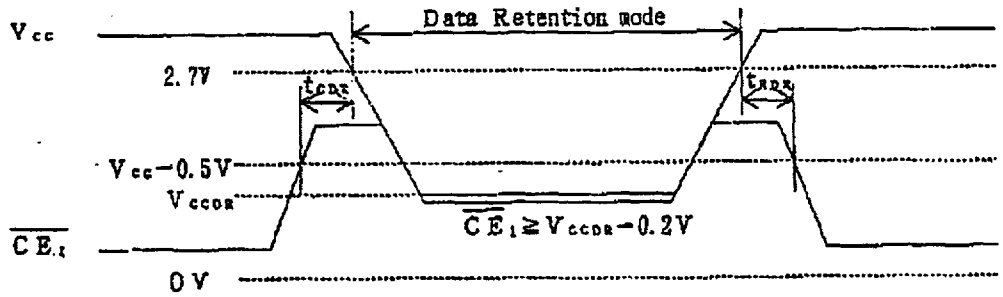
(Ta=−10℃ to +70℃)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$CE_2 \leq 0.2V$ or $\overline{CE_1} \geq V_{CCDR}-0.2V$ (*14)		2.0		V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=3V$	Ta=25℃		0.2	μA
		$CE_2 \leq 0.2V$ or	Ta=40℃		0.4	μA
		$\overline{CE_1} \geq V_{CCDR}-0.2V$ (*14)			0.6	μA
Chip enable setup time	t_{CDR}			0		ns
Chip enable hold time	t_{RDR}			(*15) t_{RC}		ns

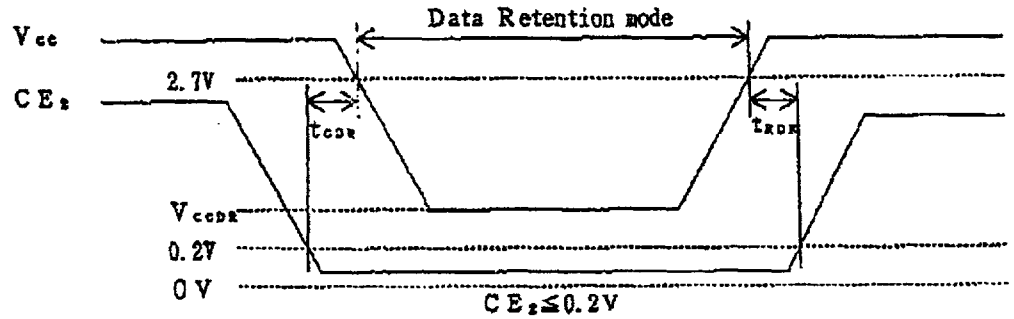
Note) *14. $CE_2 \geq V_{CCDR}-0.2V$ or $CE_2 \leq 0.2V$

*15. Read cycle time

Timing Chart−[$\overline{CE_1}$ Controlled] (*16)



Timing Chart−[CE_2 Contorolled]



Note) *16. To control the data retention mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} and $V_{CCDR}-0.2V$ or 0V and 0.2V during the data retention mode.

10. Pin Capacitance

(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN}=0V			7	pF	*17
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V			10	pF	*17

Note) *17. This parameter is sample and not 100% tested.

11 Package and packing specification

1. Package Outline Specification

Refer to drawing No. AA1068

2. Markings

2－1. Marking contents

(1) Product name : LH5168VT

(2) Company name : SHARP

(3) Date code

(Example) YY WW ×××

- YY: Indicates the product was manufactured in the WWth week of 19YY.
- WW: Denotes the production week. (01,02,03,・・・・・52,53)
- ××× : Denotes the production ref. code(1~3)
- YY: Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer drawing No. AA1068

(This layout do not define the dimensions of marking character and marking position.)

3. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

3－1. Soldering conditions (The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1~4℃/second	IC surface
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

3－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less

(2) Washing time : Total 1 minute maximum

(3) Solvent temperature : 15~40℃

ISSUE DATE	'94.07.29	T. Maeda	Y. Tohda	M. Uchida	(NOTE)
ISSUE NUMBER	R40729-27				
S/C NUMBER	LH5168V2				(DOCUMENT No. 1068-EDE)

4. Packing Specification (Embossed Carrier Taping Specification)

This standard apply to the embossed carrier taping specification for ICs to be delivered from SHARP CORPORATION. SHARP's embossed carrier taping specification are generally based on those set forth by the Japanese Industrial Standard JIS C 0806 and the EIA481A.

4 – 1. Tape Structure

- Embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and covered with a top covering tape to enclose them.

4 – 2. Taping Reel and Embossed Carrier Tape Size

- For the taping reel and embossed carrier tape sizes, refer to the attached drawings (NO.CV674 and CV521)

4 – 3. IC Package Enclosure in Embossed Carrier Tape

- The IC package enclosure direction in the embossed portion as it compares to the direction in which the tape is pulled is indicated by an index mark on package (Index mark indicate the NO.1 pin on package) in the attached drawing (NO. CV522).

4 – 4. Missing IC Packages inside Embossed Carrier Tape

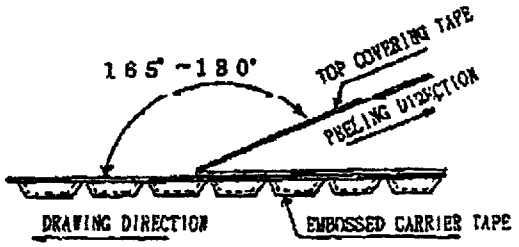
- The number of missing IC packages inside the embossed carrier tape should not exceed 0.1% of the total enclosed in the tape per reel, or 1, Whichever may be larger. There should never be more than two consecutive missing IC package.

4 – 5. Tape Joints

- The embossed carrier tape should not have more than one joint per reel.

4 – 6. Peeling Strength of the Top Covering Tape

- Peeling strength must meet the following conditions.
  1) Peeling angle
     at 165° to 180°
  2) Peeling speed
     at 300mm/min.
  3) Peeling strength
     at 0.2 to 0.7N(20 to 70gf)



4－7. Packing

- The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, shall be held in place with paper adhesive tape exceeding 30mm in length.
- The leading and trailing edges of the embossed carrier tape shall be left empty (with embossed portions not filled with IC packages), in the attached drawing (NO. CV522).
- The number of IC packages enclosed in the embossed carrier tape per reel shall, in principle, be as listed below.

Package Type	Number of IC Packages/Reel
SOP14-P-225	2,500 pcs
SOP16-P-225	2,500 pcs
SOP24-P-450	1,500 pcs
SOP28-P-450	1,000 pcs
SOP32-P-525	1,000 pcs
SOP44-P-600	750 pcs
TSOP28-P-1218	1,000 pcs

4－8. Indications

- The following shall be indicated on the taping reel and the packing case.
  1)Part Number (Product Name)
  2)Storage Quantity
  3)Production Date
  4)Manufacture's Name (SHARP)

4－9. Protection While in Transit

Embossed carrier tape should be free from deformed IC leads and deterioration in electrical characteristics.

5. Packing Specification (Dry packing for surface mount packages)

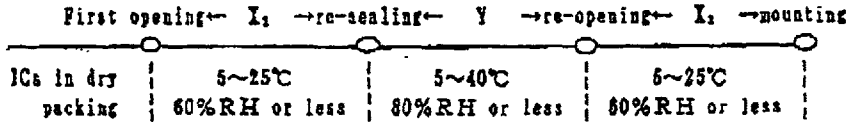
Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip,lead frame) this moisture may suddenly vaporise into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages. Please conform to the following conditions concerning the storage and opening of dry packing.

5－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

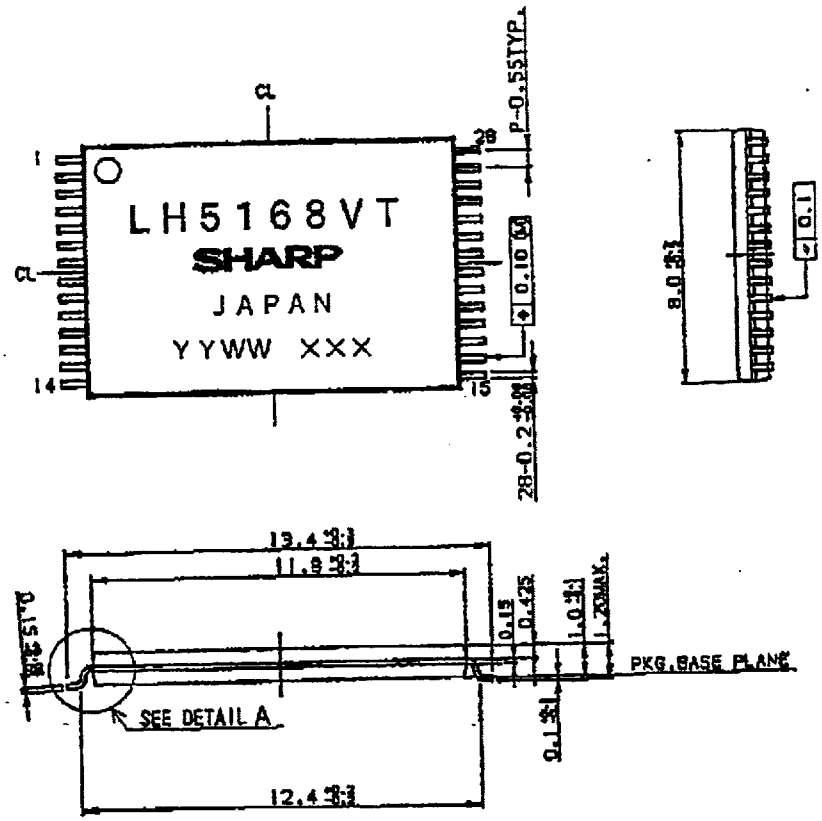
5－2. Notes on opening the dry packing
Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.

5－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 3 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whose indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 3 days, and store the ICs in the same environment as section 5-3.(1).



X_1+X_2 : within 3 days
Y : within 2 weeks

5－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 5－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃ or 5～10 hours at 150℃. Note that the embossed carrier tape can not be baked at the above temperature. Please transfar ICs to heat resistant carrier.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 5-3.(1).



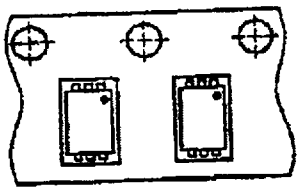
名称 NAME	TSOP28-P-0813	リード仕上 LEAD FINISH	TIN-LEAD PLATING	単位 UNIT	mm
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP		DRAWING NO.	AA1068		

備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
NOTE Plastic body dimensions do not include burr of resin.

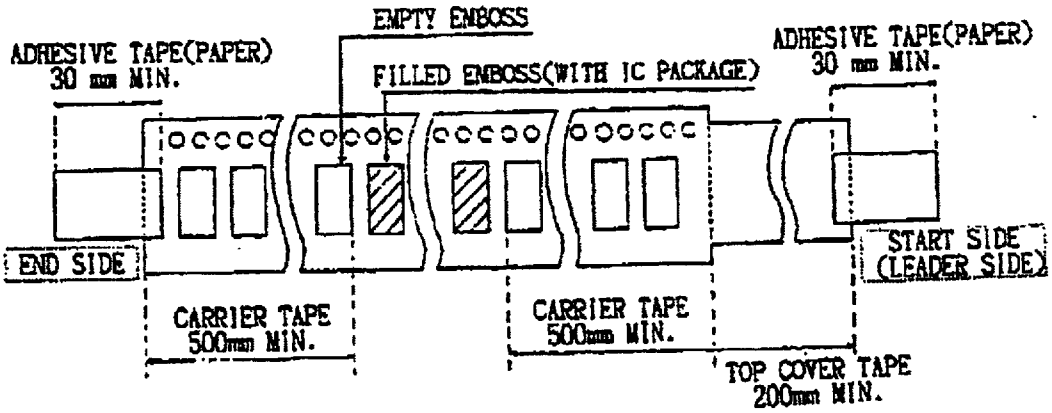
EMBOSS TAPING TYPE

IC TAPING DIRECTION

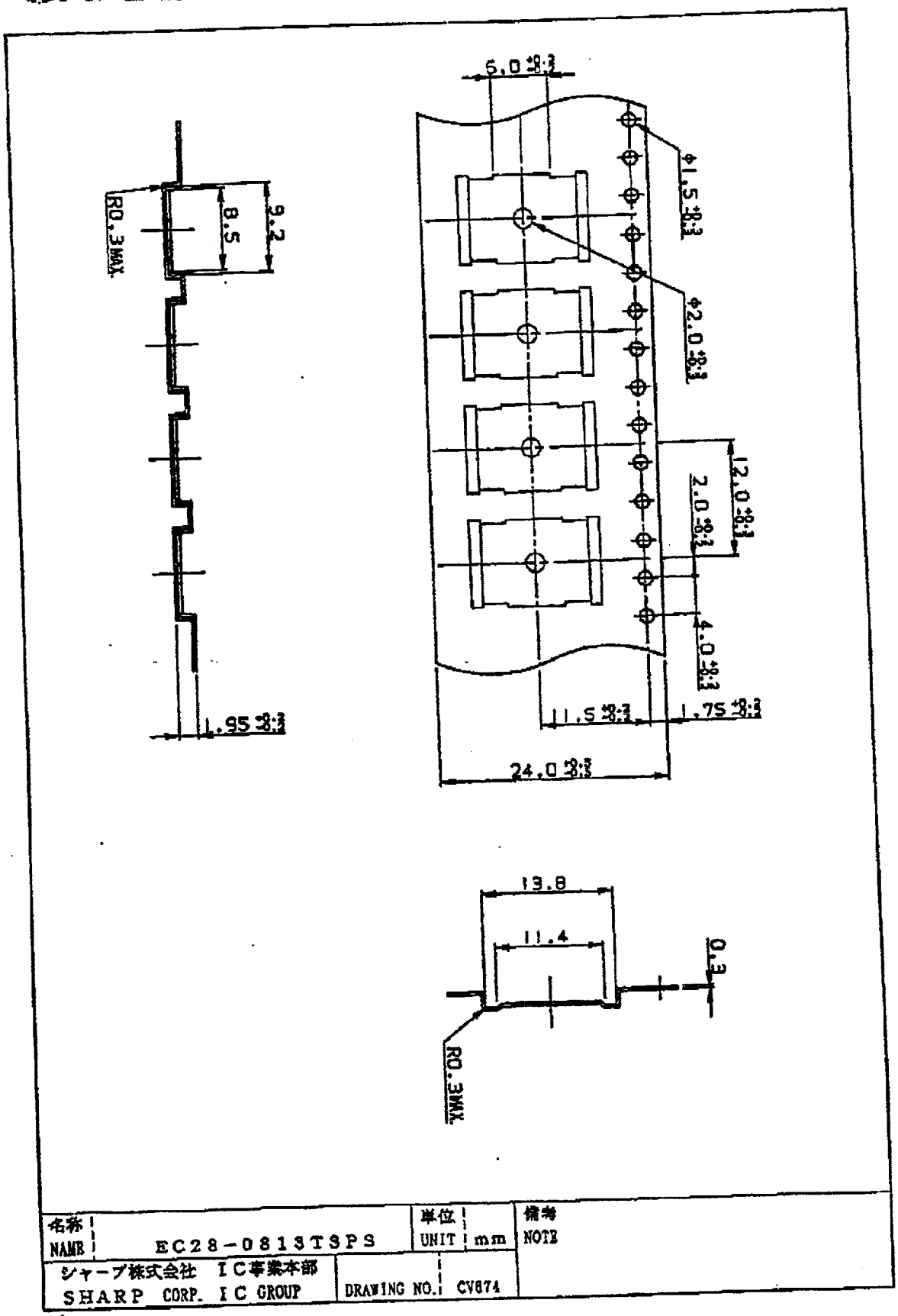
THE DRAWING DIRECTION OF TAPE →



LEADER SIDE AND END SIDE OF TAPE

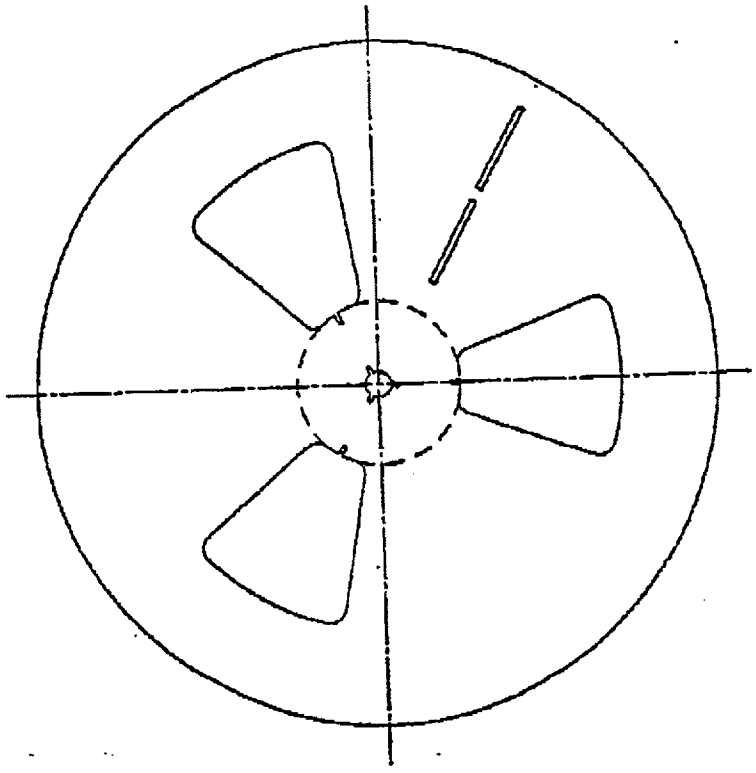


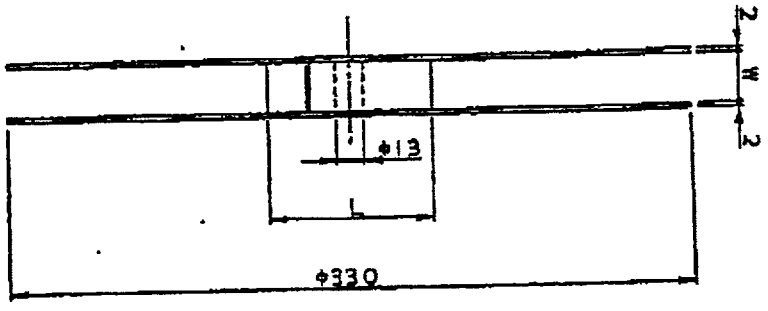
名称 NAME	EMBOSS TAPING TYPE	単位 UNIT	mm	備考 NOTE
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP		DRAWING NO.	CV622	



名称 NAME	EC28-0813TSPS	単位 UNIT	mm
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP	DRAWING NO. CV874		

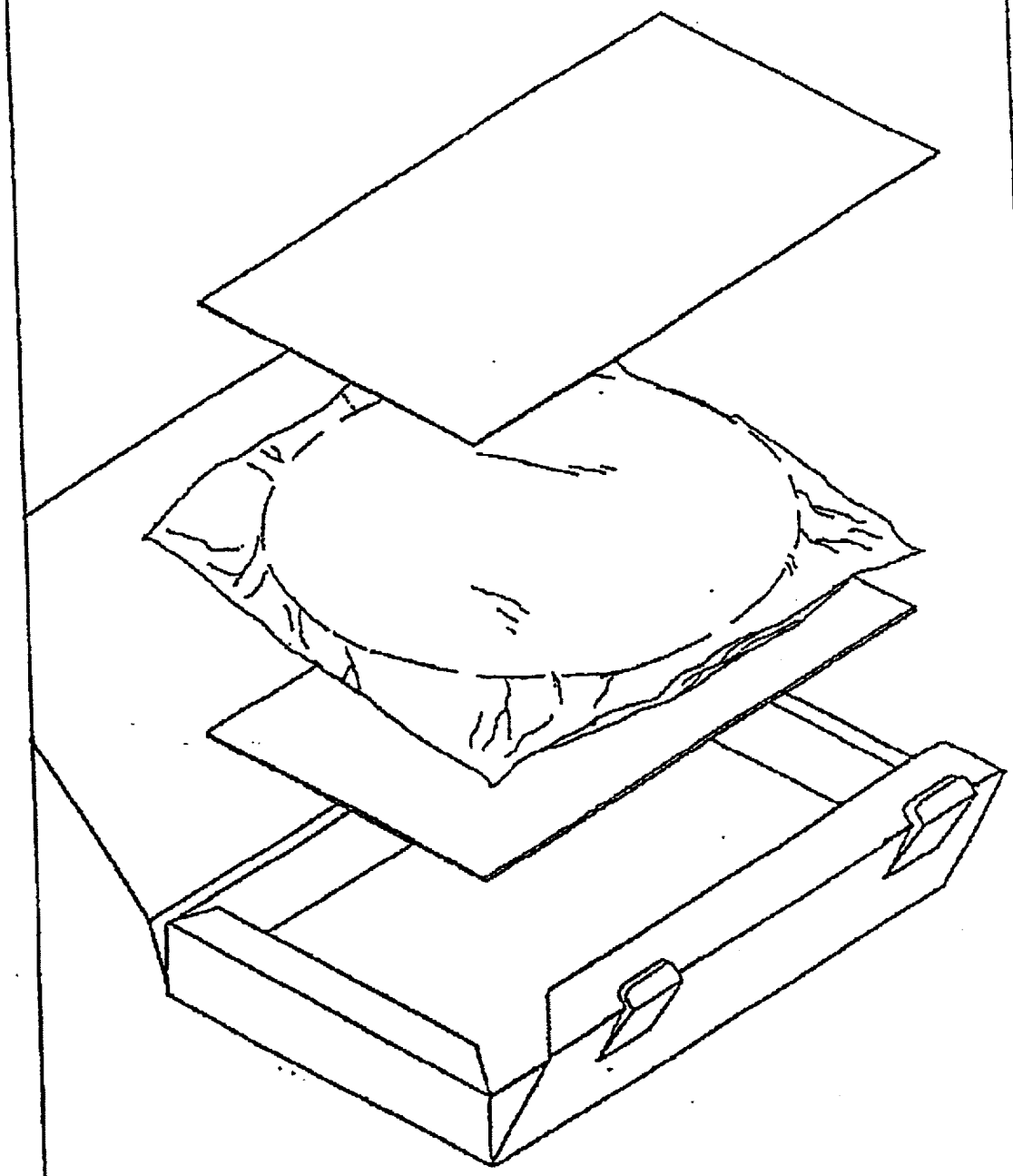
備考 NOTE





PKG	W (mm)	L (mm)	REEL NUMBER
SOP14-P-225	16.4	φ80	ECR16
SOP16-P-225	〃	〃	〃
SOP24-P-450	24.4	〃	ECR24
SOP28-P-450	〃	〃	〃
SOP32-P-525	32.4	φ100	ECR32
SOP44-P-600	44.8	φ100	ECR44-H
TSOP28-P-0813	24.4	φ100	ECR24-100

名称 NAME	REEL FOR EMBOSS CARRIER TAPING	単位 UNIT	mm
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP	DRAWING NO.	CV521	備考 NOTE



CASE SIZE : 345×345×55 (mm)

名称 NAME	EXTERNAL APPEARANCE OF PACKING CASE FOR EMBOSS CARRIER TAPING	単位 UNIT	mm
シャープ株式会社 IC事業本部 SHARP CORP. IC GROUP	DRAWING NO.	BJ279	備考 NOTE