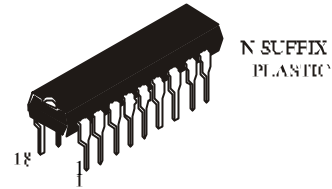**ILA1068**

Versatile Telephone Transmission Circuit with Dialler Interface

The ILA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 KΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 KΩ) for electret microphone
- Dual-Tone Multi-Frequency (DTMF) signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current-dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

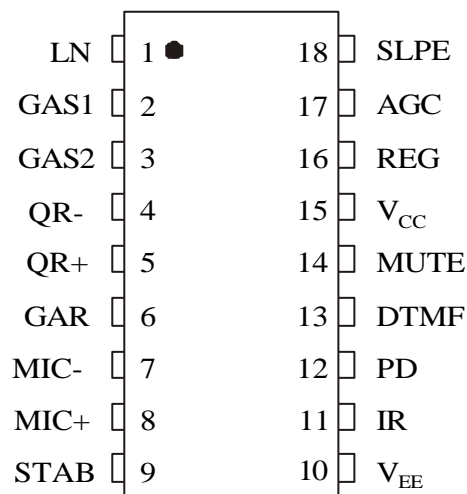N SUFFIX
PLASTIC

ORDERING INFORMATION
ILA1068N   Plastic DIP

T_A = -25° to 75° C
for package

BLOCK DIAGRAM
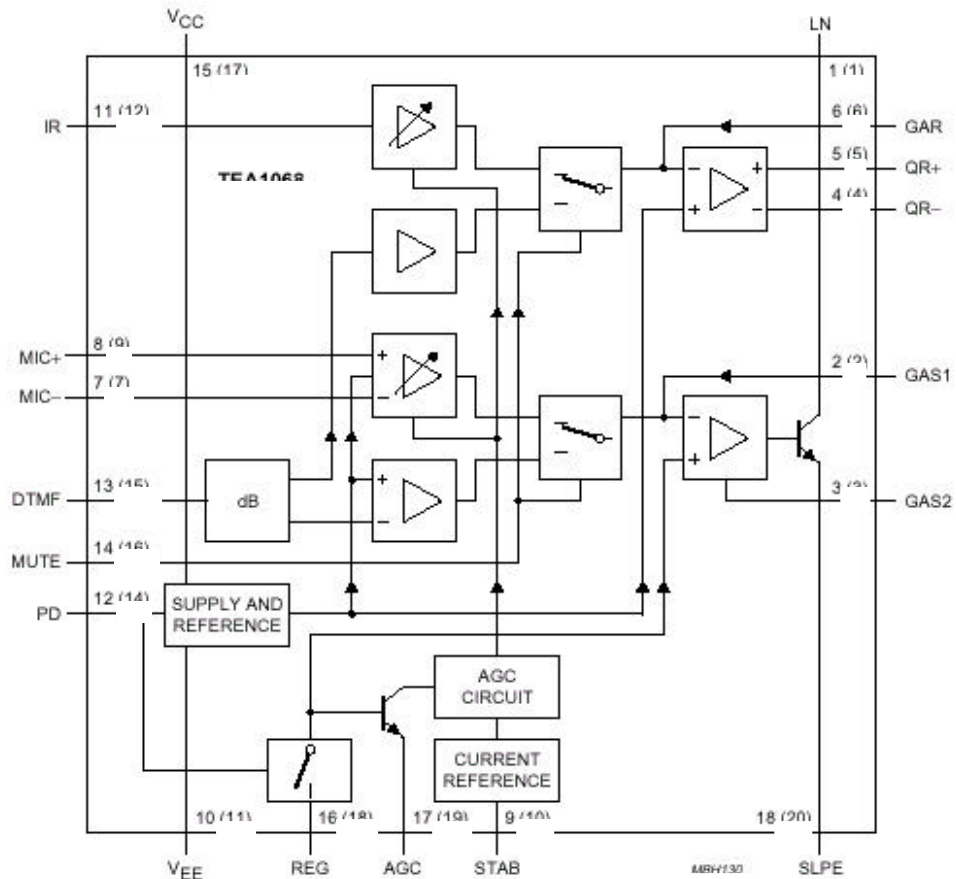
PIN DESCRIPTION

Pin No	Designation	Description
1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR-	inverting output receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MIC-	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

PIN ASSIGNMENT

|		
LN	1	18 SLPE
GAS1	2	17 AGC
GAS2	3	16 REG
QR-	4	15 V_{CC}
QR+	5	14 MUTE
GAR	6	13 DTMF
MIC-	7	12 PD
MIC+	8	11 IR
STAB	9	10 V_{EE}

INTEGRAL

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The ILA1068 develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits, e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}; the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

An internal current stabilizer is set by a resistor of 3.6 KΩ between the current stabilizer pin STAB and V_{EE} (see Fig.1).
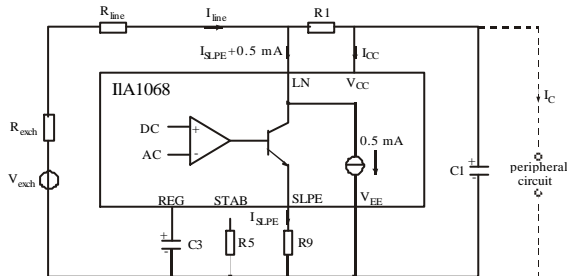
Figure 1. Supply arrangement

If the line current I_{line} exceeds the current $I_{CC} + 0.5$ mA required by the circuit itself (approximately 1mA) plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The regulated voltage on the line terminal ($V_{LN)}$ can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

$$V_{LN} = V_{ref} + ((I_{line} - I_{CC} - 0.5 \times 10^3) - I_p) \times R9,$$

where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level, the maximum output swing on LN and the DC characteristics (especially at lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5$ mA $+$ Ip , the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range, the dynamic impedance is largely determined by R1 (see Fig.2).

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor, connected between LN and REG, will decrease the internal reference voltage; when connected between REG and SLPE, it will increase the internal reference voltage. Current (Ip) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current.
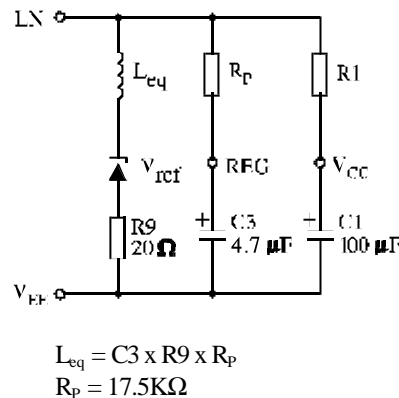
$$L_{eq} = C3 \times R9 \times R_P$$
$$R_P = 17.5 K\Omega$$

Figure 2. Equivalent impedance circuit

Microphone inputs MIC+ and MIC- and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 KΩ (2 x 32 KΩ) and its voltage gain is typically 52 dB (when R7 = 68 KΩ, see Figure 5). Dynamic, magnetic, piezo-electric or electret (with built-in FET source followers) can be used.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of R7 connected between GAS1 and GAS2. An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone and the receiving amplifier inputs.
A LOW level or an open circuit has the reverse effect. MUTE switching causes only negligible clicks at the earpiece outputs and on the line.

Dial-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 KΩ) and varies with R7 in the same way as the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR-, QR+ and GAR

The receiving amplifier has one input (IR) and two complementary outputs, a non-inverting output QR+ and an inverting output QR-. These outputs may be used for single-ended or for differential drive depending on the sensitivity and type of earpiece used. Gain from IR to QR+ is typically 25 dB (when R4 = 100 KΩ). This is sufficient for low-impedance magnetic or dynamic microphones, which are suited for single-ended drive. By using both outputs (differential drive), the gain is increased by 6dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak to RMS value is higher.

The receiving amplifier gain can be adjusted between 17 dB and 33 dB with single-ended drive and between 26 dB and 39 dB with differential drive to suit the sensitivity of the transducer used. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subtracting the anti-side-tone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 = 100 pF and C7 = 10 x C4 = 1nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The 'cut-off' frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}.

The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current.

The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Table 1). Different values of R6 give the same ratio of line currents for start and end of the control range. If automatic line loss compensation is not required, AGC may be left open. The amplifiers then all give their maximum gain as specified.

Table 1 Values of resistor R6 for optimum line-loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

$V_{exch}(V)$	400 $R_{exch}(\Omega)$	600 $R_{exch}(\Omega)$	800 $R_{exch}(\Omega)$	1000 $R_{exch}(\Omega)$
	R6(KΩ)			
24	61.9	48.7	-	-
36	100	78.8	68	60.4
48	140	110	93.1	82
60	-	-	120	102

Power-Down input (PD)

During pulse dialling or register recall (timed loop break), the telephone line is interrupted. During these interruptions, the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input, which reduces the typical supply current from 1mA to 55 mA and switches off the voltage regulator, thus preventing discharge through LN. When PD is HIGH, the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required, PD may be left open-circuit.

Side-tone suppression

The anti-side-tone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig.5) suppress the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times \left(R3 + R8//Z_{line} \right) \quad (1)$$

$$\frac{Z_{bal}}{Z_{bal} + R8} = \frac{Z_{line}}{Z_{line} + R1} \quad (2)$$

It fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled when $|R8//Z_{bal}| <<R3$.

To obtain optimum side-tone suppression, condition (2) has to be fulfilled which results in:

$$Z_{bal} = \frac{R8}{R1} Z_{line} = k \times Z_{line}$$

Where k is a scale factor; $k = \dfrac{R8}{R1}$

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

• compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}

• $|Z_{bal} // R8| <<R3$ fulfilling condition (1) and thus ensuring correct anti-side-tone bridge operation

• $|Z_{bal} + R8| >>R9$ to avoid influencing the transmit gain.

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.
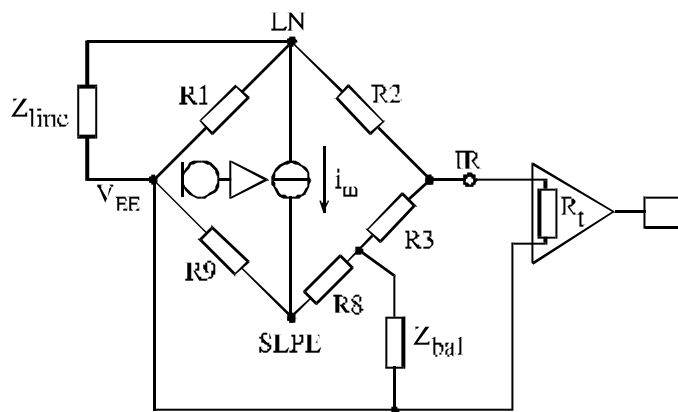

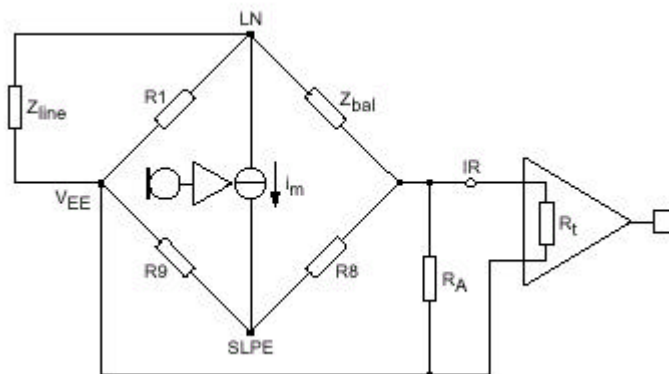**Figure 3. Equivalent circuit of ILA1068 anti-side-tone bridge**

Figure 4. Equivalent circuit of an anti-side-tone network in a Wheatstone bridge configuration.

MAXIMUM RATINGS*

Symbol	Parameter	Condition	Min	Max	Unit
I_{line}	Line current	Input 01	-	140	mA
Tstg	Storage temperature		-40	+85	°C
T_L	Lead Temperature, 1.0 mm from Case for 4 Seconds			265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
I_{line}	Operating line current normal operation		10	140	mA
A_{U1}	Voltage gain microphone amplifier	ILA1068A ILA1068B	51 45.5	53 59	dB
A_{U2}	Voltage gain multi-frequency	ILA1068A ILA1068B	24.5 18.5	26.5 32.5	dB
A_{U3}	Voltage gain receiving amplifier	ILA1068A ILA1068B	24 18	26 32	dB
T_{amb}	Operating ambient temperature		-25	+70	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND$\leq$(V_{IN} or V_{OUT})$\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Guaranteed Limits								Unit
			ILA1068AN				ILA1068BN				
			25°C		-25°C to 70°C		25°C		-25°C to 70°C		
			min	max	min	max	min	max	min	max	
V_{LN1}	Voltage Drop Over Circuit between LN and V_{EE}	V(12,14) = 0 V, I_{line} (01) = 5 mA I_{line} (01) = 15 mA I_{line} (01) = 100 mA I_{line} (01) = 140 mA	3.95 4.2 5.4 -	4.55 4.7 6.7 7.5	2.96 3.15 4.05 -	5.69 5.87 8.37 9.37	3.6 3.6 4.5 5.5	5.55 6.3 7.7 9.0	2.96 3.15 4.05 -	5.69 5.87 8.37 9.37	V
I_{CC1}	Supply Current	V(15) = 2.8 V, V(12,14) = 0 V	-	1.3	-	1.62	0.05	1.3	-	1.62	mA
I_{CC2}	Supply Current	V(12,15) = 2.8 V, V(14) = 0 V	-	82	-	84	-	82	-	84	µA
I	Feed current for the peripheral circuits	I_{line} (01) = 15 mA, V(14,15) = 2.2 V	1.8	5.2	1.35	-	1.8	5.2	1.35	-	mA
		I_{line} (01) = 15 mA, V(14,15) = 3.0 V	0.4	5.2	0.5	-	0.4	5.2	0.5	-	mA
A_{U1}	Voltage Gain MIC+ or MIC- to LN	I_{line} (01) = 15 mA, V(12,14) = 0 V	51	53	38.3	66.2	45.5	59	38.3	66.2	dB
A_{U2}	Voltage Gain from DTMF to LN	I_{line} (01) = 15 mA, V(12,14) = 0 V	24.5	26.5	18.4	33.1	18.5	32.5	18.4	33.1	dB
A_{U3}	Voltage Gain from IR to QR+ or QR-	I_{line} (01) = 15 mA, V(12,14) = 0 V	24	26	18	32.5	18	32	18	32.5	dB
V_{LN2}	Voltage Drop Over Circuit between LN and V_{EE} with External Resistor R_{VA}	I_{line} (01) = 15 mA, V(12,14) = 0 V, R_{VA} (REG to SLPE)=39 KΩ	4.65	5.35	3.5	6.7	4.25	5.65	3.5	6.7	V
		R_{VA} (LN to REG)=68 KΩ	3.45	4.1	2.6	5.0	3.15	4.4	2.6	5.0	
R_{I1}	Input Impedance differential between MIC- and MIC+	I_{line} (01) = 15 mA	51	77	38	96	51	77	38	96	KΩ

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R_{I2} R_{I3}	Input Impedance single-ended MIC- or MIC+ to V_{EE}	I_{line} (01) = 15 mA	8.0 58	16 78	- -	- -	8.0 58	16 78	- -	- -	KΩ

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Symbol	Parameter	Test Conditions	Guaranteed Limits								Unit
			ILA1068AN				ILA1068BN				
			25°C		-25°C to 70°C		25°C		-25°C to 70°C		
			min	max	min	max	min	max	min	max	
R_{I4}	Input Impedance (DTMF input)	I_{line} (01) = 15 mA	16.8	24.6	12.6	30.8	16.8	24.6	12.6	30.8	KΩ
R_{I5}	Input Impedance (Receiving Amplifier Input IR)	I_{line} (01) = 15 mA	17	25	12.75	31.25	17	25	12.75	31.25	KΩ
V_{O1}	Output Voltage	I_{line} (01) = 15 mA THD = 2% THD = 10%	1.9 2.1	- -	1.43 1.58	- -	1.9 2.1	- -	1.43 1.58	- -	V
V_{O2}	Output Voltage	I_{line} (01) = 15 mA THD = 2%	0.8	-	0.6	-	0.8	-	0.6	-	V
K_U	Voltage Gain	I_{line} (01) = 15 mA, V(12) = 3.5 V	-17	-21	-12.75	-26.25	-17	-21	-12.75	-26.25	dB
I_{PD}	Input Current	I_{line} (01) = 15 mA, V(14) = 3.5 V	0	10	0	12.5	0	10	0	12.5	µA
I_{MUTE}	Input Current	I_{line} (01) = 15 mA, V(14) = 3.5 V	-	15	-	18.75	-	15	-	18.75	µA
ΔA_U	Voltage Gain Reduction Between MIC+ and MIC- to LN	I_{line} (01) = 15 mA, V(14) = 2.8 V	70	-	70	-	-	-	-	-	dB

INTEGRAL
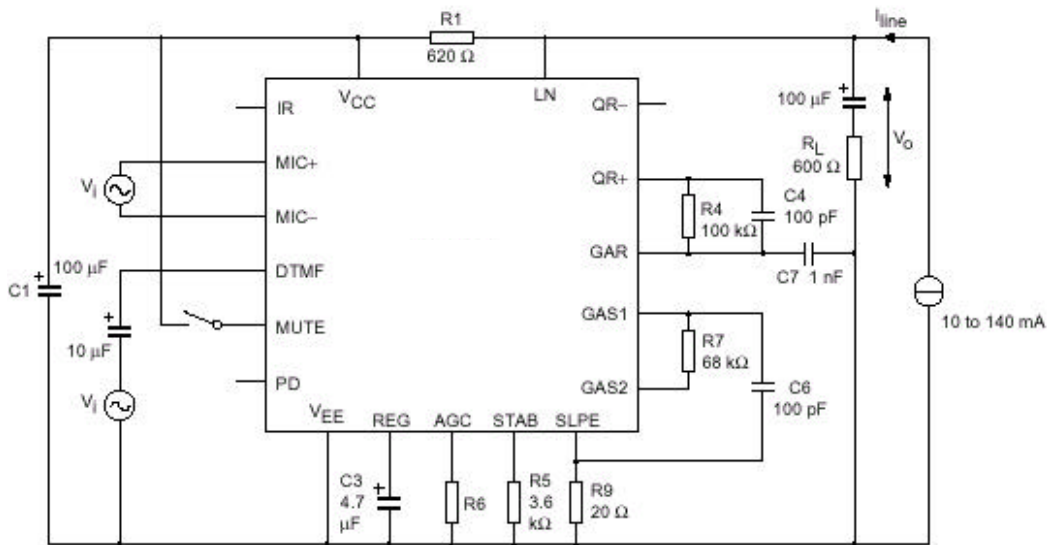
Voltage gain is defined as $G_V = 20 \log \left| \dfrac{V_O}{V_I} \right|$

For measuring gain from MIC+ and MIC- the MUTE input should be LOW or open. For measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open.

Figure 5. Test circuit for defining voltage gain of MIC+, MIC- and DTMF inputs.
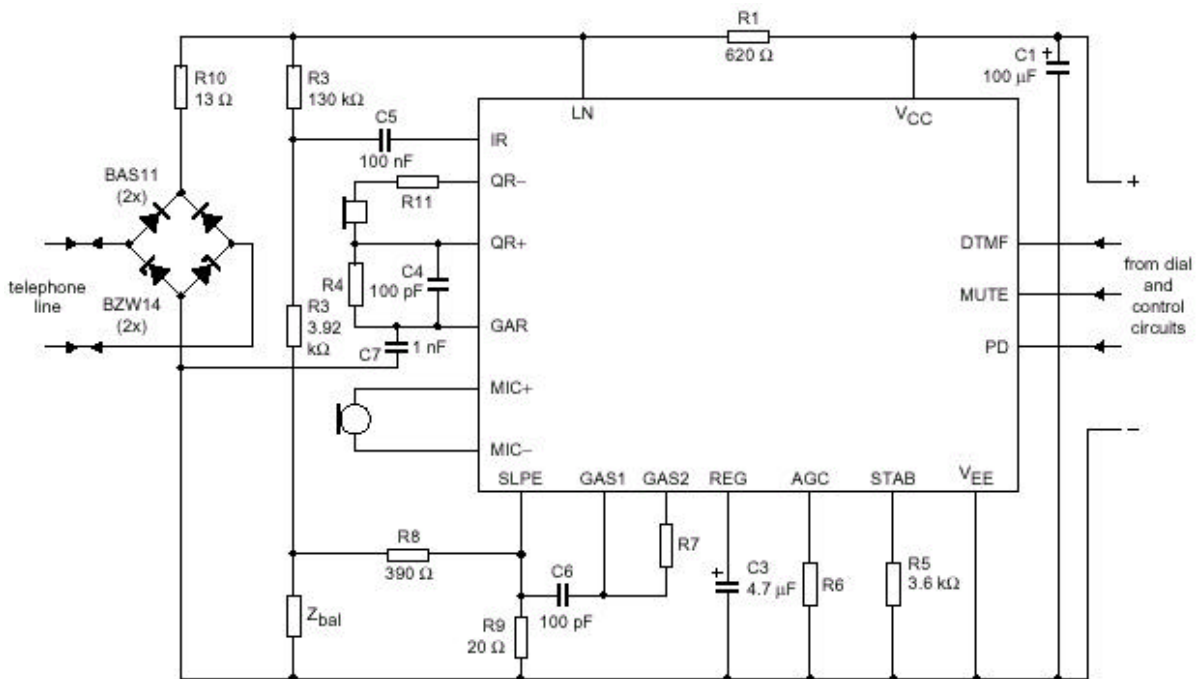
Typical application of the ILA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

Figure 6. Application diagram.

INTEGRAL

CHIP PAD DIAGRAM

Chip marking
14152

2.8 ± 0.02

(0,0)

3.2 ± 0.03

Y

X
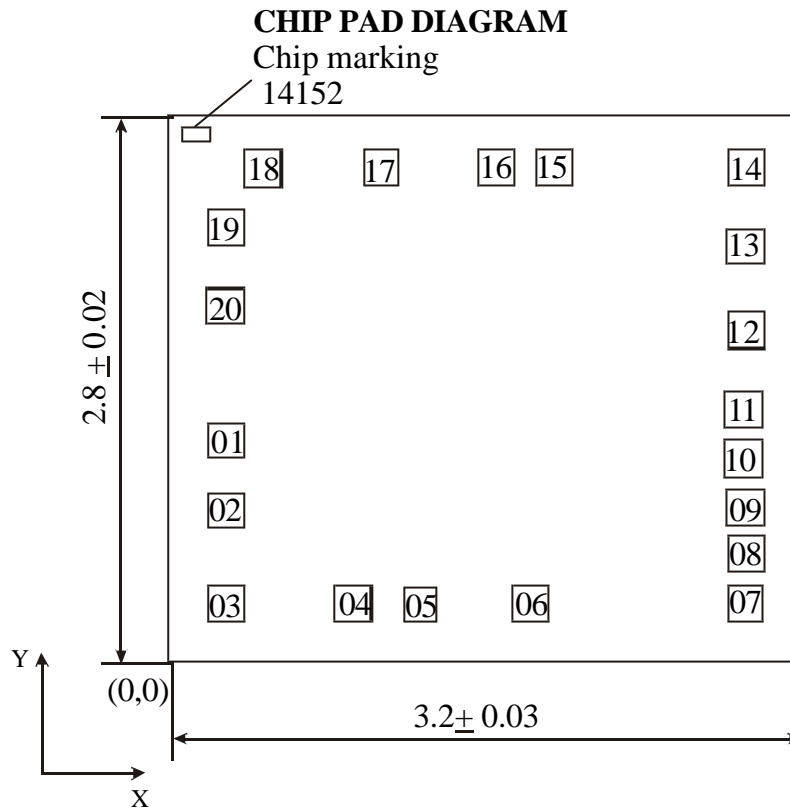
Location of marking (mm): left lower corner x=0.180, y=2.555.

Chip thickness: 0.46 ± 0.02 mm.

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	LN	0.268	1.133	0.140 x 0.140
02	GAS1	0.268	0.784	0.140 x 0.140
03	GAS2	0.268	0.284	0.140 x 0.140
04	QR-	0.804	0.284	0.140 x 0.140
05	QR+	1.068	0.284	0.140 x 0.140
06	GAR	1.708	0.284	0.140 x 0.140
07	MIC-	2.807	0.284	0.140 x 0.140
08	-	2.807	0.554	0.140 x 0.140
09	MIC+	2.807	0.738	0.140 x 0.140
10	-	2.807	1.075	0.140 x 0.140
11	STAB	2.807	1.293	0.140 x 0.140
12	V_{EE}	2.807	1.619	0.140 x 0.140
13	IR	2.807	1.911	0.140 x 0.140
14	PD	2.807	2.350	0.140 x 0.140
15	DTMF	1.825	2.350	0.140 x 0.140
16	MUTE	1.584	2.350	0.140 x 0.140
17	V_{CC}	1.086	2.350	0.140 x 0.140
18	REG	0.320	2.350	0.140 x 0.140
19	AGC	0.268	1.936	0.140 x 0.140
20	SLPE	0.268	1.686	0.140 x 0.140

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