Quad, 12-/14-/16-Bit *nano*DACs® with 5 ppm/°C On-Chip Reference

AD5624R/AD5644R/AD5664R

FEATURES

Low power, smallest pin-compatible, quad *nano*DACs
- **AD5664R: 16 bits**
- **AD5644R: 14 bits**
- **AD5624R: 12 bits**

User selectable external or internal reference
- **External reference default**
- **On-chip 1.25 V/2.5 V, 5 ppm/°C reference**

10-lead MSOP and 3 mm × 3 mm LFCSP_WD
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale
Per channel power-down
Serial interface, up to 50 MHz

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

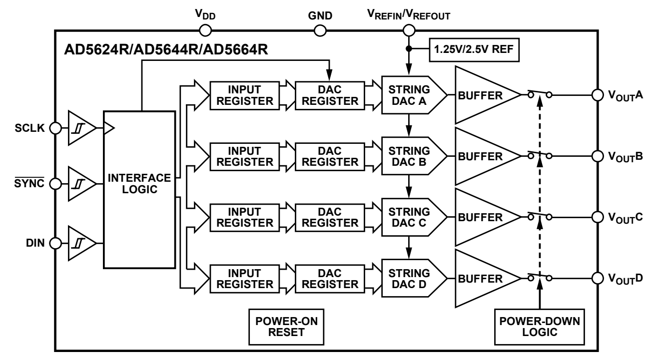

Figure 1.

Table 1. Related Devices

Part No.	Description
AD5624/AD5664	2.7 V to 5.5 V quad, 12-/16-bit DACs, external reference
AD5666	2.7 V to 5.5 V quad 16-bit DAC, internal reference, LDAC, CLR pins

GENERAL DESCRIPTION

The AD5624R/AD5644R/AD5664R, members of the *nano*DAC family, are low power, quad, 12-/14-/16-bit buffered voltage-out DACs. All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design.

The AD5624R/AD5644R/AD5664R have an on-chip reference. The AD56x4R-3 has a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD56x4R-5 has a 2.5 V, 5 ppm/°C reference giving a full-scale output range of 5 V. The on-chip reference is off at power-up allowing the use of an external reference and all devices can be operated from a single 2.7 V to 5.5 V supply. The internal reference is enabled via a software write.

The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place. The part contains a per-channel power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode. The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment.

The AD5624R/AD5644R/AD5664R use a versatile 3-wire serial interface that operates at clock rates up to 50 MHz, and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing.

PRODUCT HIGHLIGHTS

1. Quad 12-/14-/16-bit DACs.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 10-lead MSOP and 10-lead, 3 mm × 3 mm, LFCSP_WD.
4. Low power, typically consumes 1.32 mW at 3 V and 2.25 mW at 5 V.

Rev. A

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REVISION HISTORY

11/06—Rev. 0 to Rev A

4/06—Revision 0: Initial Version

SPECIFICATIONS

AD5624R-5/AD5644R-5/AD5664R-5

V_{DD} = 4.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE[2]					
AD5664R					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5644R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5624R					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±1	% of FSR	All ones loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale ; V_{DD} = 5 V ± 10%
DC Crosstalk (External Reference)		10		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		μV/mA	Due to load current change
		5		μV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		μs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE INPUTS					
Reference Current		170	200	μA	V_{REF} = V_{DD} = 5.5 V
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		26		kΩ	
REFERENCE OUTPUT					
Output Voltage	2.495		2.505	V	At ambient
Reference TC[3]		±5	±10	ppm/°C	MSOP package models
		±10		ppm/°C	LFCSP package models
Output Impedance		7.5		kΩ	

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
LOGIC INPUTS[3]					
Input Current			±2	μA	All digital inputs
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = 5 V
V_{INH}, Input High Voltage	2			V	V_{DD} = 5 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	4.5		5.5	V	
I_{DD} (Normal Mode)[4]					V_{IH} = V_{DD}, V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.45	0.9	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		0.95	1.2	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]					V_{IH} = V_{DD}, V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.48	1	μA	

[1] Temperature range: B grade: −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5664R (Code 512 to Code 65,024); AD5644R (Code 128 to Code 16,256); AD5624R (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization, not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down.

AD5624R-3/AD5644R-3/AD5664R-3

V_{DD} = 2.7 V to 3.6 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE[2]					
AD5664R					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5644R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5624R					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±1	% of FSR	All ones loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−100		dB	DAC code = midscale; V_{DD} = 3 V ± 10%
DC Crosstalk (External Reference)		10		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		μV/mA	Due to load current change
		5		μV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 3 V
Power-Up Time		4		μs	Coming out of power-down mode; V_{DD} = 3 V
REFERENCE INPUTS					
Reference Current		170	200	μA	V_{REF} = V_{DD} = 3.6 V
Reference Input Range	0		V_{DD}	V	
Reference Input Impedance		26		kΩ	
REFERENCE OUTPUT					
Output Voltage	1.247		1.253	V	At ambient
Reference TC[3]		±5	±15	ppm/°C	MSOP package models
		±10		ppm/°C	LFCSP package models
Output Impedance		7.5		kΩ	

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
LOGIC INPUTS[3]					
Input Current			±2	μA	All digital inputs
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = 3 V
V_{INH}, Input High Voltage	2			V	V_{DD} = 3 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		3.6	V	
I_{DD} (Normal Mode)[4]					V_{IH} = V_{DD}, V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.44	0.85	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		0.95	1.15	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]					V_{IH} = V_{DD}, V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.2	1	μA	

[1] Temperature range: B grade: −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5664R (Code 512 to Code 65,024); AD5644R (Code 128 to Code 16,256); AD5624R (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization, not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 4.

Parameter[2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time					
AD5624R		3	4.5	μs	¼ to ¾ scale settling to ±0.5 LSB
AD5644R		3.5	5	μs	¼ to ¾ scale settling to ±0.5 LSB
AD5664R		4	7	μs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/μs	
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB change around major carry
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-s	
Analog Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
DAC-to-DAC Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		μV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ (see Figure 2). $V_{DD} = 2.7$ V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 5.

Parameter	Limit at T_{MIN}, T_{MAX} $V_{DD} = 2.7$ V to 5.5 V	Unit	Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
t_2	9	ns min	SCLK high time
t_3	9	ns min	SCLK low time
t_4	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore

[1] Guaranteed by design and characterization, not production tested.
[2] Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7$ V to 5.5 V.

TIMING DIAGRAM

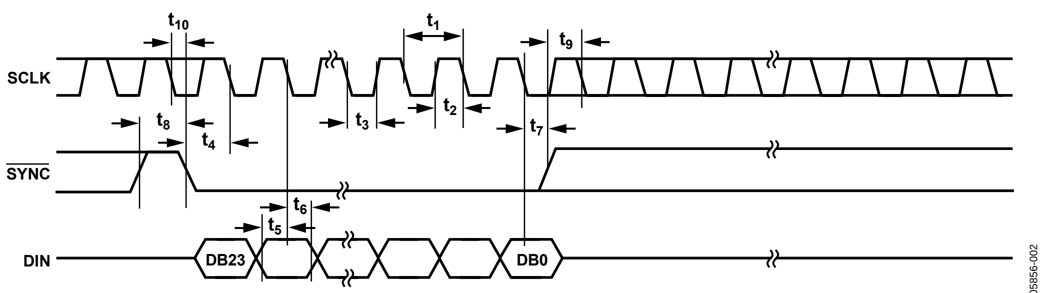


Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

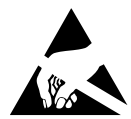
T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$
LFCSP_WD Package (4-Layer Board)	
θ_{JA} Thermal Impedance	61°C/W
MSOP Package (4-Layer Board)	
θ_{JA} Thermal Impedance	142°C/W
θ_{JC} Thermal Impedance	43.7°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

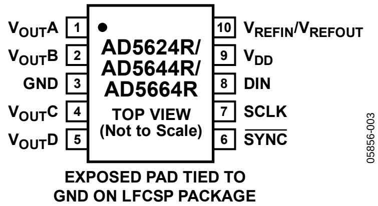


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
3	GND	Ground Reference Point for all Circuitry on the Part.
4	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
6	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 24 clocks. If $\overline{\text{SYNC}}$ is taken high before the 24th falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
8	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
9	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
10	V_{REFIN}/V_{REFOUT}	The AD5624R/AD5644R/AD5664R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.

TYPICAL PERFORMANCE CHARACTERISTICS

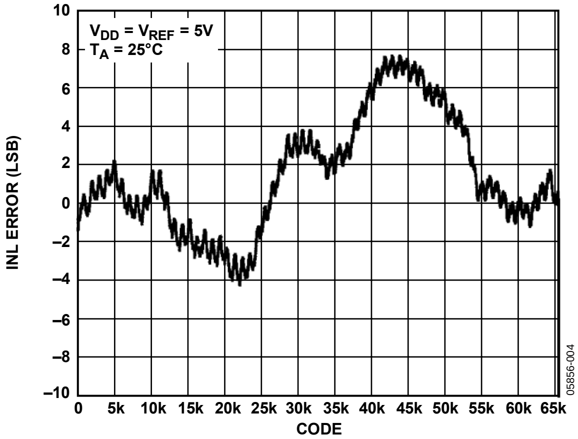


Figure 4. INL AD5664R, External Reference

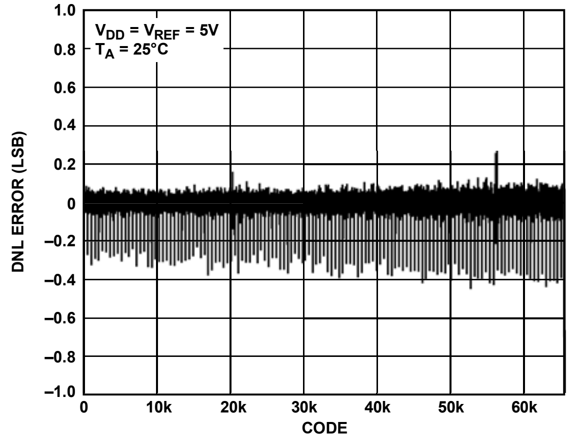


Figure 7. DNL AD5664R, External Reference

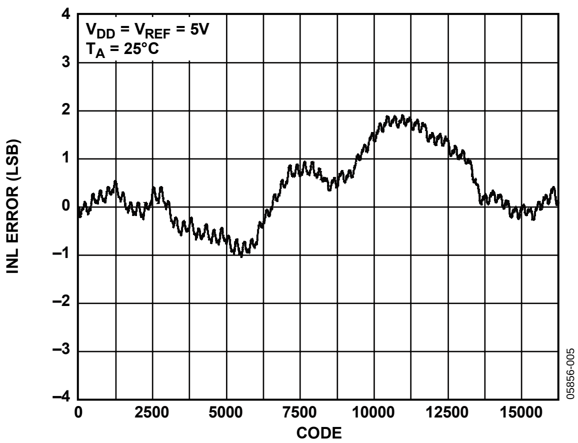


Figure 5. INL AD5644R, External Reference

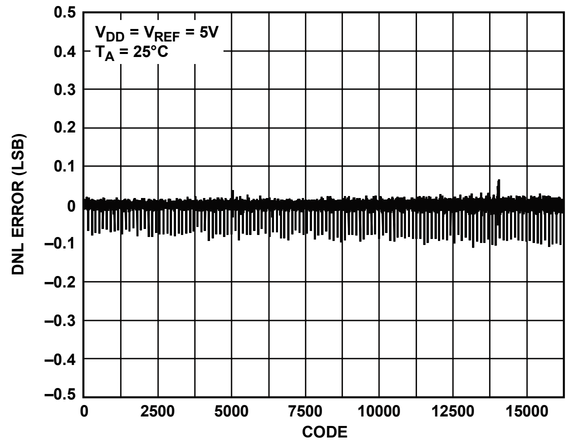


Figure 8. DNL AD5644R, External Reference

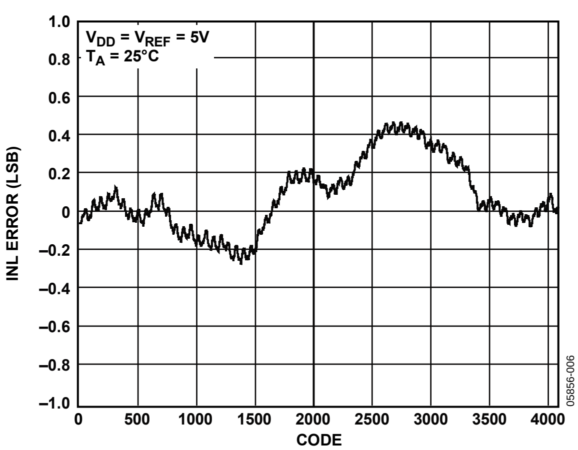


Figure 6. INL AD5624R, External Reference

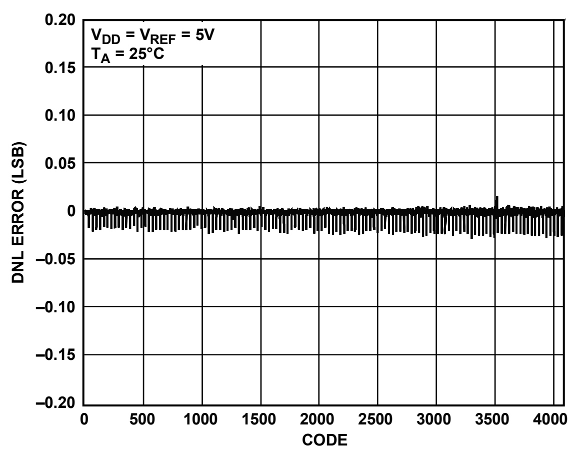


Figure 9. DNL AD5624R, External Reference

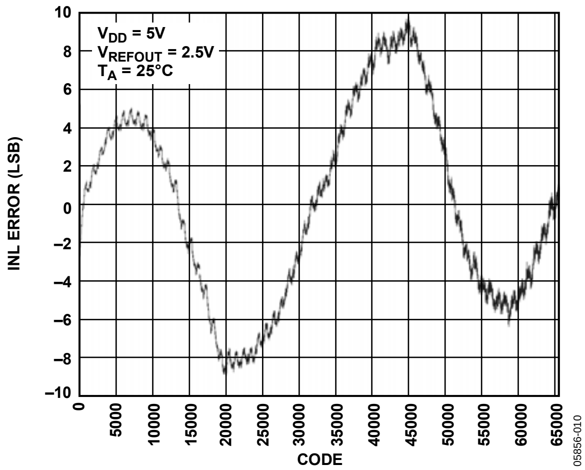


Figure 10. INL AD5664R-5, Internal Reference

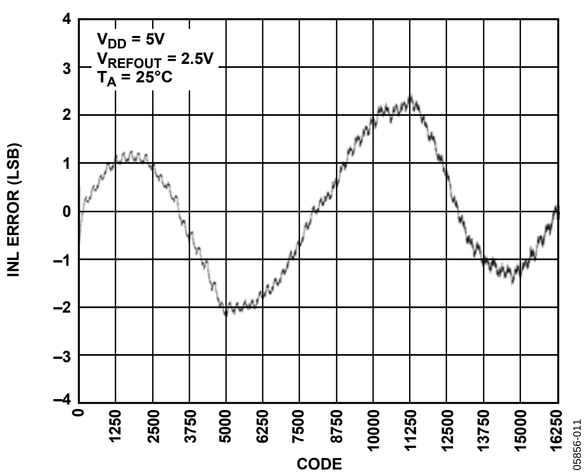


Figure 11. INL AD5644R-5, Internal Reference

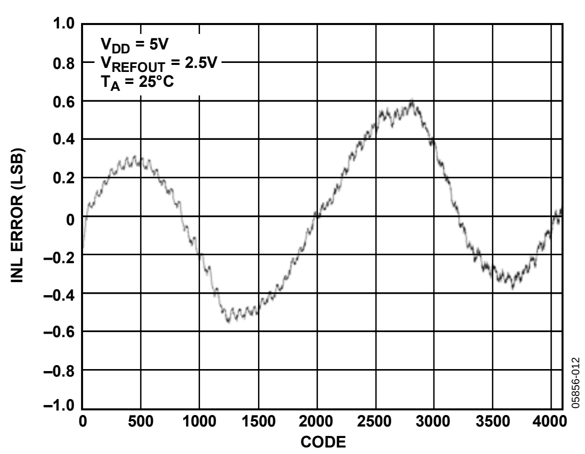


Figure 12. INL AD5624R-5, Internal Reference

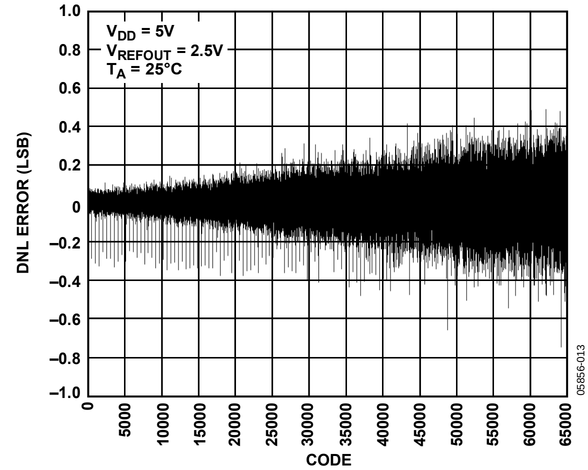


Figure 13. DNL AD5664R-5, Internal Reference

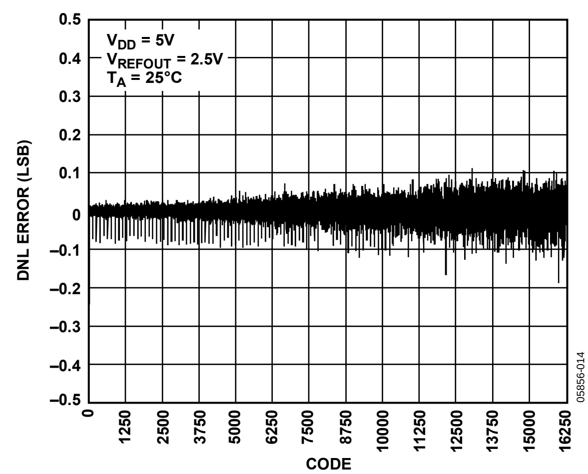


Figure 14. DNL AD5644R-5, Internal Reference

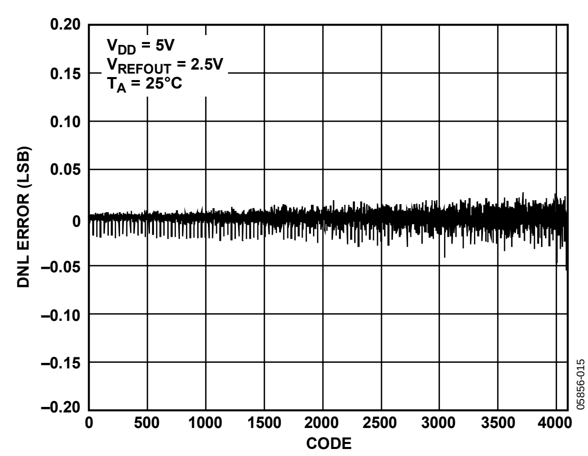


Figure 15. DNL AD5624R-5, Internal Reference

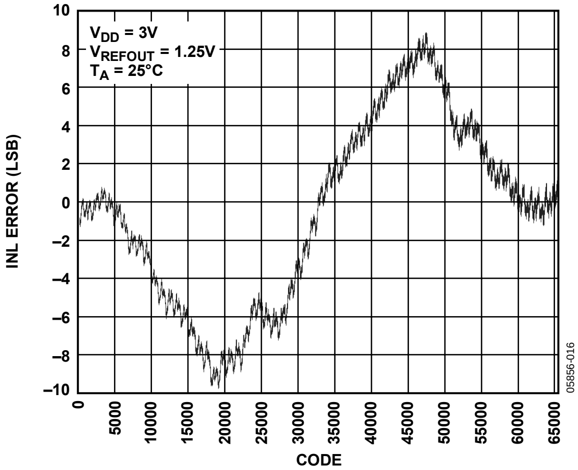


Figure 16. INL AD5664R-3, Internal Reference

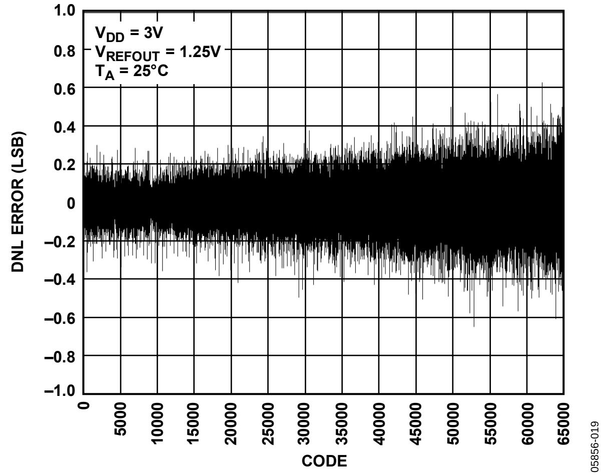


Figure 19. DNL AD5664R-3, Internal Reference

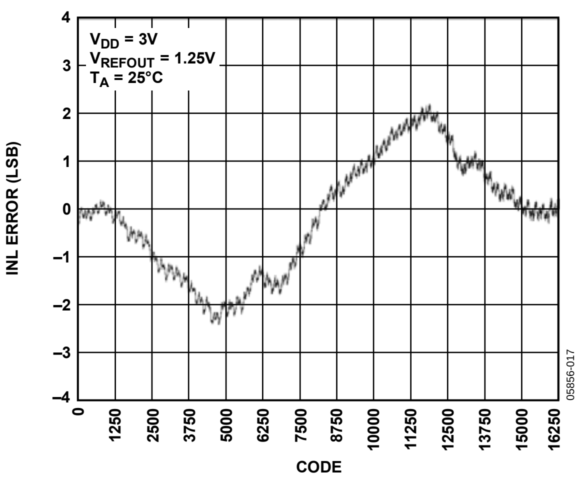


Figure 17. INL AD5644R-3, Internal Reference

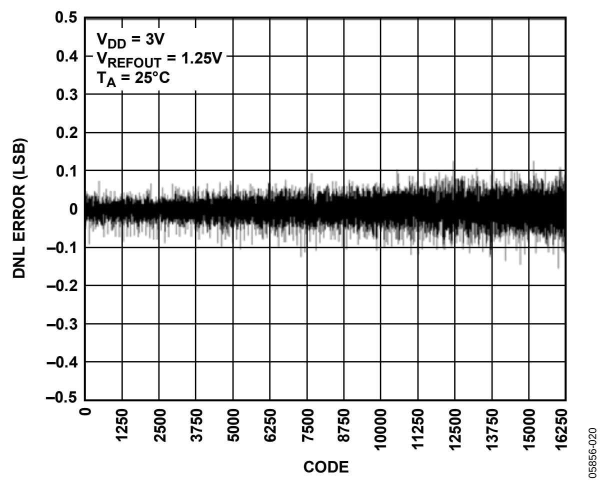


Figure 20. DNL AD5644R-3, Internal Reference

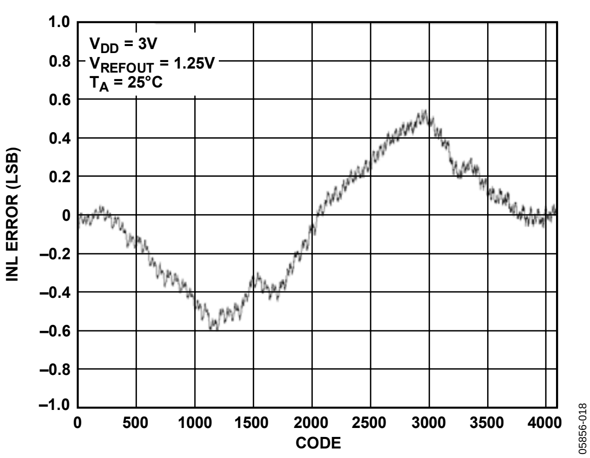


Figure 18. INL AD5624R-3, Internal Reference

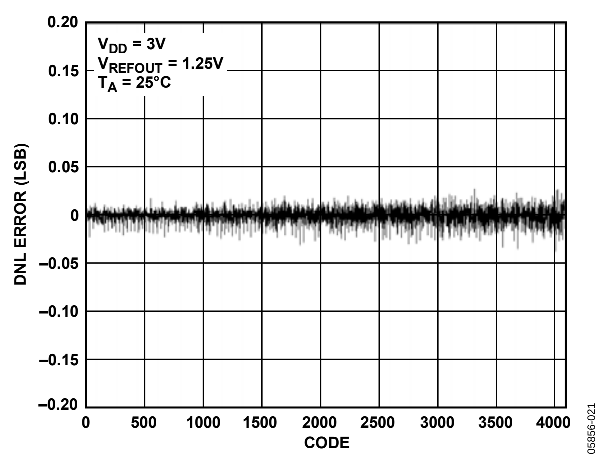


Figure 21. DNL AD5624R-3, Internal Reference

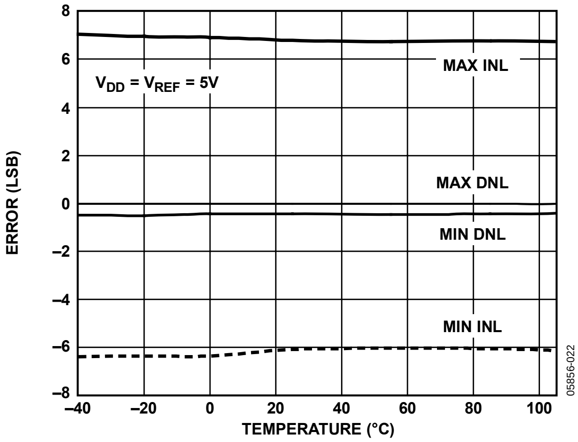


Figure 22. INL Error and DNL Error vs. Temperature

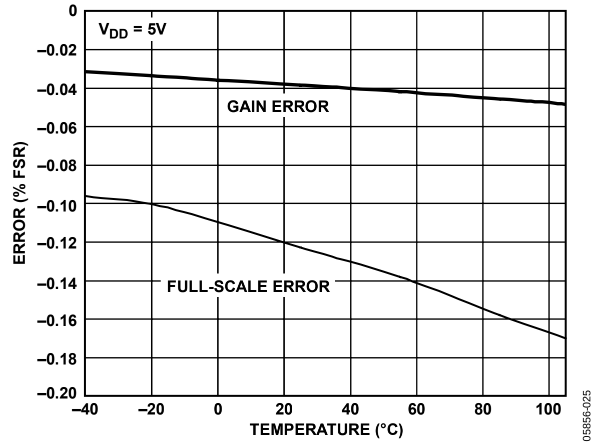


Figure 25. Gain Error and Full-Scale Error vs. Temperature

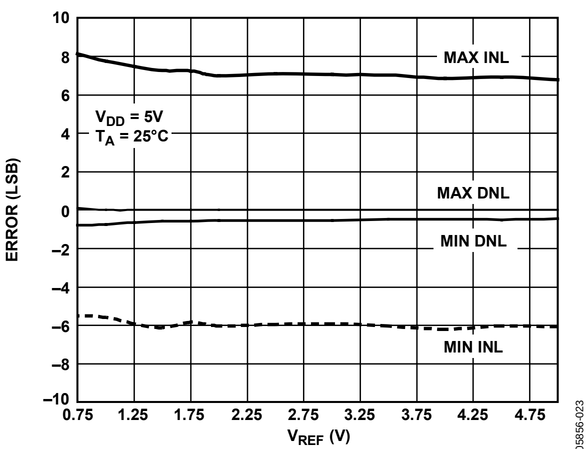


Figure 23. INL Error and DNL Error vs. V_{REF}

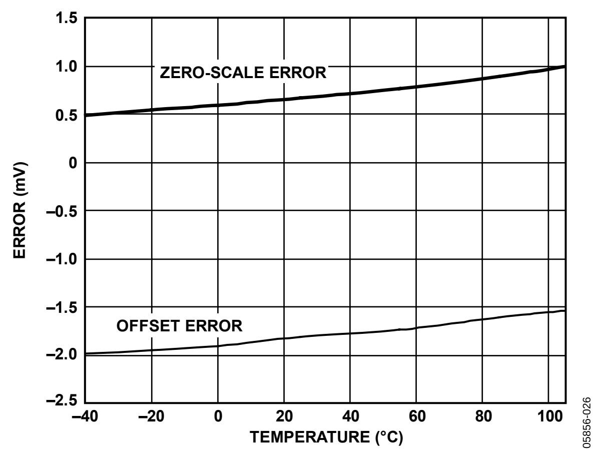


Figure 26. Zero-Scale Error and Offset Error vs. Temperature

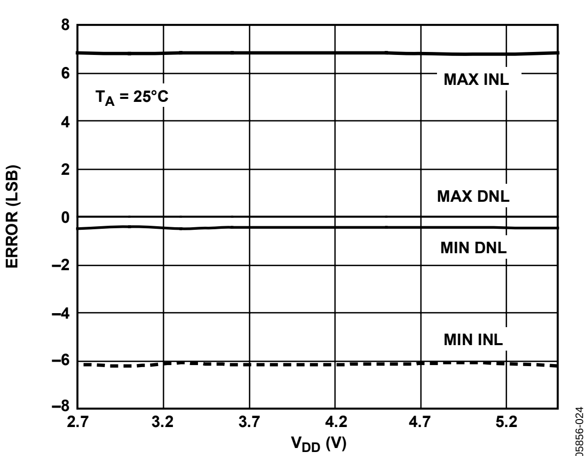


Figure 24. INL Error and DNL Error vs. Supply

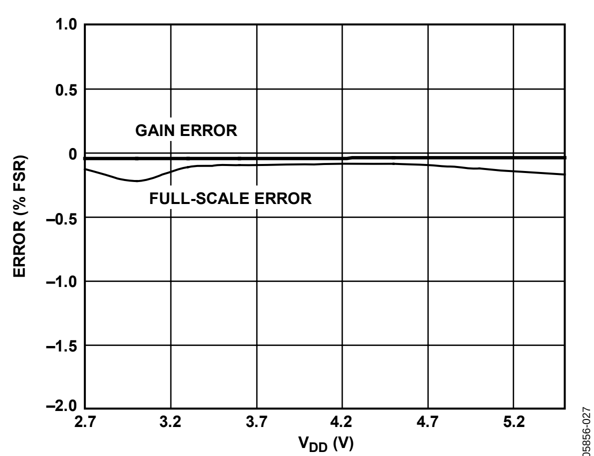


Figure 27. Gain Error and Full-Scale Error vs. Supply

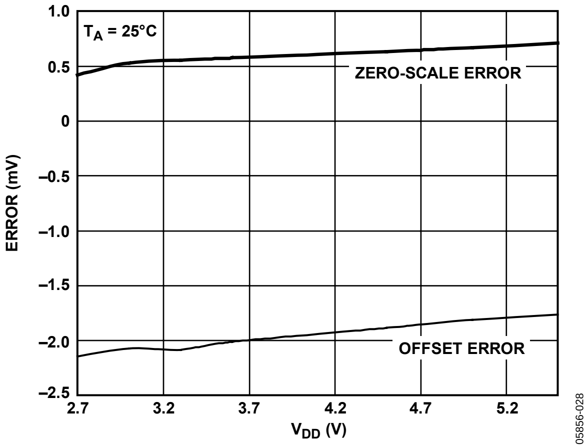


Figure 28. Zero-Scale Error and Offset Error vs. Supply

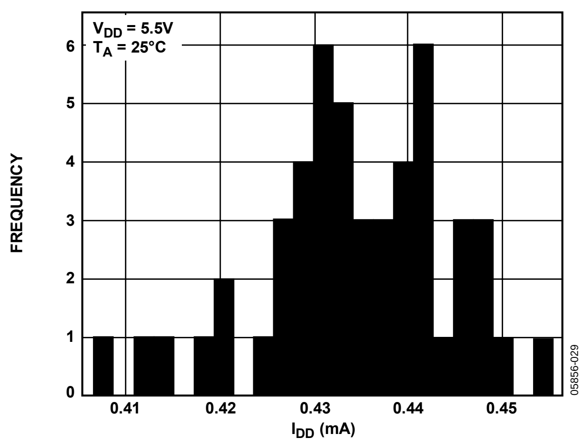


Figure 29. I_{DD} Histogram with External Reference, 5.5 V

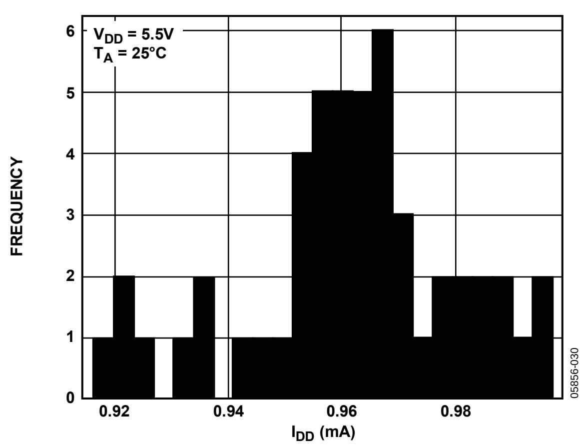


Figure 30. I_{DD} Histogram with Internal Reference, $V_{REFOUT} = 2.5$ V

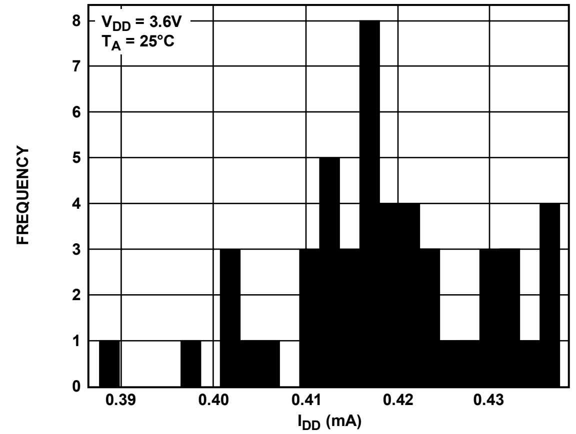


Figure 31. I_{DD} Histogram with External Reference, 3.6 V

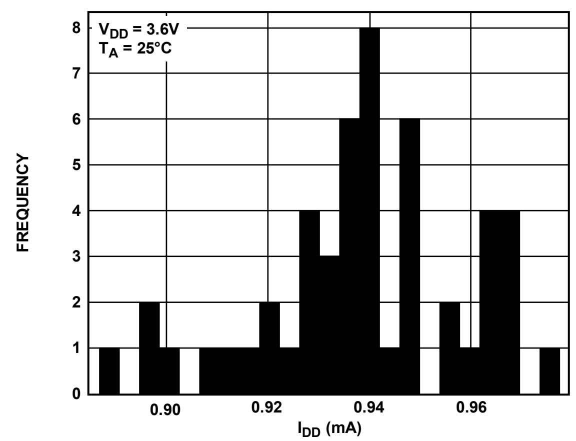


Figure 32. I_{DD} Histogram with Internal Reference, $V_{REFOUT} = 1.25$ V

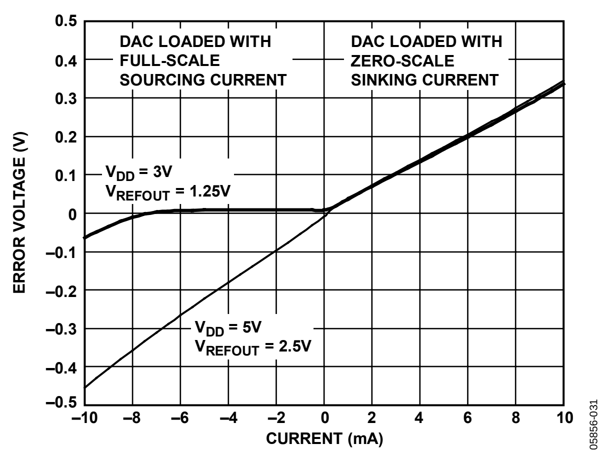


Figure 33. Headroom at Rails vs. Source and Sink

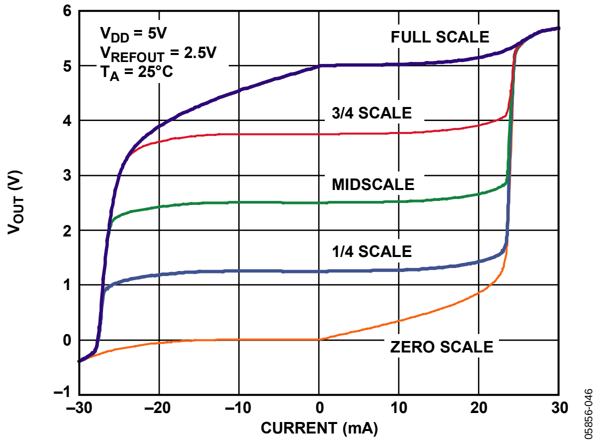


Figure 34. AD56x4R-5 Source and Sink Capability

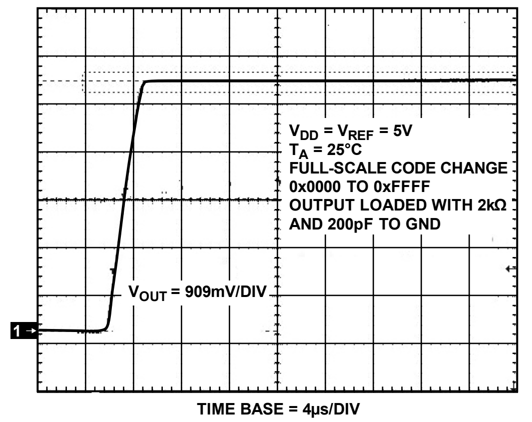


Figure 37. Full-Scale Settling Time, 5 V

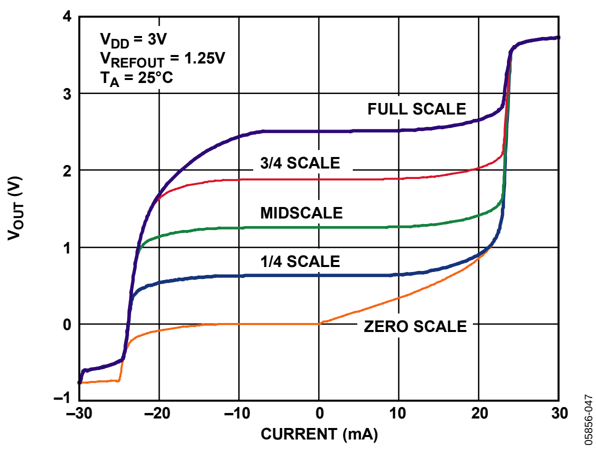


Figure 35. AD56x4R-3 Source and Sink Capability

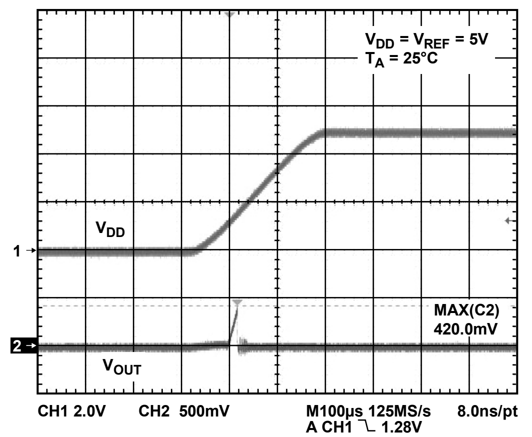


Figure 38. Power-On Reset to 0 V

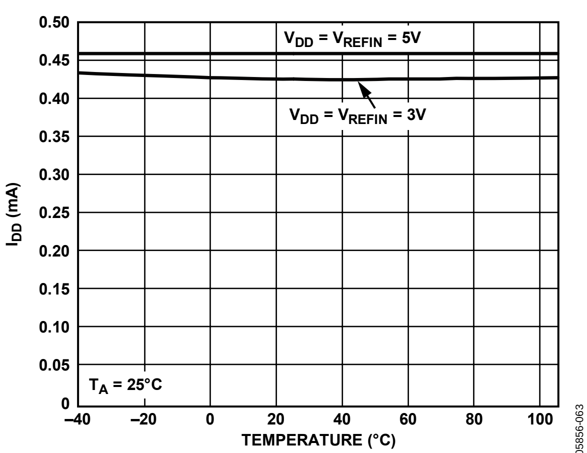


Figure 36. Supply Current vs. Temperature

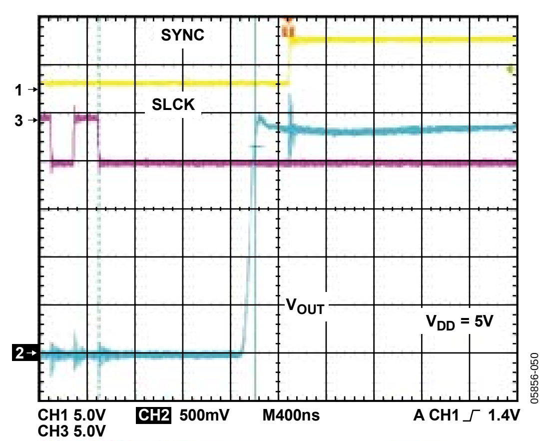


Figure 39. Exiting Power-Down to Midscale

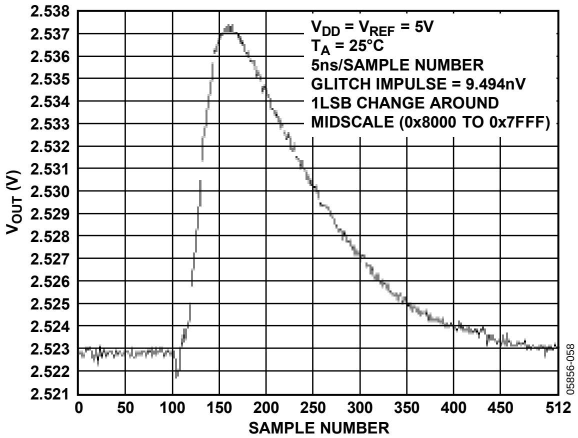


Figure 40. Digital-to-Analog Glitch Impulse (Negative)

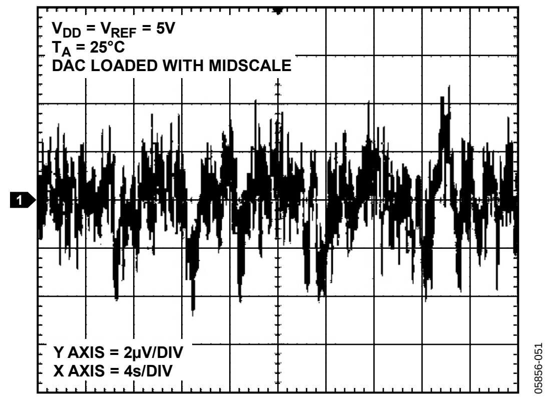


Figure 43. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

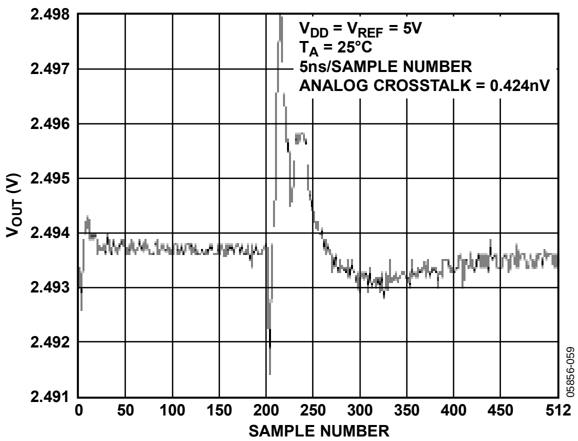


Figure 41. Analog Crosstalk, External Reference

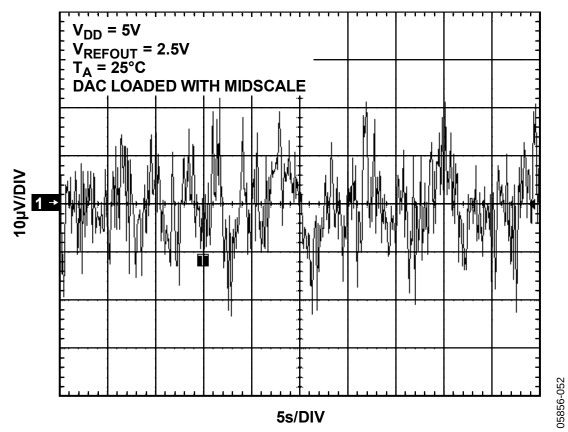


Figure 44. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

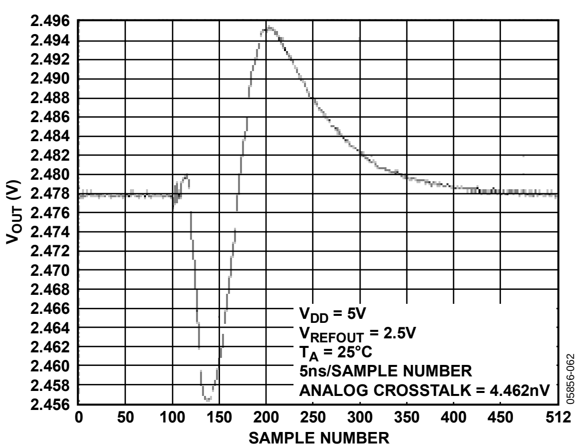


Figure 42. Analog Crosstalk, Internal Reference

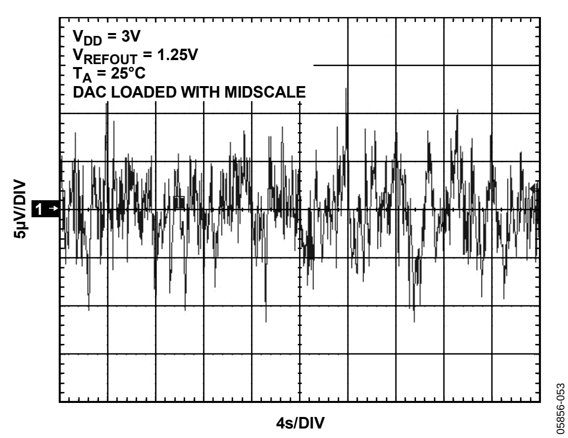


Figure 45. 0.1 Hz to 10 Hz Output Noise Plot, 1.25 V Internal Reference

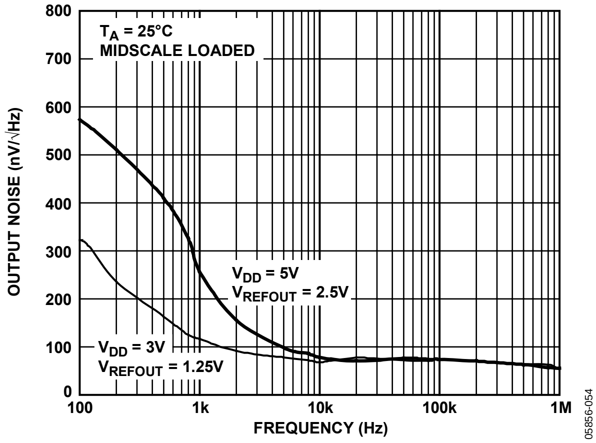


Figure 46. Noise Spectral Density, Internal Reference

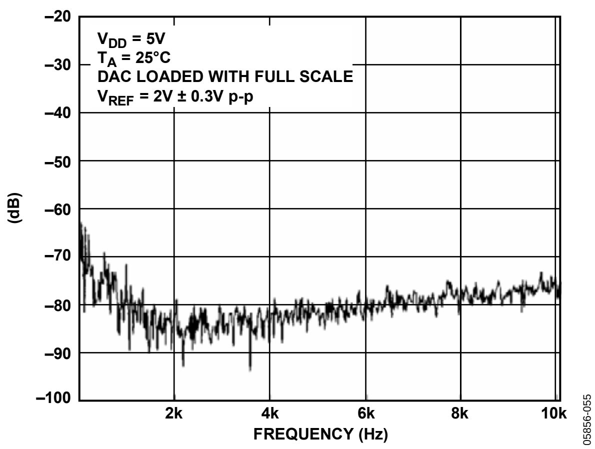


Figure 47. Total Harmonic Distortion

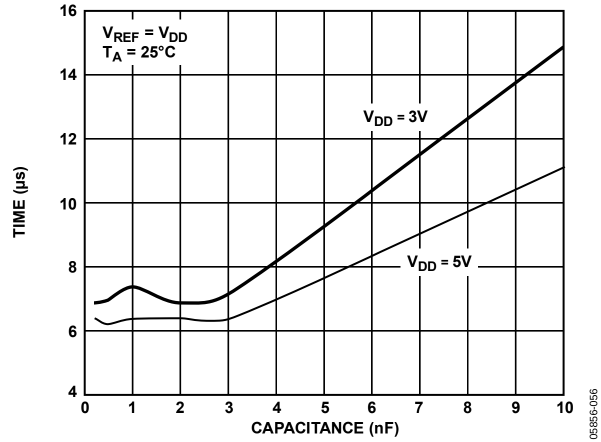


Figure 48. Settling Time vs. Capacitive Load

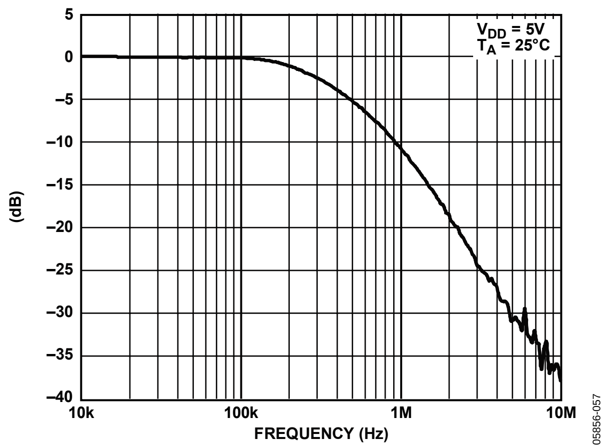


Figure 49. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 4.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 7.

Zero-Code Error
Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5664R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 26.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 25.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Zero-Code Error Drift
This is a measurement of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Temperature Coefficient
This is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5664R with code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the 24th falling edge of SCLK.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 40).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density can be seen in Figure 46.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in μV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in μV/mA.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) using the command write to and update while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

THEORY OF OPERATION

D/A SECTION

The AD5624R/AD5644R/AD5664R DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 50 shows a block diagram of the DAC architecture.

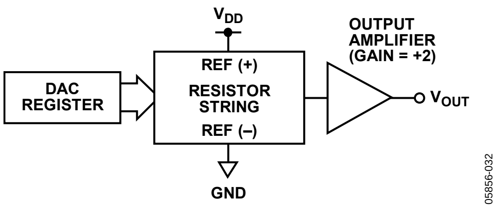


Figure 50. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N}\right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N}\right)$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register:

0 to 4095 for AD5624R (12 bit).
0 to 16,383 for AD5644R (14 bit).
0 to 65,535 for AD5664R (16 bit).

N is the DAC resolution.

RESISTOR STRING

The resistor string is shown in Figure 51. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 33 and Figure 34. The slew rate is 1.8 V/µs with a ¼ to ¾ full-scale settling time of 7 µs.

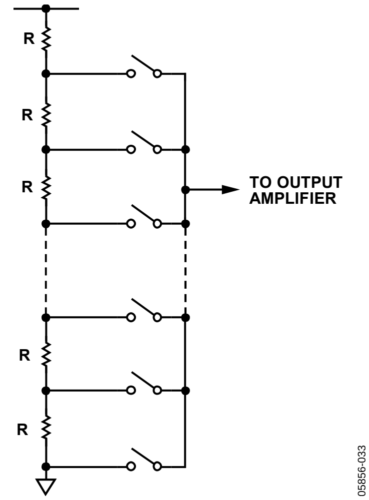


Figure 51. Resistor String

INTERNAL REFERENCE

The AD5624R/AD5644R/AD5664R on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

The AD56x4R-3 has a 1.25 V, 5 ppm/°C reference giving a full-scale output of 2.5 V. The AD56x4R-5 has a 2.5 V, 5 ppm/°C reference giving a full-scale output of 5 V. The internal reference associated with each part is available at the V_{REFOUT} pin.
A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor is placed between reference output and GND for reference stability.

EXTERNAL REFERENCE

The V_{REFIN} pin on the AD56x4R-3 and AD56x4R-5 allows the use of an external reference if the application requires it. The default condition of the on-chip reference is off at power-up. All devices (AD56x4R-3 and the AD56x4R-5) can be operated from a single 2.7 V to 5.5 V supply.

SERIAL INTERFACE

The AD5624R/AD5644R/AD5664R have a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as with most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5624R/AD5644R/AD5664R compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation.

At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

Since the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 2 V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation. As mentioned previously, it must, however, be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide (see Figure 52). The first two bits are don't care bits. The next three are the command bits, C2 to C0 (see Table 8), followed by the 3-bit DAC address, A2 to A0 (see Table 9), and then the 16-, 14-, 12-bit data-word. The data-word comprises the 16-, 14-, 12-bit input code followed by 0, 2, or 4 don't care bits, for the AD5664R, AD5644R, and AD5624R, respectively (see Figure 52, Figure 53, and Figure 54). These data bits are transferred to the DAC register on the 24th falling edge of SCLK.

Table 8. Command Definition

C2	C1	C0	Command
0	0	0	Write to input register *n*
0	0	1	Update DAC register *n*
0	1	0	Write to input register *n*, update all (software LDAC)
0	1	1	Write to and update DAC channel *n*
1	0	0	Power down DAC (power-up)
1	0	1	Reset
1	1	0	LDAC register setup
1	1	1	Internal reference setup (on/off)

Table 9. Address Command

A2	A1	A0	Address (*n*)
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	1	1	All DACs

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 24 falling edges of SCLK, and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 24th falling edge, then this acts as an interrupt to the write sequence. The input shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 55).

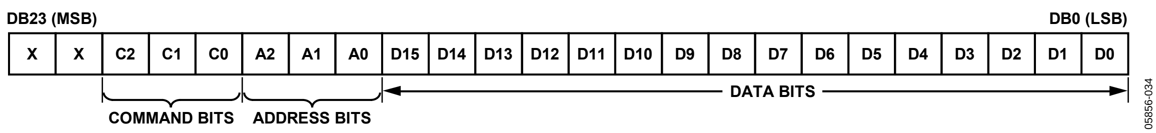


Figure 52. AD5664R Input Shift Register Contents

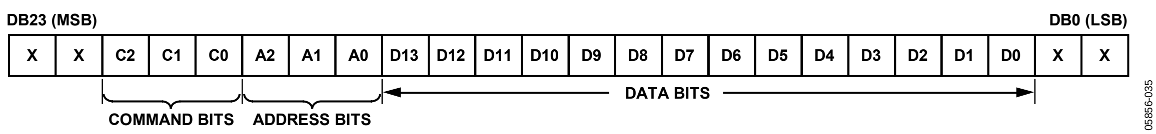


Figure 53. AD5644R Input Shift Register Contents

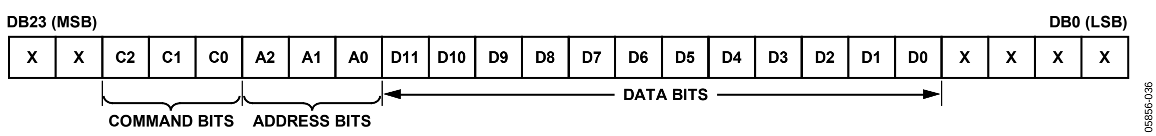


Figure 54. AD5624R Input Shift Register Contents

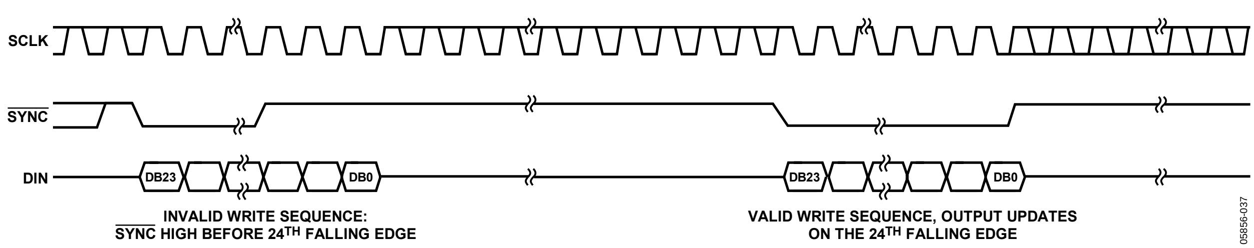


Figure 55. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-ON RESET

The AD5624R/AD5644R/AD5664R family contains a power-on reset circuit that controls the output voltage during power-up. The AD5624R/AD5644R/AD5664R DACs output power up to 0 V and the output remains there until a valid write sequence is made to the DACs. This is useful in applications where it is important to know the state of the output of the DACs while they are in the process of powering up.

SOFTWARE RESET

The AD5624R/AD5644R/AD5664R contain a software reset function. Command 101 is reserved for the software reset function (see Table 8). The software reset command contains two reset modes that are software programmable by setting bit DB0 in the control register.

Table 10 shows how the state of the bit corresponds to the software reset modes of operation of the devices. Table 12 shows the contents of the input shift register during the software reset mode of operation.

Table 10. Software Reset Modes for the AD5624R/AD5644R/AD5664R

DB0	Registers Reset to Zero
0	DAC register
	Input shift register
1 (Power-On Reset)	DAC register
	Input shift register
	LDAC register
	Power-down register
	Internal reference setup register

POWER-DOWN MODES

The AD5624R/AD5644R/AD5664R contain four separate modes of operation. Command 100 is reserved for the power-down function (see Table 8). These modes are software programmable by setting two bits (DB5 and DB4) in the control register. Table 11 shows how the state of the bits corresponds to the mode of operation of the device. All DACs, (DAC D to DAC A) can be powered down to the selected mode by setting the corresponding four bits (DB3, DB2, DB1, and DB0) to 1.

By executing the same Command 100, any combination of DACs can be powered up by setting the bits (DB5 and DB4) to normal operation mode. To select which combination of DAC channels to power-up, set the corresponding four bits (DB3, DB2, DB1, and DB0) to 1. See Table 13 for contents of the input shift register during power-down/power-up operation.

Table 11. Modes of Operation for the AD5624R/AD5644R/AD5664R

DB5	DB4	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

When Bit DB5 and Bit DB4 are set to 0, the part works normally with its normal power consumption of 450 µA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V (200 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This allows the output impedance of the part to be known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ resistor, or left open-circuited (three-state) as shown in Figure 54.

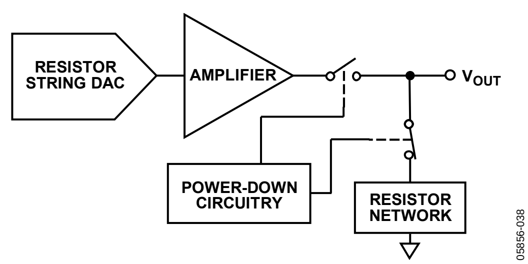


Figure 56. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shutdown when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for V_{DD} = 5 V and for V_{DD} = 3 V (see Figure 39).

Table 12. 24-Bit Input Shift Register Contents for Software Reset Command

DB23 to DB22 (MSB)	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0 (LSB)
x	1	0	1	x	x	x	x	1/0
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0)			Don't care	Determines software reset mode

Table 13. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation for the AD5624R/AD5644R/AD5664R

DB23 to DB22 (MSB)	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
x	1	0	0	x	x	x	x	PD1	PD0	DAC D	DAC C	DAC B	DAC A
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0) Don't care			Don't care	Power-down mode		Power-down/power-up channel selection, set bit to 1 to select channel			

LDAC FUNCTION

The AD5624R/AD5644R/AD5664R DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to three of the input registers individually and then write to the remaining input register, updating all DAC registers simultaneously. Command 010 is reserved for this software LDAC.

Access to the DAC registers is controlled by the LDAC function. The LDAC register contains two modes of operation for each DAC channel. The DAC channels are selected by setting the bits of the 4-bit LDAC register (DB3, DB2, DB1, and DB0). Command 110 is reserved for setting up the LDAC register. When the LDAC bit register is set low, the corresponding DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When the LDAC bit register is set high, however, the DAC registers become transparent and the contents of the input registers are transferred to them on the falling edge of the 24th SCLK pulse. This is equivalent to having an $\overline{\text{LDAC}}$ hardware pin tied permanently low for the selected DAC channel, that is, synchronous update mode. See Table 14 for the LDAC register mode of operation. See Table 16 for contents of the input shift register during the LDAC register setup command.

This flexibility is useful in applications where the user wants to update select channels simultaneously, while the rest of the channels update synchronously.

Table 14. LDAC Register Mode of Operation

Load DAC Register	
LDAC Bits (DB3 to DB0)	**LDAC Mode of Operation**
0	Normal operation (default), DAC register update is controlled by write command.
1	The DAC registers are updated after new data is read in on the falling edge of the 24th SCLK pulse.

INTERNAL REFERENCE SETUP

The on-chip reference is off at power-up by default. This reference can be turned on or off by setting a software programmable bit, DB0 in the control register. Table 15 shows how the state of the bit corresponds to the mode of operation. Command 111 is reserved for setting up the internal reference (see Table 8). Table 16 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device during internal reference setup.

Table 15. Reference Set-up Register

Internal Reference Setup Register (DB0)	Action
0	Reference off (default)
1	Reference on

Table 16. 24-Bit Input Shift Register Contents for LDAC Setup Command for the AD5624R/AD5644R/AD5664R

DB23 to DB22 (MSB)	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB4	DB3	DB2	DB1	DB0 (LSB)
x	1	1	0	x	x	x	x	DAC D	DAC C	DAC B	DAC A
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0); don't care			Don't care	Set bit to 0 or 1 for required mode of operation on respective channel			

Table 17. 24-Bit Input Shift Register Contents for Internal Reference Setup Command

DB23 to DB22 (MSB)	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0 (LSB)
x	1	1	1	x	x	x	x	1/0
Don't care	Command bits (C2 to C0)			Address bits (A2 to A0)			Don't care	Reference setup register

MICROPROCESSOR INTERFACING

AD5624R/AD5644R/AD5664R to Blackfin® ADSP-BF53x Interface

Figure 57 shows a serial interface between the AD5624R/AD5644R/AD5664R and the Black*fin* ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5624R/AD5644R/AD5664R, the setup for the interface is that the DT0PRI drives the DIN pin of the AD5624R/AD5644R/AD5664R, while TSCLK0 drives the SCLK of the part. The $\overline{\text{SYNC}}$ is driven from TFS0.

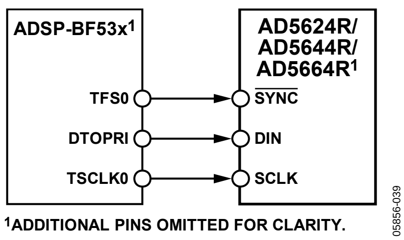


*Figure 57. Black*fin *ADSP-BF53x Interface to AD5624R/AD5644R/AD5664R*

AD5624R/AD5644R/AD5664R to 68HC11/68L11 Interface

Figure 58 shows a serial interface between the AD5624R/AD5644R/AD5664R and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5624R/AD5644R/AD5664R, while the MOSI output drives the serial data line of the DAC.

The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are that the 68HC11/68L11 is configured with its CPOL bit as 0 and its CPHA bit as 1. When data is transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured as described above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5624R/AD5644R/AD5664R, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC; PC7 is taken high at the end of this procedure.

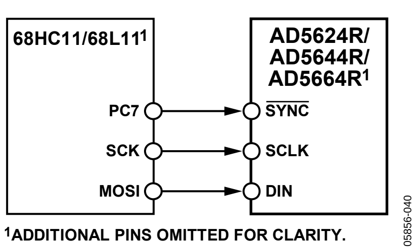


Figure 58. 68HC11/68L11 Interface to AD5624R/AD5644R/AD5664R

AD5624R/AD5644R/AD5664R to 80C51/80L51 Interface

Figure 59 shows a serial interface between the AD5624R/AD5644R/AD5664R and the 80C51/80L51 microcontroller. The setup for the interface is that the TxD of the 80C51/80L51 drives SCLK of the AD5624R/AD5644R/AD5664R, while RxD drives the serial data line of the part. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port. In this case, port line P3.3 is used. When data is transmitted to the AD5624R/AD5644R/AD5664R, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in LSB first format. The AD5624R/ AD5644R/AD5664R must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

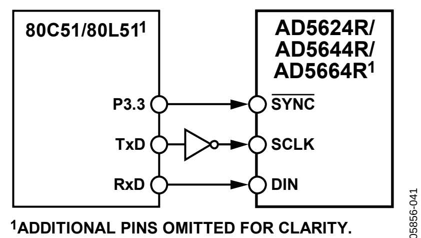


Figure 59. 80C51/80L51 Interface to AD5624R/AD5644R/AD5664R

AD5624R/AD5644R/AD5664R to MICROWIRE Interface

Figure 60 shows an interface between the AD5624R/AD5644R/AD5664R and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5624R/AD5644R/AD5664R on the rising edge of the SK.

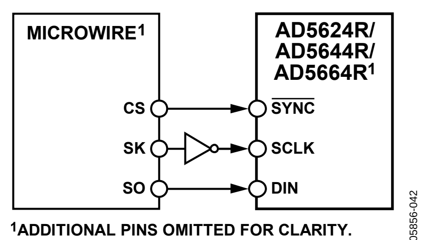


Figure 60. MICROWIRE Interface to AD5624R/AD5644R/AD5664R

APPLICATIONS

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5624R/AD5644R/AD5664R

Because the supply current required by the AD5624R/AD5644R/AD5664R is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 61). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5624R/AD5644R/AD5664R (see Figure 59). If the low dropout REF195 is used, it must supply 450 μA of current to the AD5624R/AD5644R/AD5664R with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

450 μA + (5 V/5 kΩ) = 1.45 mA

The load regulation of the REF195 is typically 2 ppm/mA, resulting in a 2.9 ppm (14.5 μV) error for the 1.45 mA current drawn from it. This corresponds to a 0.191 LSB error.

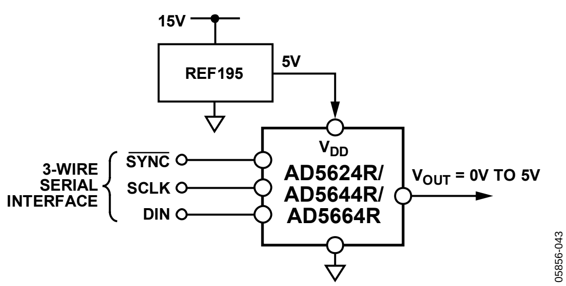


Figure 61. REF195 as Power Supply to the AD5624R/AD5644R/AD5664R

BIPOLAR OPERATION USING THE AD5624R/AD5644R/AD5664R

The AD5624R/AD5644R/AD5664R has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 62. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65536).
With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5\text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

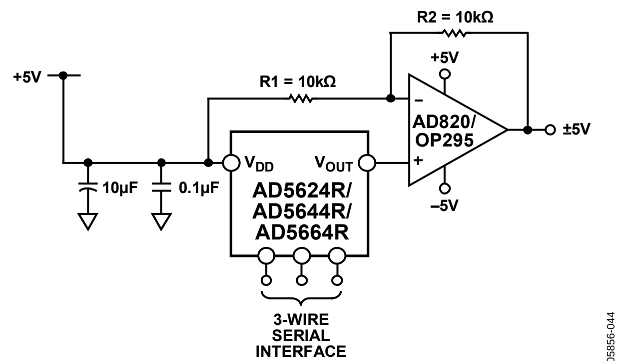


Figure 62. Bipolar Operation with the AD5624R/AD5644R/AD5664R

USING AD5624R/AD5644R/AD5664R WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur in the area where the DAC is functioning. Isocouplers provide isolation in excess of 3 kV. The AD5624R/AD5644R/AD5664R use a 3-wire serial logic interface, so the ADuM130x 3-channel digital isolator provides the required isolation (see Figure 63). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5624R/AD5644R/AD5664R.

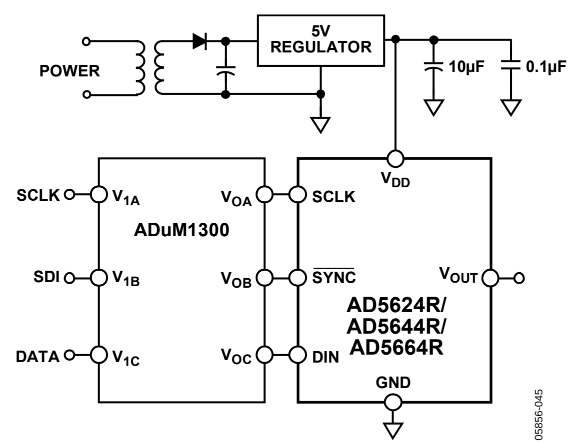


Figure 63. AD5624R/AD5644R/AD5664R with a Galvanica ly Isolated Interface

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5624R/AD5644R/AD5664R should have separate analog and digital sections, each having its own area of the board. If the AD5624R/AD5644R/AD5664R are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5624R/AD5644R/AD5664R.

The power supply to the AD5624R/AD5644R/AD5664R should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitor is the tantalum bead type. It is important that the 0.1 μF capacitor have low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

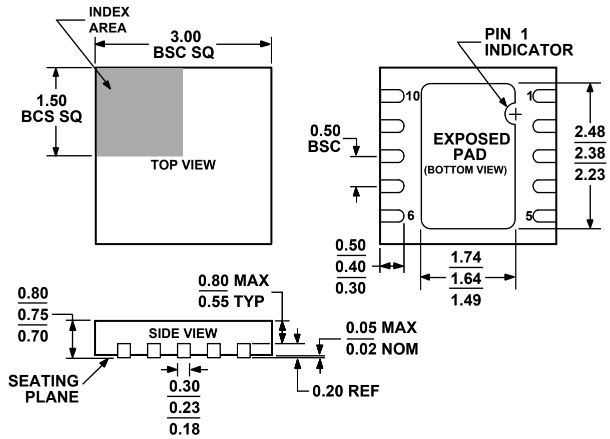


Figure 64. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

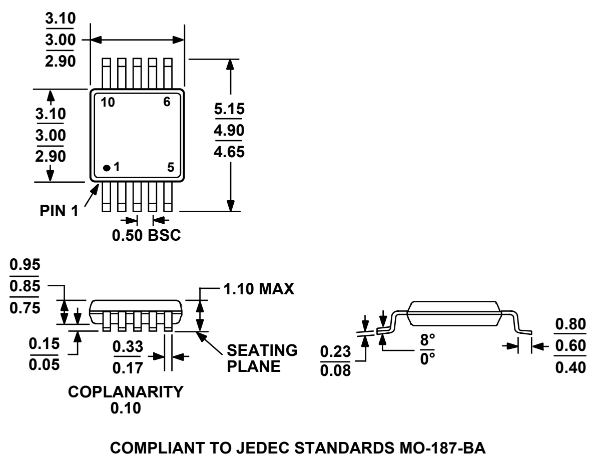


Figure 65. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Accuracy	Internal Reference	Package Description	Package Option	Branding
AD5624RBCPZ-3R2[1]	−40°C to +105°C	±1 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D7L
AD5624RBCPZ-3REEL7[1]	−40°C to +105°C	±1 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D7L
AD5624RBRMZ-3[1]	−40°C to +105°C	±1 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7L
AD5624RBRMZ-3REEL7[1]	−40°C to +105°C	±1 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7L
AD5624RBRMZ-5[1]	−40°C to +105°C	±1 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7V
AD5624RBRMZ-5REEL7[1]	−40°C to +105°C	±1 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7V
AD5644RBRMZ-3[1]	−40°C to +105°C	±4 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7E
AD5644RBRMZ-3REEL7[1]	−40°C to +105°C	±4 LSB INL	1.25 V	10-Lead MSOP	RM-10	D7E
AD5644RBRMZ-5[1]	−40°C to +105°C	±4 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7D
AD5644RBRMZ-5REEL7[1]	−40°C to +105°C	±4 LSB INL	2.5 V	10-Lead MSOP	RM-10	D7D
AD5664RBCPZ-3R2[1]	−40°C to +105°C	±16 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D73
AD5664RBCPZ-3REEL7[1]	−40°C to +105°C	±16 LSB INL	1.25 V	10-Lead LFCSP_WD	CP-10-9	D73
AD5664RBRMZ-3[1]	−40°C to +105°C	±16 LSB INL	1.25 V	10-Lead MSOP	RM-10	D73
AD5664RBRMZ-3REEL7[1]	−40°C to +105°C	±16 LSB INL	1.25 V	10-Lead MSOP	RM-10	D73
AD5664RBRMZ-5[1]	−40°C to +105°C	±16 LSB INL	2.5 V	10-Lead MSOP	RM-10	D75
AD5664RBRMZ-5REEL7[1]	−40°C to +105°C	±16 LSB INL	2.5 V	10-Lead MSOP	RM-10	D75
EVAL-AD5664REB				Evaluation Board		

[1] Z = Pb-free part.

D05856-0-11/06(A)