FAN7310

LCD Back Light Inverter Drive IC

Features

- High Efficiency Single Stage Power Conversion
- Wide Input Voltage Range 5V to 24V
- Back Light Lamp Ballast and Soft Dimming
- Reduce External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS full-bridge topology
- Soft Start
- PWM Control at fixed frequency
- Analog and Burst Dimming Function
- Synchronizable Switching Frequency With An External Signal
- Open Lamp Protection
- Open Lamp Regulation
- 20 Pin SSOP

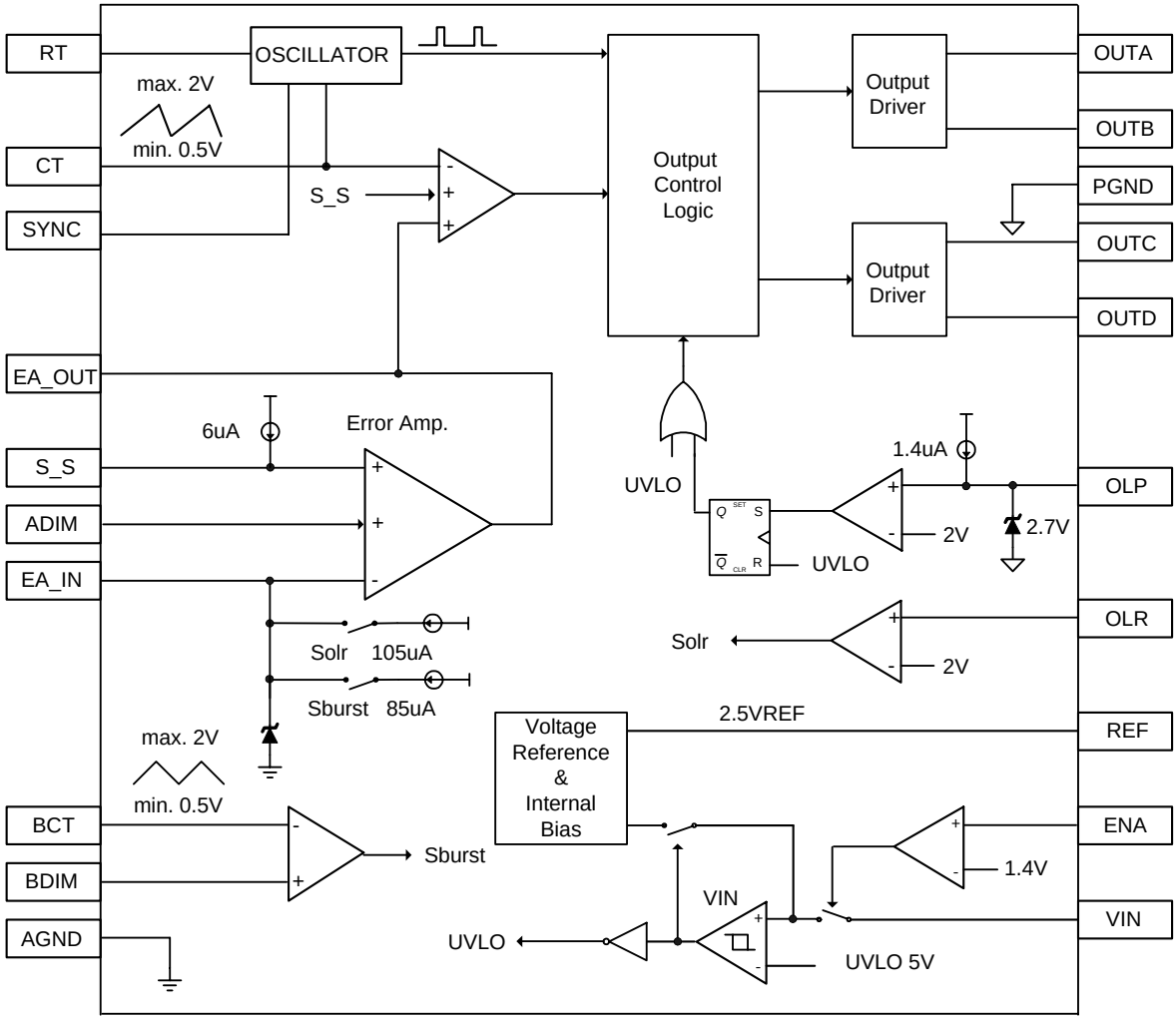
Description

The FAN7310 provides all the control functions for a series parallel resonant converter and also contains a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz depending on the CCFL and the transformer's characteristics.
The FAN7310 has a patent-pending on new phase-shift control.

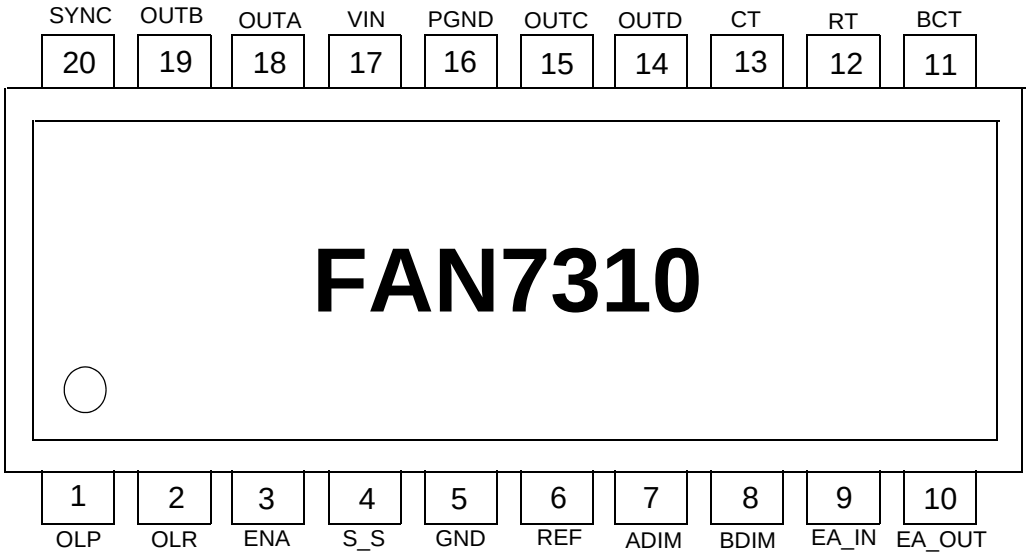
20-SSOP

1

Internal Block Diagram



Pin Assignments



Pin Definitions

No	Name	Function Description	No	Name	Function Description
1	OLP	Open Lamp Protection	11	BCT	Burst Dimming Timing Capacitor
2	OLR	Open Lamp Regulation	12	RT	Timing Resistor
3	ENA	Enable Input	13	CT	Timing Capacitor
4	S_S	Soft Start	14	OUTD	NMOSFET Drive Output D
5	GND	Analog Ground	15	OUTC	PMOSFET Drive Output C
6	REF	2.5V Reference Voltage	16	PGND	Power Ground
7	ADIM	Analog Dimming Input	17	VIN	Supply Voltage
8	BDIM	Burst Dimming Input	18	OUTA	PMOSFET Drive Output A
9	EA_IN	Error Amplifier Input	19	OUTB	NMOSFET Drive Output B
10	EA_OUT	Error Amplifier Output	20	SYNC	Sychronization Input/Output

Absolute Maximum Ratings

For typical values Ta=25°C, Vcc=12V and for min/max values Ta is the operating ambient temperature range with -25°C ≤ Ta ≤ 85°C and 5V ≤ Vcc ≤ 24V, unless otherwise specified.

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	5 ~ 24	V
Operating Temperature Range	Topr	-25 ~ 85	°C
Storage Temperature Range	Tstg	-65 ~ 150	°C
Thermal Resistance Junction-Air (Note1,2)	$R_{\theta JA}$	112	°C/W
Power Dissipation	Pd	1.1	W

Note:

1. Thermal resistance test board
   Size: 76.2mm * 114.3mm * 1.6mm(1S0P)
   JEDEC standard: JESD51-3, JESD51-7
2. Assume no ambient airflow

Electrical Characteristics

For typical values Ta=25°C, Vcc=12V and for min/max values Ta is the operating ambient temperature range with -25°C ≤ Ta ≤ 85°C and 5V ≤ Vcc ≤ 24V, unless otherwise specified.

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION (Recommend X7R Capacitor)						
Line Regulation	ΔVref	$5 \le V_{CC} \le 24V$	-	2	25	mV
2.5V Regulation Voltage	V25	-	2.45	2.5	2.55	V
OSCILLATOR SECTION(MAIN)						
Oscillation Frequency	fosc	Ta = 25°C, Ct = 270pF Rt = 18k	108	115	122	kHz
		Ct = 270pF, Rt = 18k	106	115	124	
CT High Voltage	Vcth	-	-	2.0	-	V
CT Low Voltage	Vctl	-	-	0.5	-	V
SYNC Threshold Voltage	-		-	1	-	V
Recommeded SYNC Input Pulse Width	-		-	10	-	%
OSCILLATOR SECTION(BURST)						
Oscillation Frequency	foscb	Ctb = 10nF, Rt=18k	195	225	255	Hz
BCT High Voltage	Vbcth	-	-	2	-	V
BCT Low Voltage	Vbctl	-	-	0.5	-	V
ERROR AMP SECTION						
Open Loop Gain			-	80	-	dB
Unit Gain Bandwidth			-	1.5	-	MHz
Feedback Output High Voltage	Veh	EA_IN = 0V	-	2.5	-	V
Output Sink Current	Isin	EA_OUT = 1.5V	-	-	-1	mA
Output Source Current	Isur	EA_OUT = 1.5V	1	-	-	mA
EA_IN Driving Current On OLR	Iolr		75	105	135	uA
EA_IN Driving Current On Burst Dimming	Iburst		61	85	109	uA
Feedback High Voltage On Burst Dimming	Vfbh	R(EA_IN) = 60kΩ	Va+0.1	Va+0.4	Va+0.7	V
SOFT START SECTION						
Soft Start Current	I_{SS}	S_S=2V	4	6	8	uA
Soft Start Clamping Voltage	Vssh	-	-	5	-	V
PROTECTION SECTION						
Open Lamp Protection Voltage	Volp	-	1.75	2	2.25	V
Open Lamp Regulation Voltage	Volr	-	1.75	2	2.25	V
Open Lamp Protection Charging Current	Iolp		0.7	1.4	2.1	
UNDER VOLTAGE LOCK OUT SECTION						
Start Threshold Voltage	Vth	-	-	-	5	V
Start Up Current	Ist	V_{CC} = Vth-0.2	-	130	-	uA
Operating Supply Current	Iop	V_{CC} = 12V	-	1.5	-	mA
Stand-by Current	Isb	V_{CC} = 12V	-	200	-	uA
ON/OFF SECTION						
On State Input Voltage	Von	-	2	-	5	V
Off Stage Input Voltage	Voff	-	-	-	0.7	

Electrical Characteristics (Continued)

For typical values Ta=25°C, Vcc=12V and for min/max values Ta is the operating ambient temperature range with -25°C ≤ Ta ≤ 85°C and 5V ≤ Vcc ≤ 24V, unless otherwise specified.

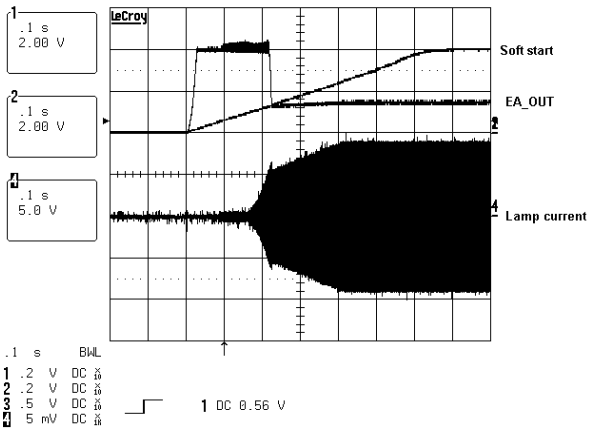
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
PMOS Gate High Voltage	Vpdhv	V_{CC} = 12V	-	Vcc	-	V
PMOS Gate Low Voltage	Vphlv	V_{CC} = 12V	Vcc-10.5	Vcc-8.5	Vcc-6	
NMOS Gate Drive Volgate	Vndhv	V_{CC} = 12V	6	8.5	10.5	V
NMOS Gate Drive Volgate	Vndhv	V_{CC} = 12V	-	0	-	
PMOS Gate Voltage With UVLO Activated	Vpuv	V_{CC} = Vth-0.2	Vcc-0.3	-	-	V
NMOS Gate Voltage With UVLO Activated	Vnuv	V_{CC} = Vth-0.2	-	-	0.3	V
Rising Time	Tr	V_{CC} = 12V, Cload=2nF	-	200	500	ns
Falling Time	Tf	V_{CC} = 12V, Cload=2nF	-	200	500	ns
MAX./MIN OVERLAP						
Min. Overlap between diagonal switches		fosc=100KHz	-	0	-	%
Max. Overlap betwwen diagonal switches		fosc=100KHz	-	100	-	%
DELAY TIME						
PDR_A/NDR_B		Rt=18k	-	450	-	ns
PDR_C/NDR_D		Rt=18k	-	450	-	ns

Function Description

UVLO : The under voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the Vin value. The UVLO circuit turns on the control circuit when Vin exceeds 5V. When Vin is lower than 5V, the IC's standby current is less than 200uA.

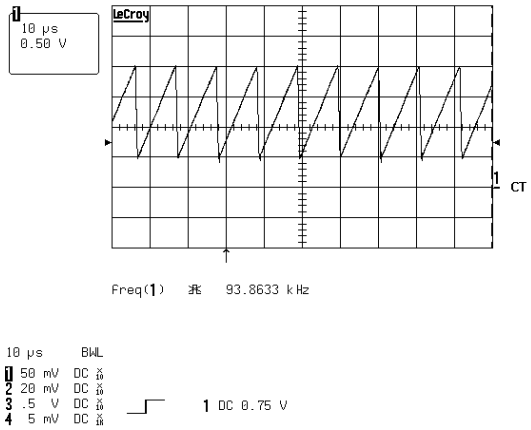
ENA : Applying the voltage higer than 2V to ENA pin enables the operation of the IC. Applying to the voltage lower than 0.7V to ENA pin will disable the operation of the inverter.

Soft start :The soft start function is provided that S_S pin is connected through a capacitor to GND. A soft start circuit ensures a gradual increase in the input and output power. The capacitor connected to S_S pin determines the rate of rise of the duty ratio. It is charged by a current source of 6uA.



Main oscillator : Timing capacitor CT are charged by the reference current source, formed by the timing resistor Rt whose voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once reached, capacitors begin discharging down to 0.5V. Next timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed with adjusting the values of Rt and CT. The main frequency can be calculated as below.

$$f_{op} = \frac{19}{32\ R_T\ C_T}$$

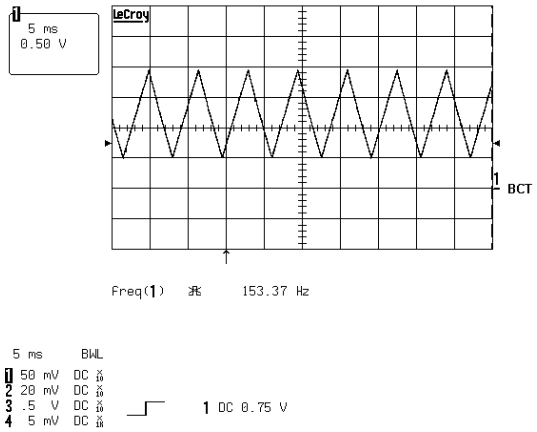


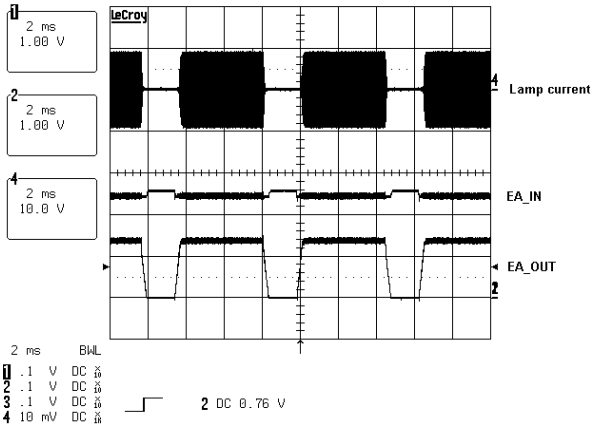
Burst oscillator & burst dimming : Timing capacitor BCT are charged by the reference current source, formed by the timing resistor Rt whose voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once reached, capacitors begin discharging down to 0.5V. Next timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed with adjusting the values of Rt and BCT. The burst dimming frequency can be calculated as below.

$$f_{burst} = \frac{3.75}{64\ R_T\ BC_T}$$

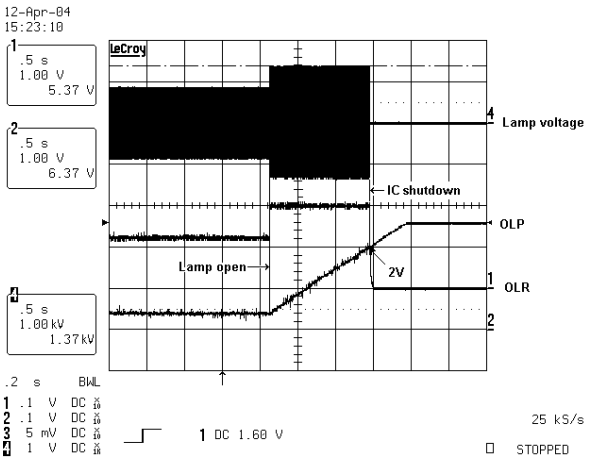
The burst dimming frequency should be greater than 120Hz to avoid visible flicker.

To compare the input of BDIM pin with the 0.5~2V triangular wave of burst oscillator makes the PWM pulse for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85uA into EA_IN pin.

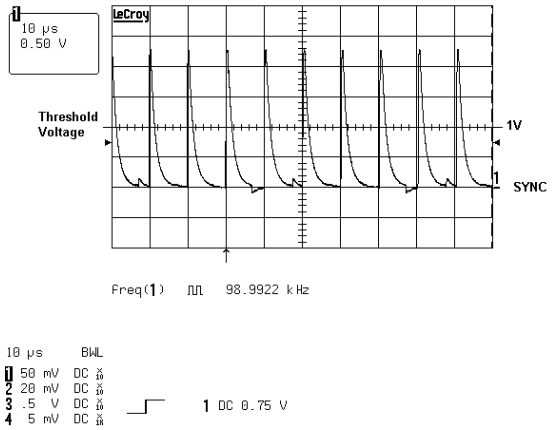




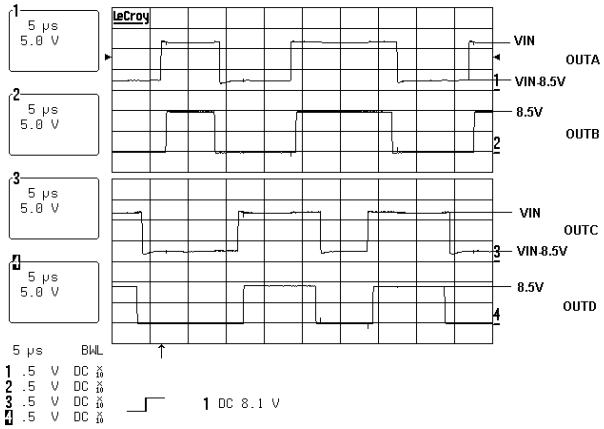
Open lamp regulation & open lamp protection : It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters the regulation mode and controls EA_OUT voltage to limit the lamp voltage by summing 105uA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4uA internal current source. Once reached to 2V, IC enters shut down where all the output is high.



SYNC: This pin is used as the frequency synchronization. The switching frequency can be synchronized with an external control signal. The threshold voltage of this pin is 1V. A resistor should be connected between this pin and GND for the safe operation.

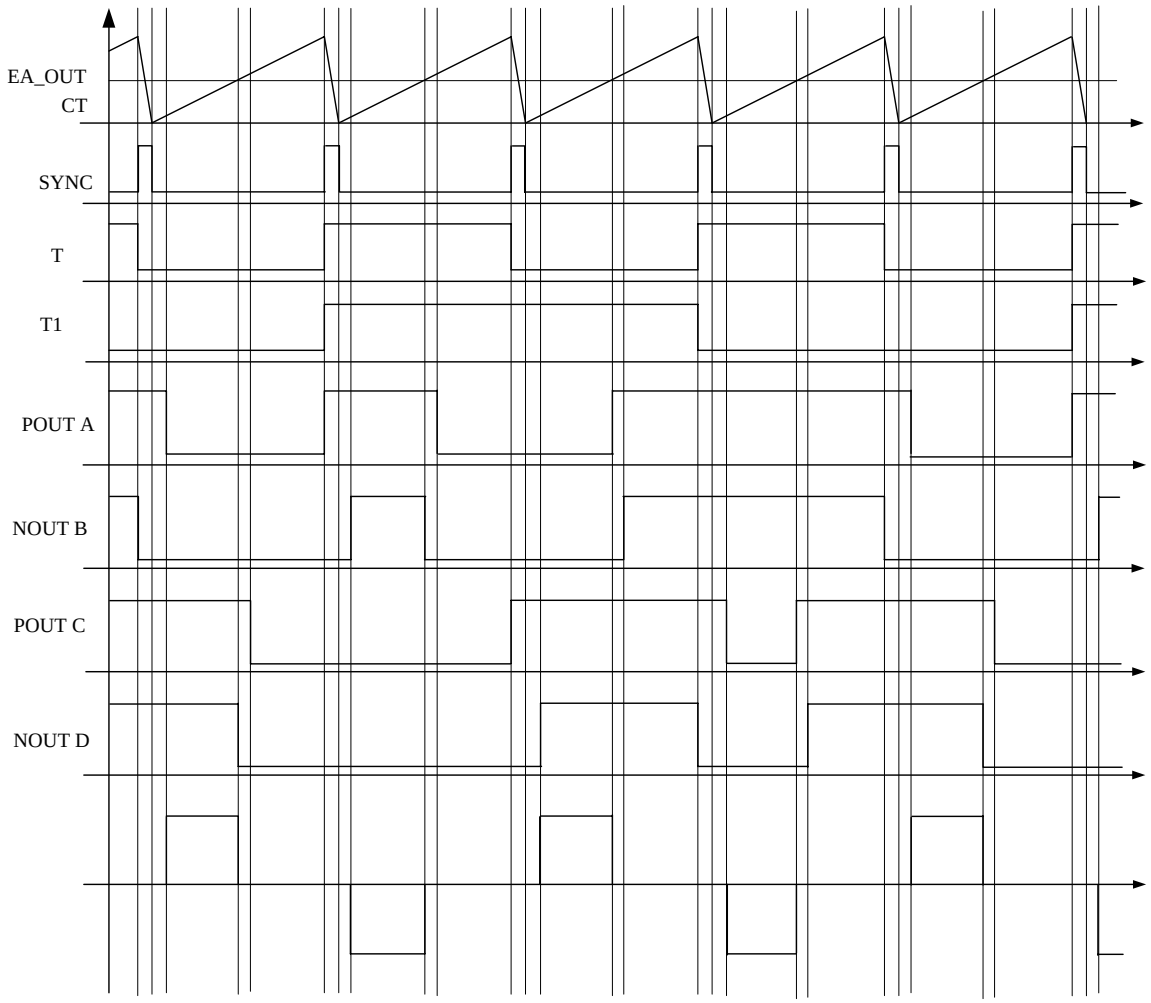


OUTPUT DRIVES: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair will drive the other half-bridge.

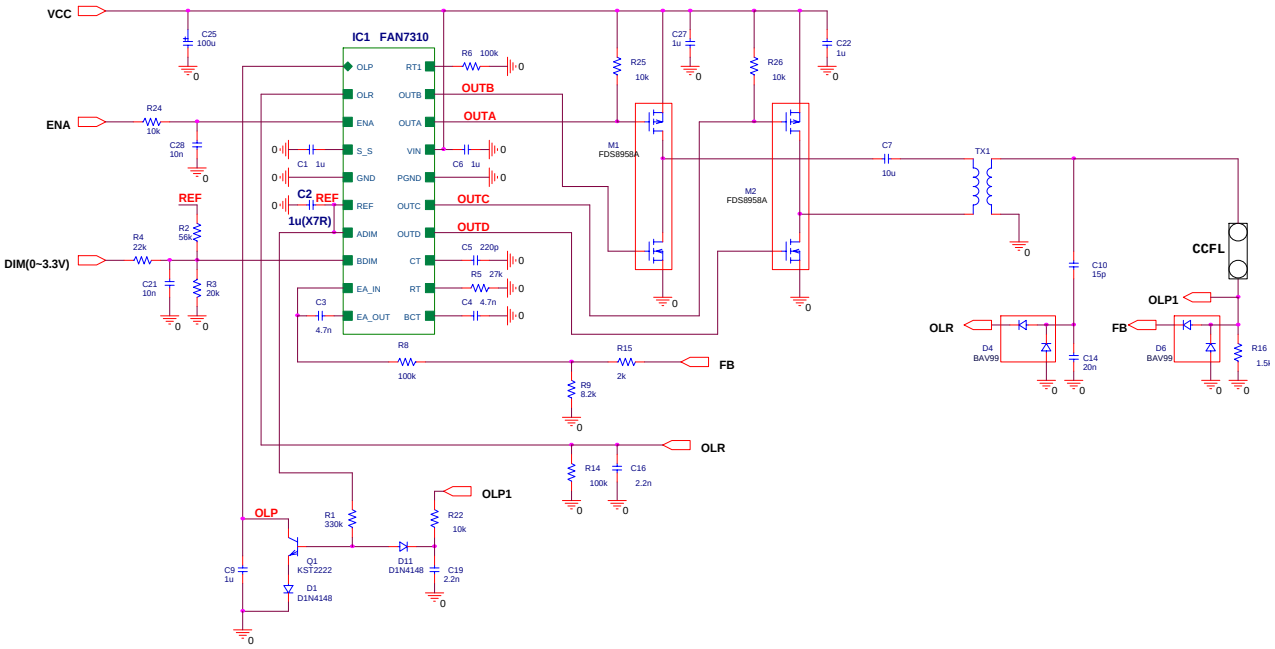


Timing Diagram

FAN7310 use the improved phase-shfit control full-brdige to drive CCFL. As a result, the temperature difference between the left leg and the right legs is almost zero. The detail timing is shown as bellow.



Typical Application Circuit

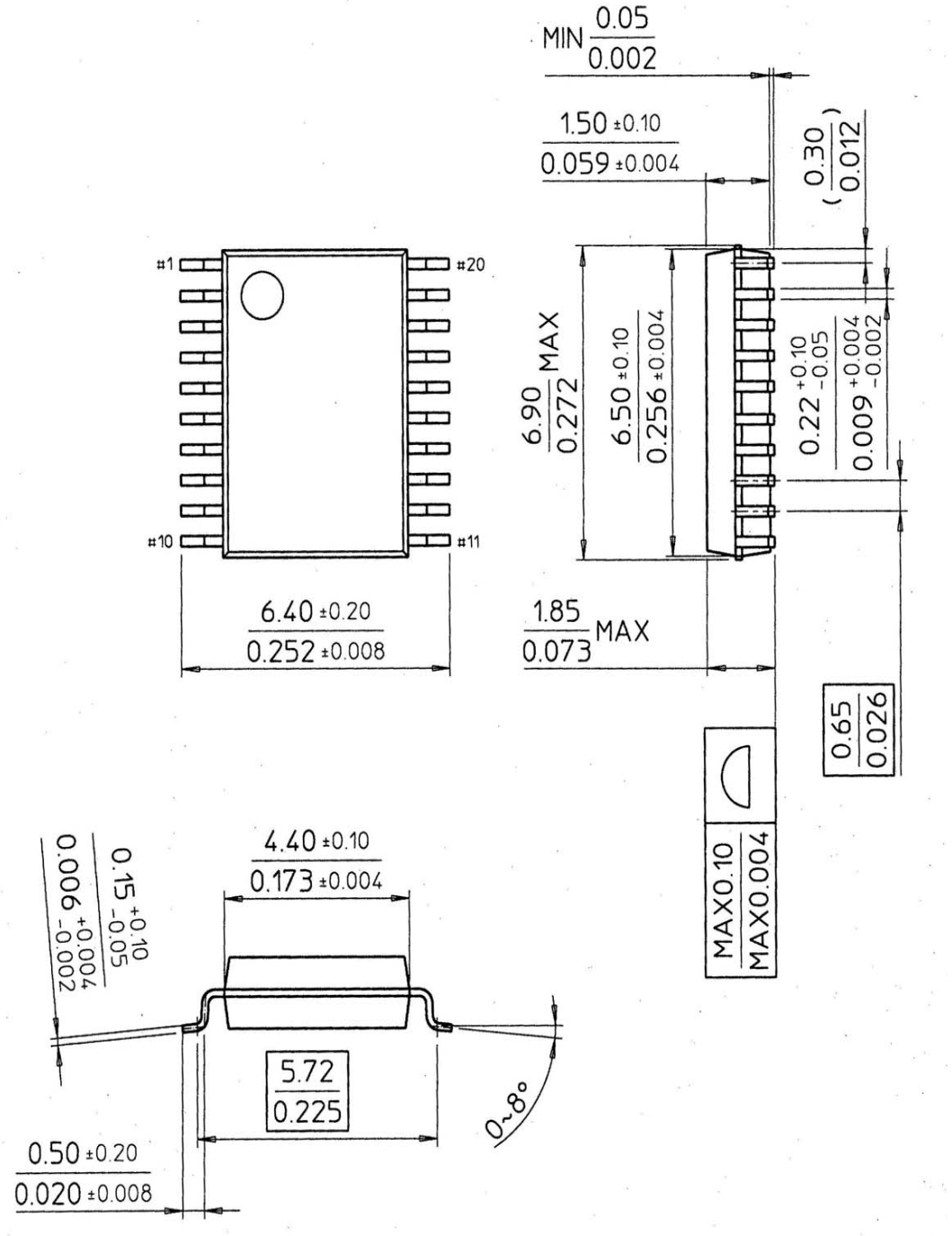


Mechanical Dimensions

Package

Dimensions in millimeters

20-SSOP



Ordering Information

Product number	Package	Operating Temperature
FAN7310G	20-SSOP	-25°C ~ 85°C