Eletech

VP1410
Speech Processor

Features:

- High quality speech generation.
- Speech synthesis with external EPROM or ROM.
- Speech ROM dividable into max. 10 different messages.
- Compatible to Eletech VP-880 voice development system.
- Build-in I/O debounce circuit to prevent false triggering.
- Memory addressable up to 1024K bits. (128K x 8 bits)
- Single 3V~6V supply voltage with low power consumption.
- Inexpensive RC oscillator.
- Bit rate adjustable from 9.6K to 128K bps.
- Continuous variable slope delta modulation (CVSD) technique.
- Internal 12MHz memory serch clock.

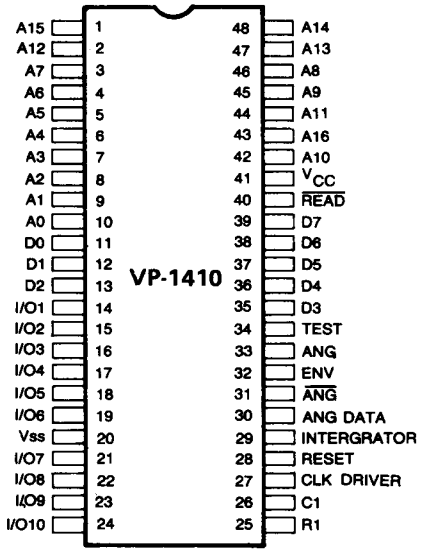
General Description:

The VP-1410 SPEECH PROCESSOR is a CMOS LSI for multi-message speech reproduction usage. It is designed to reform Eletech's VM-410 speech module more compact and reliable. When connected to external speech ROM, max. 10 messages can be re-played by the corresponding I/O signals. Encoding (digitizing) of customer phrases seperated with 6-AA segment flag can be accomplished by the chip manufacturer or alternately by the individuals using Eletech VP-880 voice development system. The VP-880 voice development kit is designed for speech ROM programming which utilizes IBM PC AT/XT as analysis tool. The system will produce very high quality voice output at the sampling rate of 24K to 32K bps as well as an acceptable voice when the sampling rate is lower down to 12K bps.

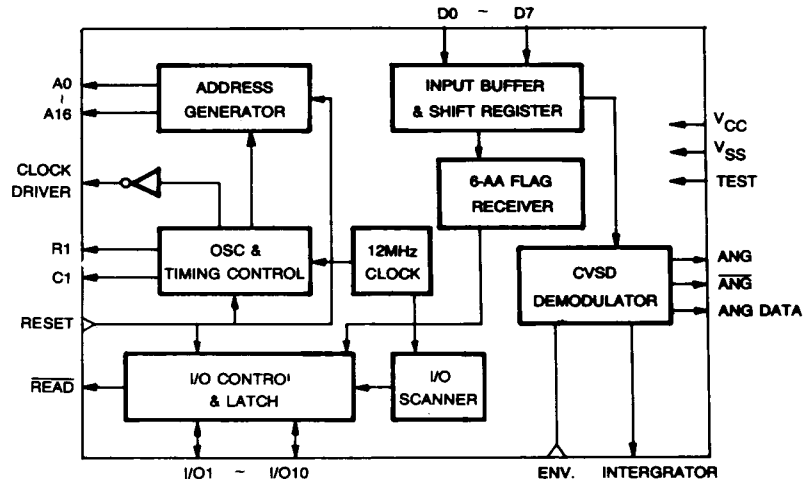
Application

- Commercial
- Industrial
- Security
- Telecommunication

Pin Assignment



Block Diagram



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Absolute Maximum Ratings*

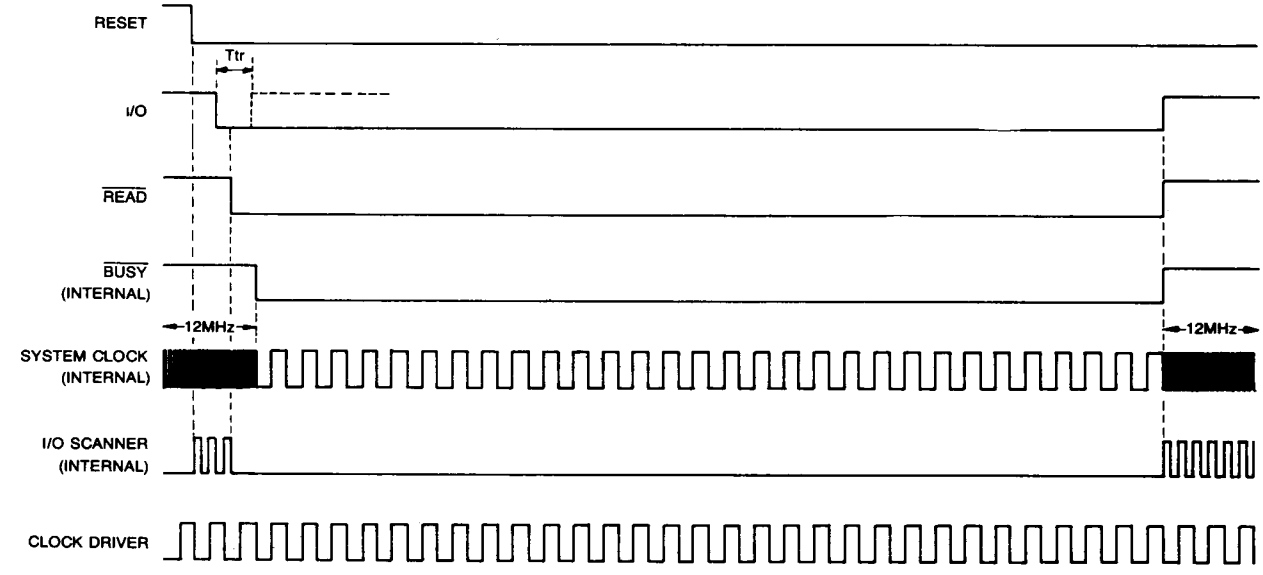
Supply Voltage, $V_{CC} - V_{SS}$ . . . . . 0 to 7V
Input Voltage, V_{IN} . . . . . V_{SS} to V_{DD}
Operating Temperature, T_{OP} . . . . . $-10^{\circ}C$ to $60^{\circ}C$
Storage Temperature, T_{ST} . . . . . $-20^{\circ}C$ to $80^{\circ}C$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Eletrical Characteristics (V_{DD} = 5V, Fosc = 32 KHz, unless otherwise specified.)

Symbol	Parameter		Limit			Units
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		3	5	6	V
I_{CC}	Stand-by Current			50		μA
I_{drive}	Clock Drive Current		12			mA
I_{sink}	Clock Sink Current		12			mA
V_{IH}	Input Voltage	High	3.5		5	V
V_{IL}		Low	0		1.5	V
I_{drive}	Output Current	Drive	3	4		mA
I_{sink}		Sink	3	4		mA
T_{reset}	Reset Pulse		500			nS
T_{tr}	I/O Input Pulse			35		μS
F_c	Internal Memory Serch Clock			12		MHz

Timing Diagram



Pin Name Description

A0 – A16
Address bus output.

READ
Output, active low. Active when any valid I/O input is being scanned.

D0 – D7
Data input.

TEST
For test purpose only. No connection shall be made

I/O 1 ~ I/O 10
Input/Output. Bi-directional, active low. A valid input pulse shall enable memory serch clock to read the right message. Output remain active when being read.

RESET:
Input, active high. When activated, all the internal counters are cleared and the chip is disabled.

ANG AND $\overline{\text{ANG}}$:
Analog signal outputs with opposite phase.

INTERGRATOR:
Output connected to external intergrator to produce envelope waveform.

ENVELOPE:
Input to be connected to external intergrator output.

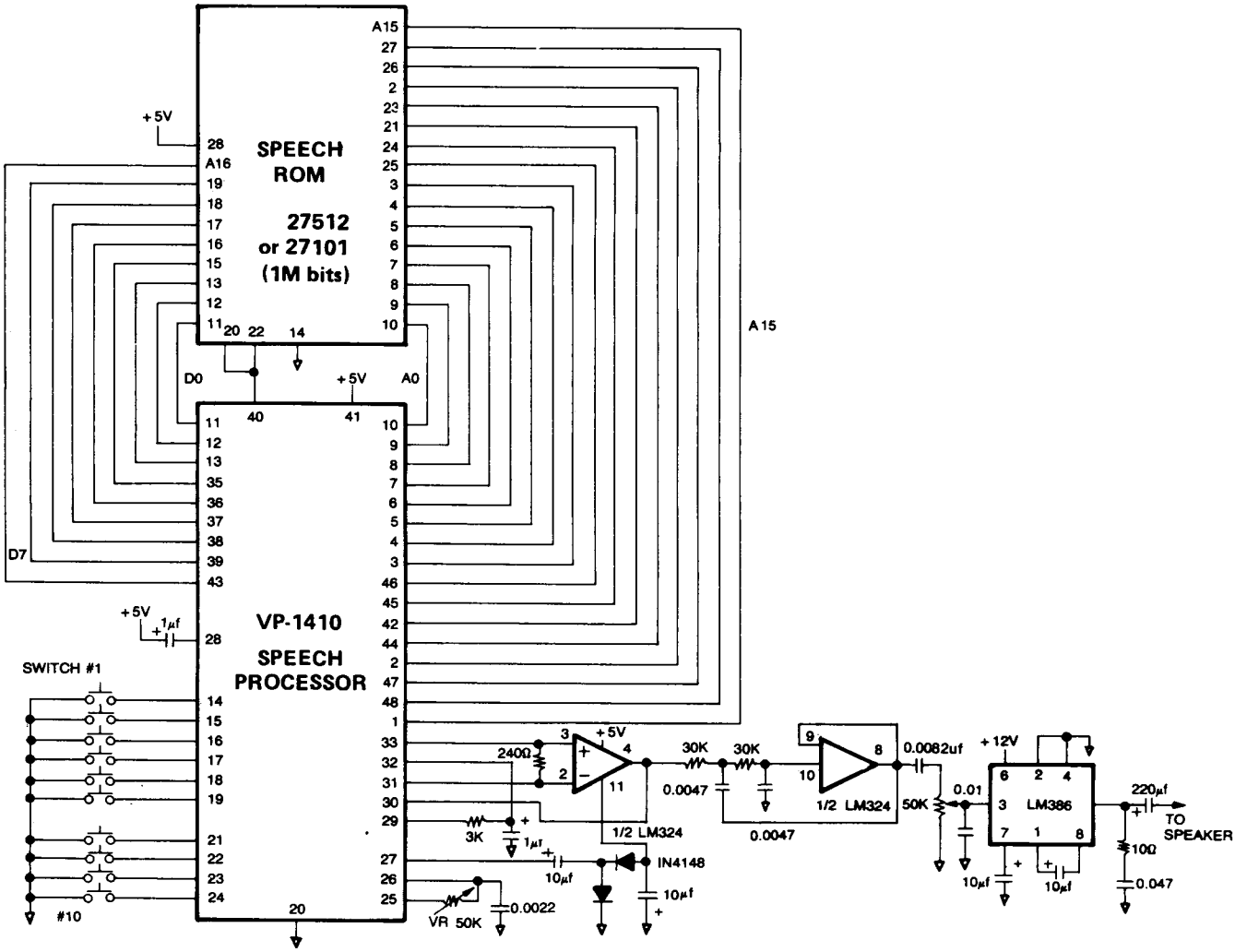
ANG DATA:
Analog signal to be connected to external comparator output.

R1, C1:
Oscillator pins of the demodulator clock. Use C1 as input when employing external clock.

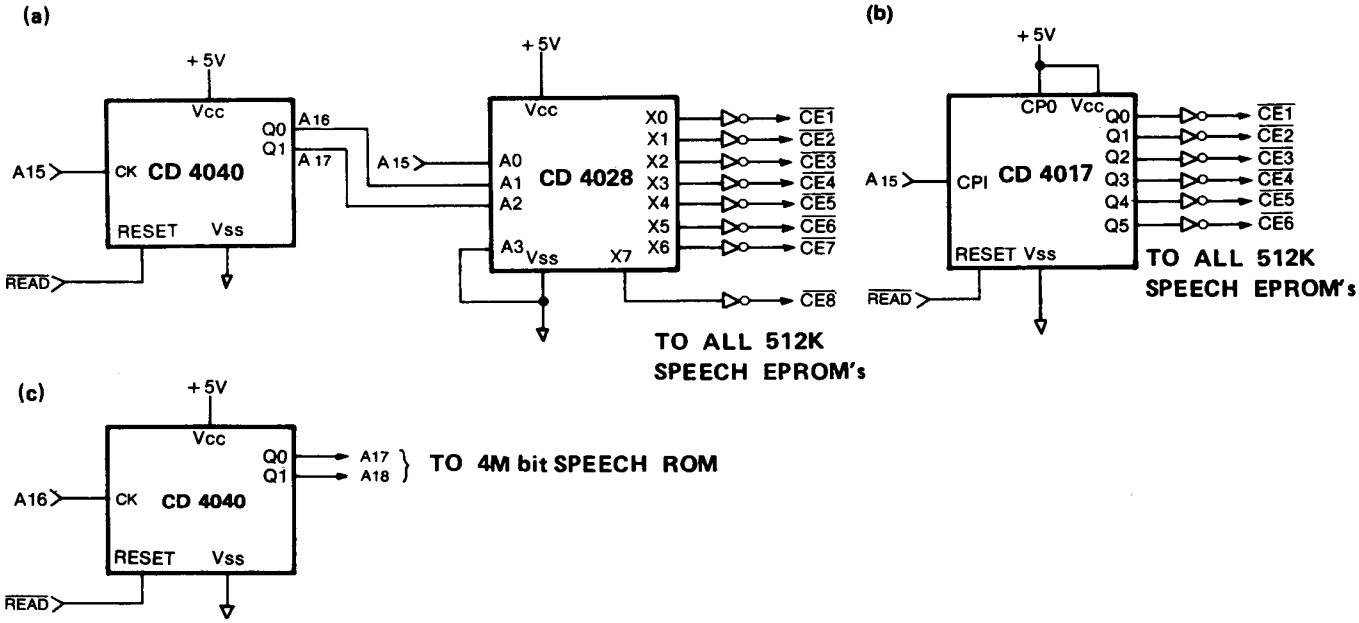
CLOCK DRIVER:
Output pin for the genration of negative voltage.

V_{DD} & Vss:
+3V ~ +6V power inputs.

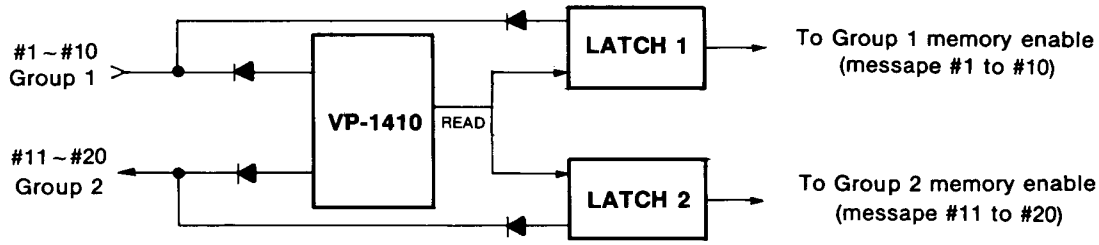
Tipical Application: Playback Module of 512K or 1M Speech ROM (Max. 10 messages)



Memory expansion/multiplexer circuits of VP-1410



Group expansion method of VP-1410



NOTICE: Eletech's products are sold by description only. Eletech reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

Eletech Enterprise Co., Ltd.
Microelectronics Division

HEADQUARTER:
12F-1, NO. 151 AN HO RD TAIPEI
TAIWAN, R.O.C.
TEL: (02) 704-3900 (REP.)
TLX: 25138 APIC FAX: 886-2-7088362

U.S. BRANCH OFFICE:
1262 E. KATELLA AVE. ANAHEM,
CA 92805
TEL: (714) 385-1707
FAX: (714) 385-1708

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