



VND5012AK-E

Double channel high side driver with analog current sense for automotive applications

Features

General

Max supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 36V
Max On-State resistance (per ch.)	R_{ON}	12 m Ω
Current limitation (typ)	I_{LIMH}	60 A
Off state supply current (TYP)	I_S	2 $\mu A^{(*)}$

(*) Typical value with all loads connected

Application

- All types of resistive, inductive and capacitive loads

Main

- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/ec european directive

Diagnostic Functions

- Proportional load current sense
- High current sense precision for wide range currents
- Current sense disable
- Thermal shutdown indication
- Very low current sense leakage

Protections

- Undervoltage shut-down
- Overvoltage clamp
- Output stuck to Vcc detection

Order codes

Package	Part number (Tube)	Part number (Tape & Reel)
PowerSSO-24 (slug down)	VND5012AK-E	VND5012AKTR-E



- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shut down
- Reverse battery protection (see [Figure 24](#))
- Electrostatic discharge protection

Description

The VND5012AK-E a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open.

When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears...

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1 Block diagram and pin description

Figure 1. Block Diagram

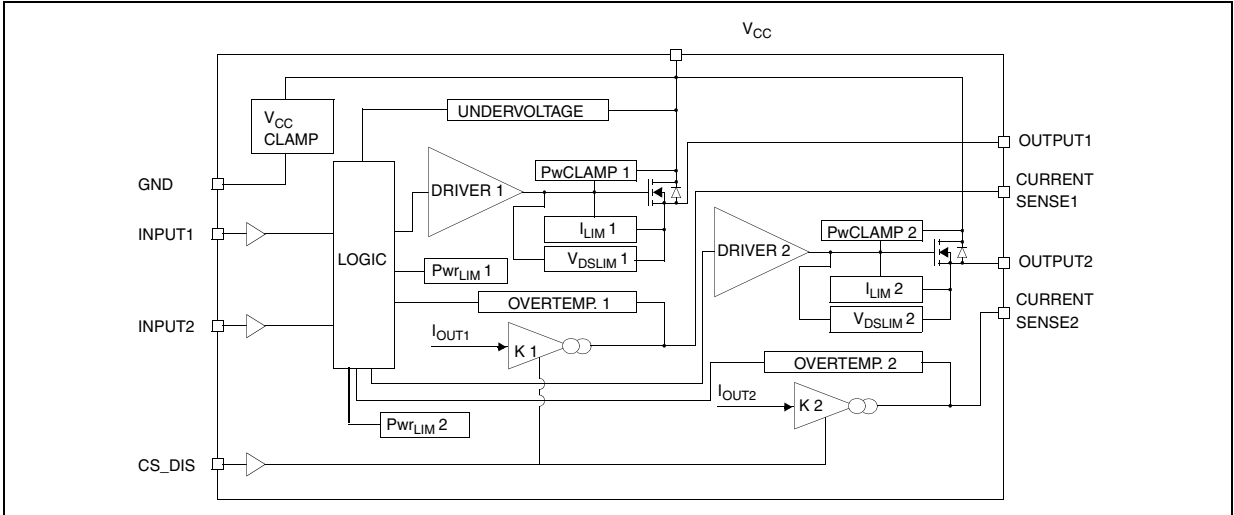
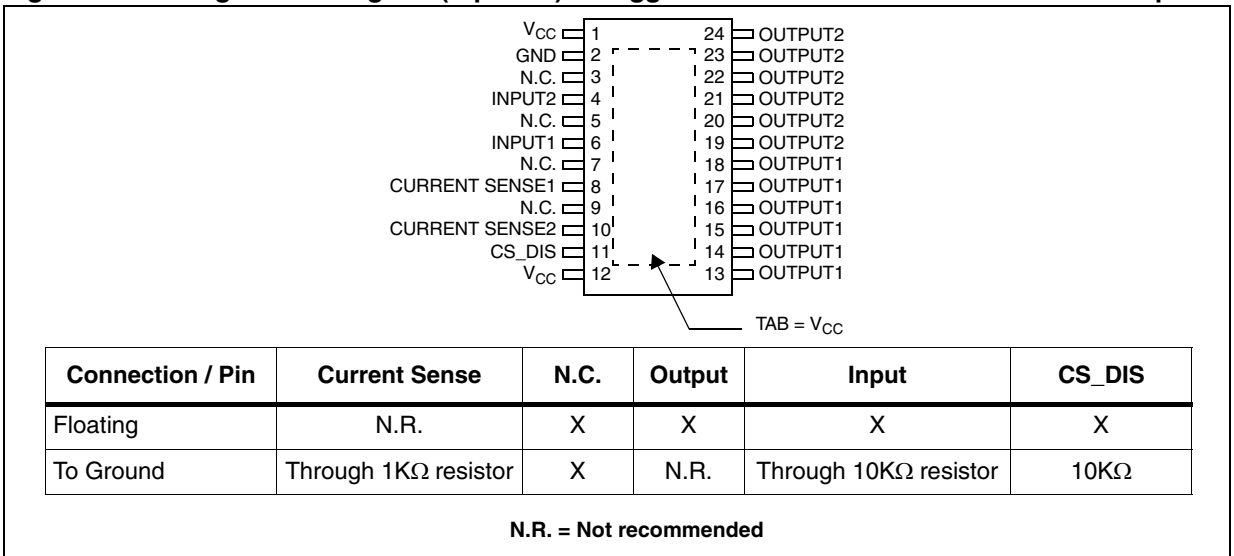


Table 1. Pin Function

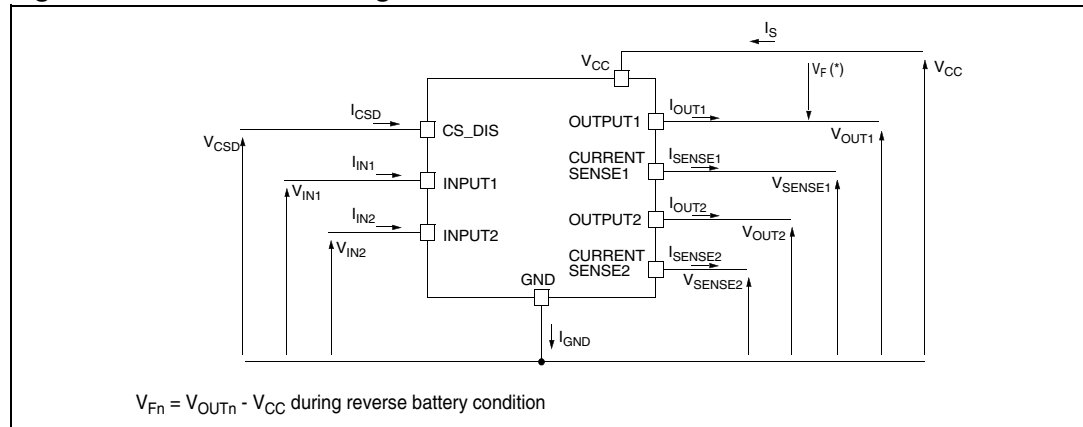
Name	Function
V _{CC}	Battery connection
OUTPUT _{1,2}	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE _{1,2}	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view) & suggested connections for unused and n.c. pins



2 Electrical specifications

Figure 3. Current and Voltage Conventions



2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-30	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC Reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
E_{MAX}	Maximum switching energy ($L=0.7mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_{OUT} = I_{limL}(Typ.)$)	283	mJ
V_{ESD}	Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)	4000	V
	– INPUT	2000	V
	– CURRENT SENSE	4000	V
	– CS_DIS	5000	V
	– OUTPUT	5000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	$^\circ C$
T_{stg}	Storage temperature	-55 to 150	$^\circ C$

2.2 Thermal Data

Table 3. Thermal Data

Symbol	Parameter	Max Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX) (With one channel ON)	0.4	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (Max.)	See Figure 26	°C/W

2.3 Electrical Characteristics

8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance ⁽²⁾	$I_{OUT}=5A$; $T_j=25^{\circ}C$ $I_{OUT}=5A$; $T_j=150^{\circ}C$ $I_{OUT}=5A$; $V_{CC}=5V$; $T_j=25^{\circ}C$			12 24 16	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	$I_S=20mA$	41	46	52	V
I_S	Supply current	Off State; $V_{CC}=13V$; $T_j=25^{\circ}C$; $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V$ On State; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0A$		2 ⁽¹⁾ 3	5 ⁽¹⁾ 6	μA mA
$I_{L(off)}$	Off state output current ⁽²⁾	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$ $V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$	0 0	0.01	3 5	μA
V_F	Output - V_{CC} diode voltage ⁽²⁾	$-I_{OUT}=8A$; $T_j=150^{\circ}C$			0.7	V

(1) PowerMOS leakage included.

(2) For each channel.

Table 5. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=2.6\Omega$ (see Figure 6)		20		μs
$t_{d(off)}$	Turn-off delay time	$R_L=2.6\Omega$ (see Figure 6)		35		μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L=2.6\Omega$	see Figure 19			V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L=2.6\Omega$	see Figure 20			V/μs
W_{ON}	Switching energy losses during t_{won}	$R_L=2.6\Omega$ (see Figure 6)		1.1		mJ
W_{OFF}	Switching energy losses during t_{woff}	$R_L=2.6\Omega$ (see Figure 6)		0.7		mJ

Table 6. Logic input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN}=0.9V$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN}=2.1V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	5.5	-0.7	7	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	$V_{CSD}=0.9V$	1			μA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	$V_{CSD}=2.1V$			10	μA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	$I_{CSD}=1mA$ $I_{CSD}=-1mA$	5.5	-0.7	7	V V

Table 7. Protections and Diagnostics ⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	$V_{CC}=13V$ $5V < V_{CC} < 36V$	42	60	84 84	A A
I_{limL}	Short circuit current during thermal cycling	$V_{CC}=13V$ $T_R < T_J < T_{TSD}$		24		A
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}C$
T_R	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}C$
T_{RS}	Thermal reset of STATUS		135			$^{\circ}C$
T_{HYST}	Thermal hysteresis ($T_{TSD}-T_R$)			7		$^{\circ}C$
t_{SDL}	Status Delay in Overload Conditions	$T_J > T_{TSD}$			20	μs
V_{DEMAG}	Turn-off output voltage clamp	$I_{OUT}=2A$; $V_{IN}=0$; $L=6mH$	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V
V_{ON}	Output voltage drop limitation	$I_{OUT}=0.4A$; $T_J = -40^{\circ}C \dots +150^{\circ}C$ (see Figure 24)		25		mV

(1) To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 8. Current Sense (8V<V_{CC}<16V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} =0.25A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C...150°C	2780	5580	8390	
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =5A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C...150°C	3590	5100	6630	
		I _{OUT} =5A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = 25°C...150°C	4110	5100	6090	
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =10A; V _{SENSE} =4V; V _{CSD} =0V; T _j =-40°C	4400	5090	5930	
		I _{OUT} =10A; V _{SENSE} =4V; V _{CSD} =0V; T _j =25°C...150°C	4600	5090	5590	
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =25A; V _{SENSE} =4V; V _{CSD} =0V; T _j =-40°C	4820	5060	5420	
		I _{OUT} =25A; V _{SENSE} =4V; V _{CSD} =0V; T _j =25°C...150°C	4860	5060	5250	
I _{SENSE0}	Analog sense leakage current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _j =-40°C...150°C	0		1	μA
		V _{CSD} =0V; V _{IN} =5V; T _j =-40°C...150°C	0		2	μA
		I _{OUT} =2A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =5V; T _j =-40°C...150°C	0		1	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} =15A; V _{CSD} =0V	5			V
V _{SENSEH}	Analog sense output voltage in overtemperature condition	V _{CC} =13V; R _{SENSE} =3.9KΩ		9		V
I _{SENSEH}	Analog sense output current in overtemperature condition	V _{CC} =13V; V _{SENSE} =5V		8		mA
t _{DSENSE1H}	Delay Response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		50	100	μs
t _{DSENSE1L}	Delay Response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		5	20	μs
t _{DSENSE2H}	Delay Response time from rising edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE max} (see Figure 4)		270	600	μs
t _{DSENSE2L}	Delay Response time from falling edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =10% of I _{SENSE max} (see Figure 4)		100	250	μs

Figure 4. Current Sense Delay Characteristics

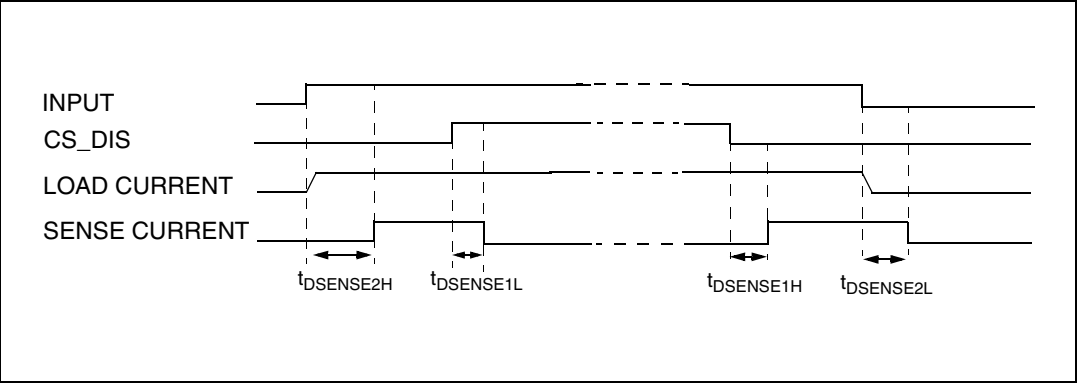


Figure 5. $I_{\text{OUT}}/I_{\text{SENSE}}$ Vs. I_{OUT} (see [Table 8](#) for details)

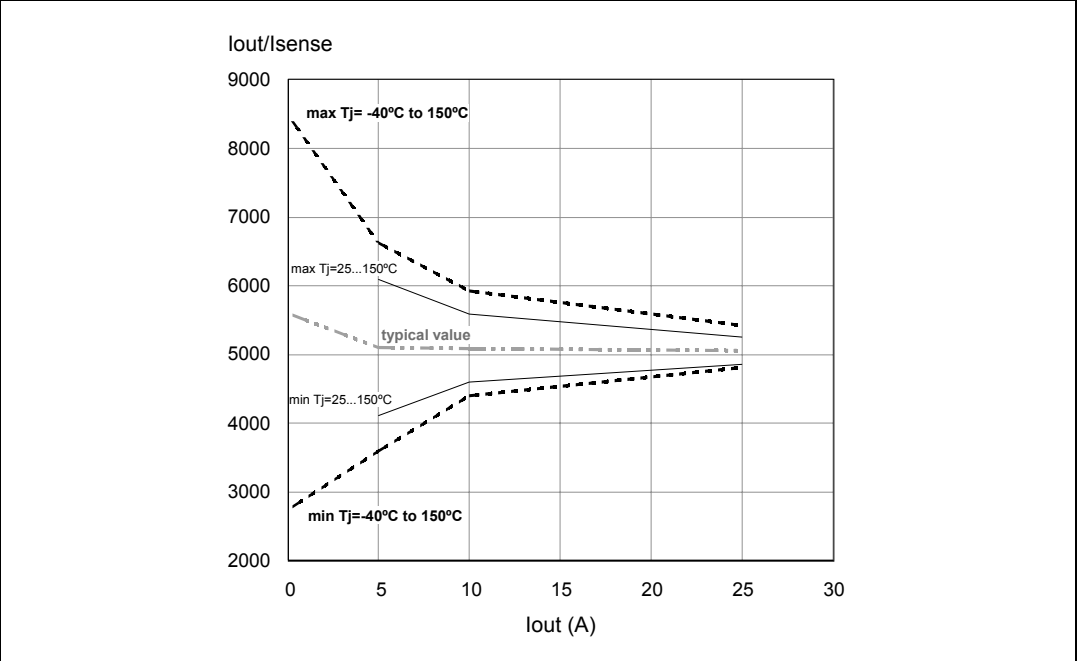


Table 9. Truth table

CONDITIONS	INPUT	OUTPUT	SENSE ($V_{CSD}=0V$) ⁽¹⁾
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND ($R_{sc} \leq 10\text{ m}\Omega$)	L H H	L L L	0 0 if $T_j < T_{TSD}$ V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

(1) If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 6. Switching characteristics

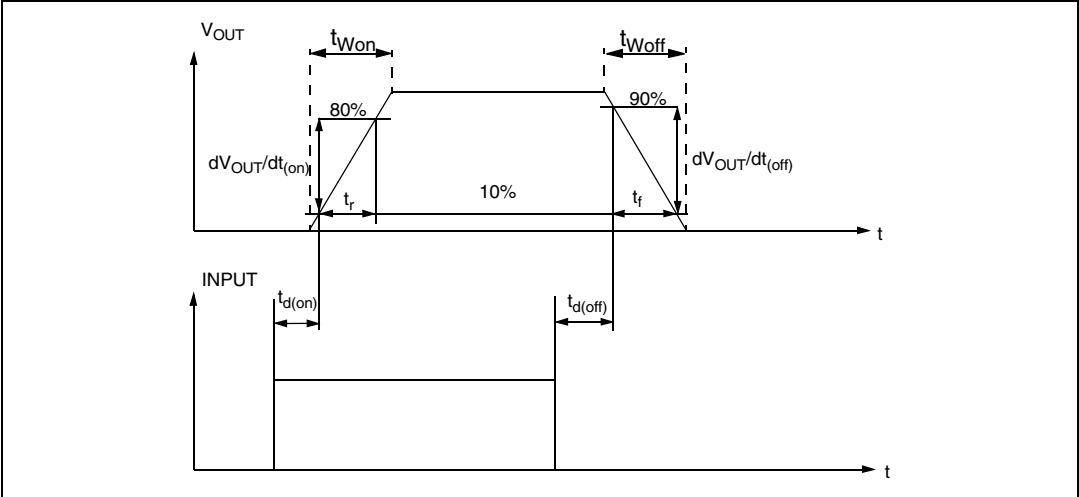


Figure 7. Output Voltage Drop Limitation

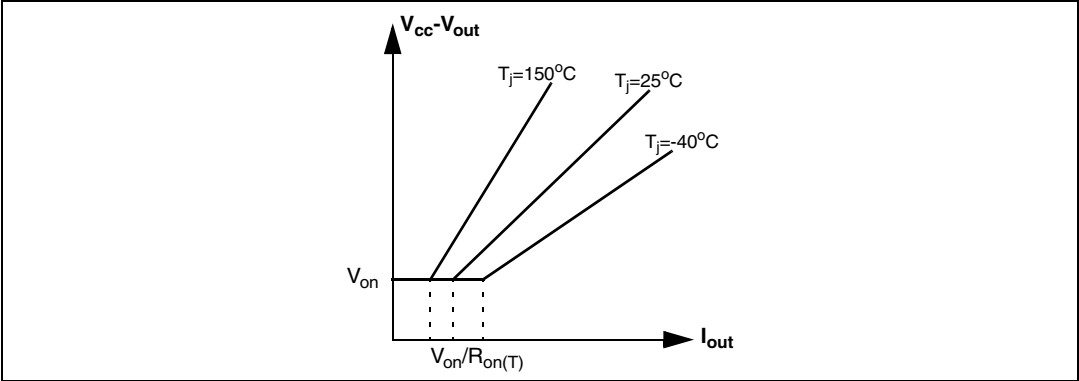


Table 10. Electrical Transient Requirements

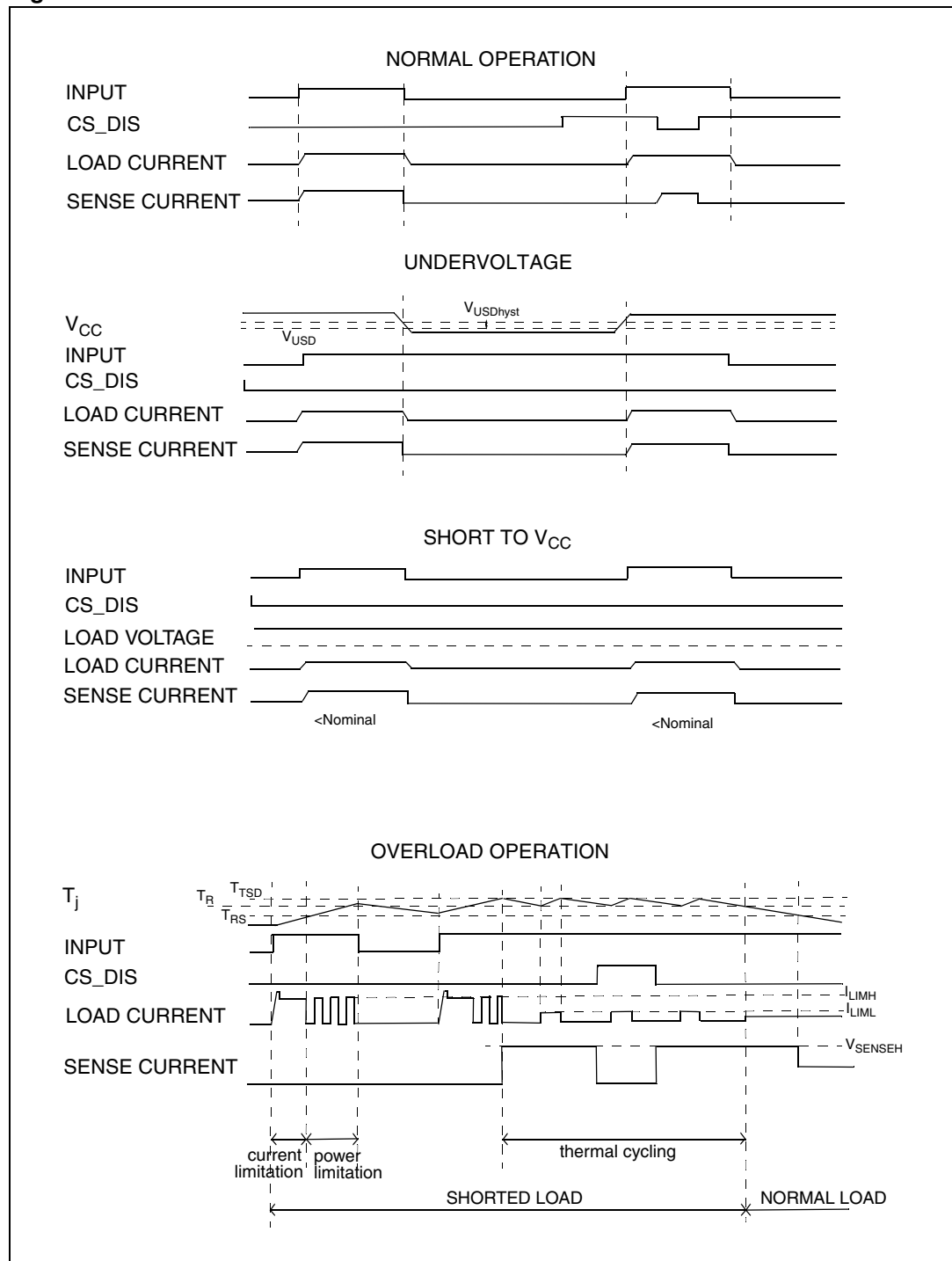
ISO 7637-2: 2004(E) Test Pulse	TEST LEVELS		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b ⁽¹⁾	+40V	+40V	1 pulse			400 ms, 2 Ω

ISO 7637-2: 2004(E) Test Pulse	TEST LEVEL RESULTS	
	III	IV
1	C	C
2	C	C
3a	C	C
3b	C	C
4	C	C
5	C	C

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

(1) For load dump exceeding the above value a centralized suppressor must be adopted.

Figure 8. Waveforms



2.4 Electrical characteristics curves

Figure 9. Off State Output Current

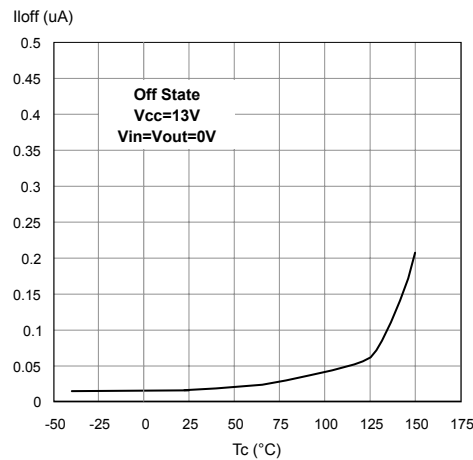


Figure 10. High Level Input Current

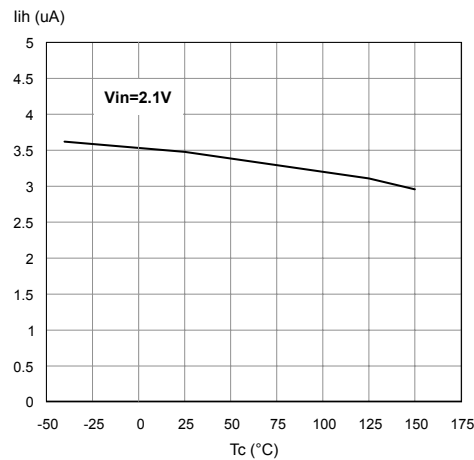


Figure 11. Input Clamp Voltage

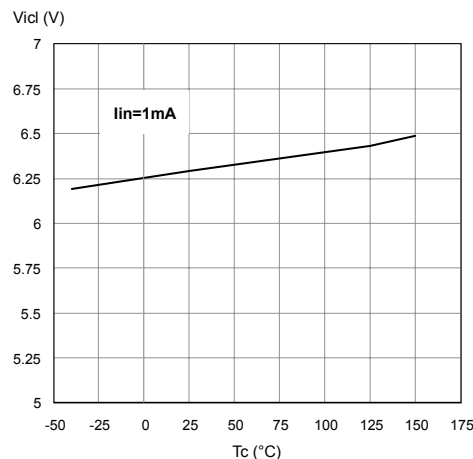


Figure 12. Input High Level

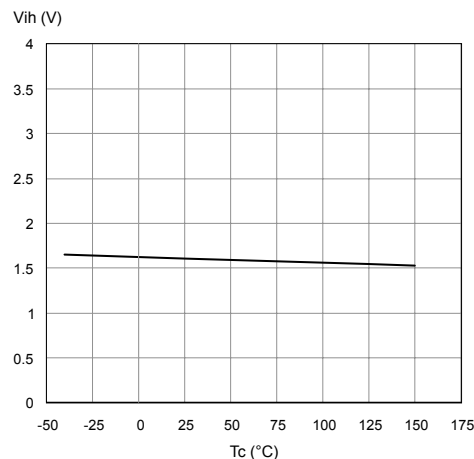


Figure 13. Input Low Level

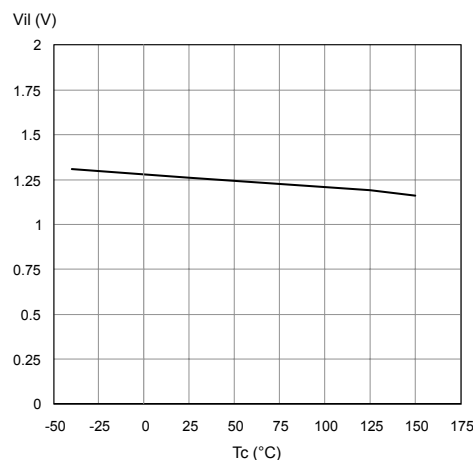


Figure 14. Input Hysteresis Voltage

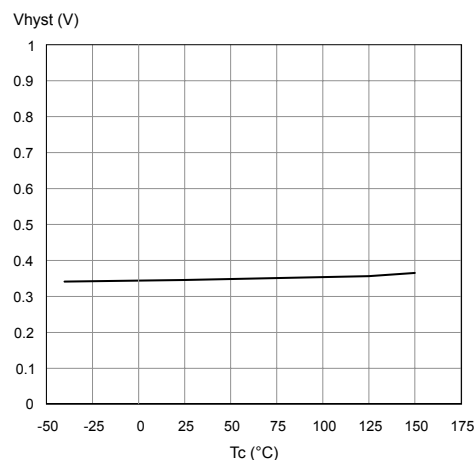


Figure 15. On State Resistance Vs. T_{case}

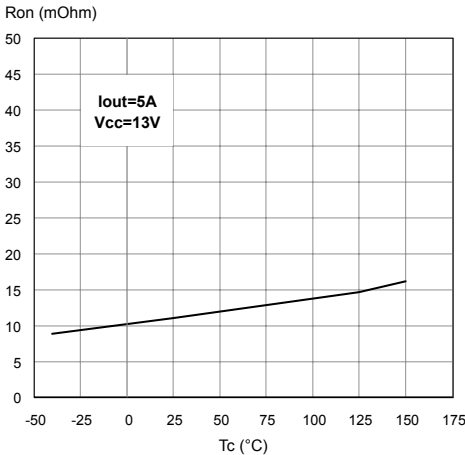


Figure 16. On State Resistance Vs. V_{CC}

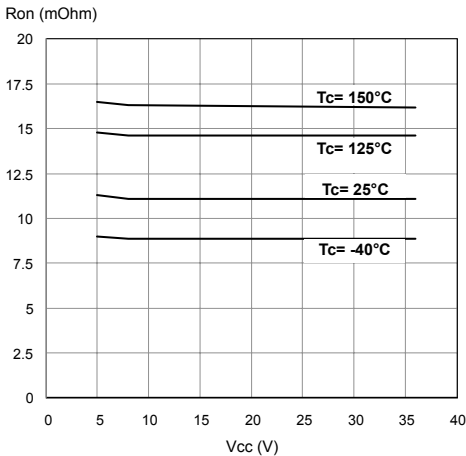


Figure 17. Undervoltage Shutdown

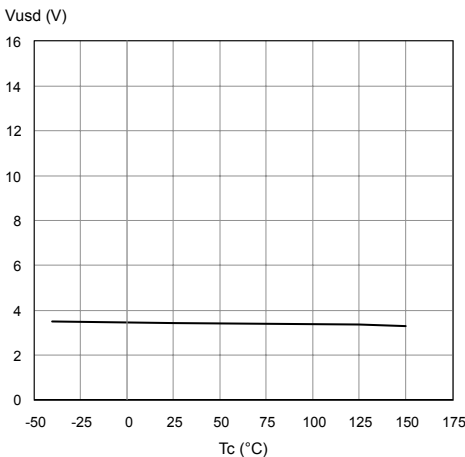


Figure 18. I_{LIMH} Vs. T_{case}

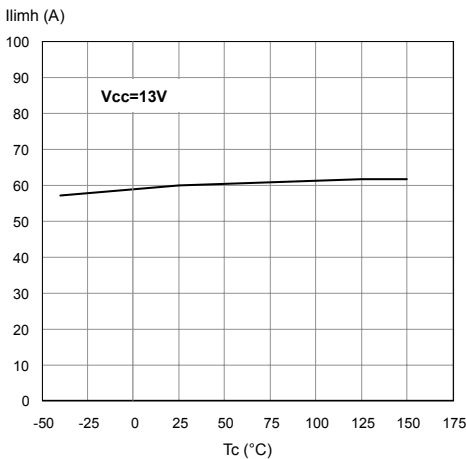


Figure 19. Turn-on Voltage Slope

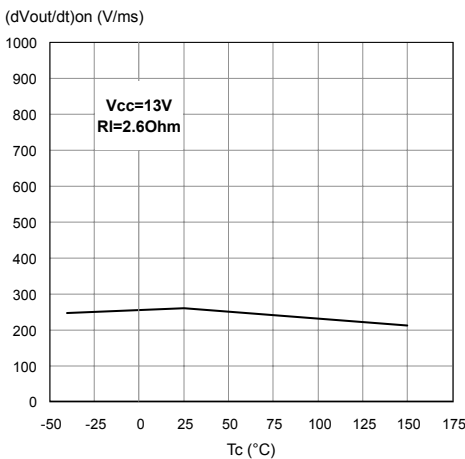


Figure 20. Turn-off Voltage Slope

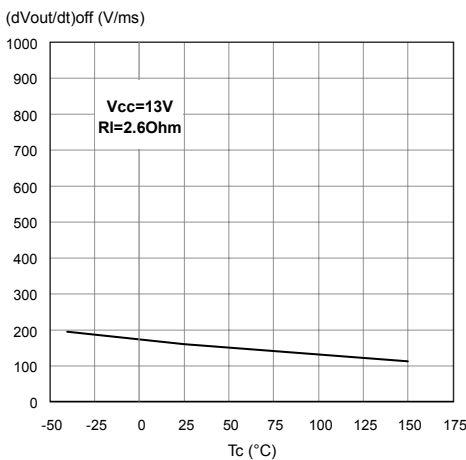


Figure 21. CS_DIS High Level Voltage

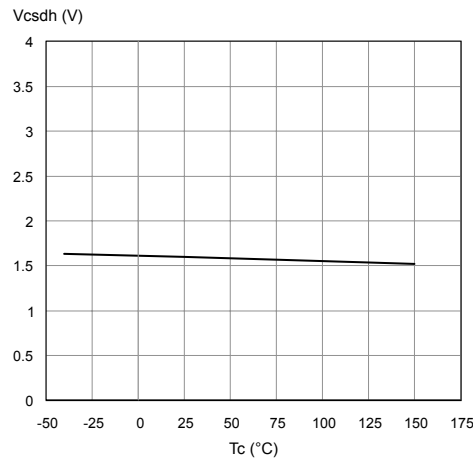


Figure 22. CS_DIS Clamp Voltage

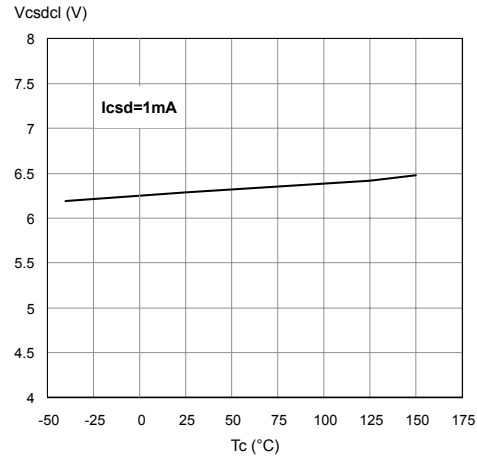
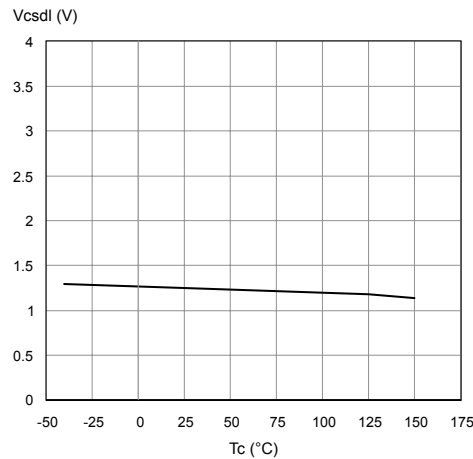
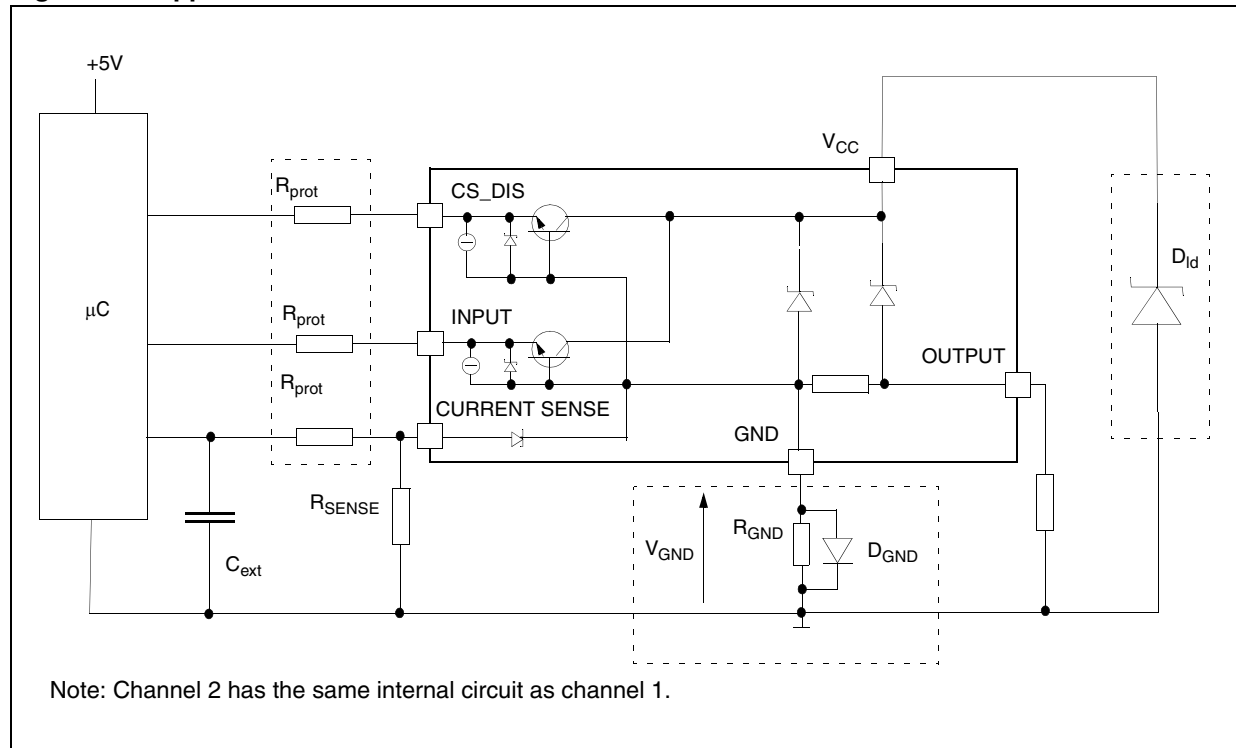


Figure 23. CS_DIS Low Level Voltage



3 Application Information

Figure 24. Application schematic



3.1 GND Protection Network Against Reverse Battery

3.1.1 Solution 1:

Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2:

A diode (D_{GND}) in the ground line.

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load Dump Protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 μC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For $V_{CCpeak} = -100V$ and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

4 Package and PCB Thermal Data

4.1 PowerSSO-24 Thermal Data

Figure 25. PowerSSO-24 PC Board

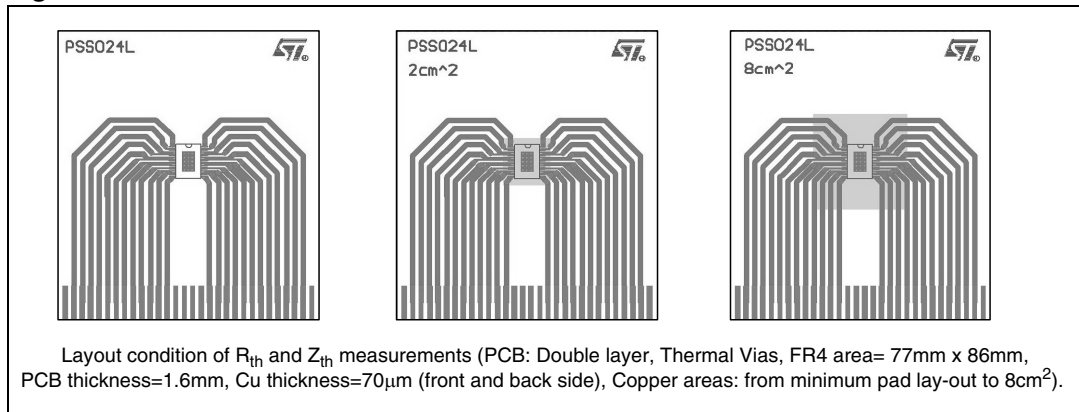


Figure 26. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

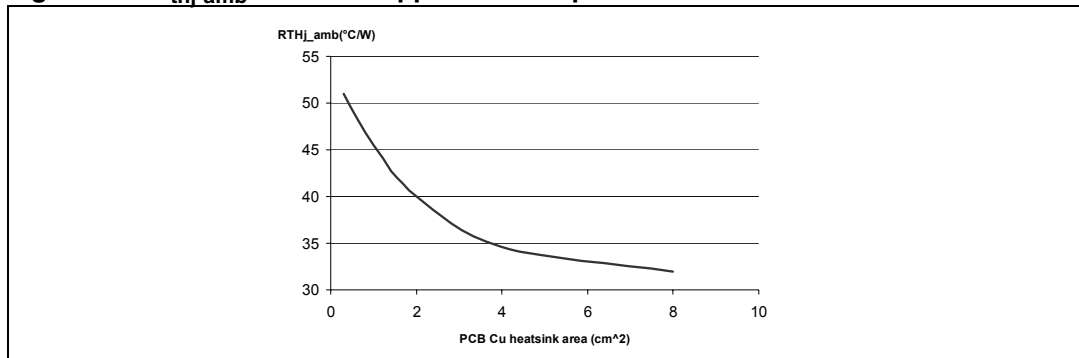
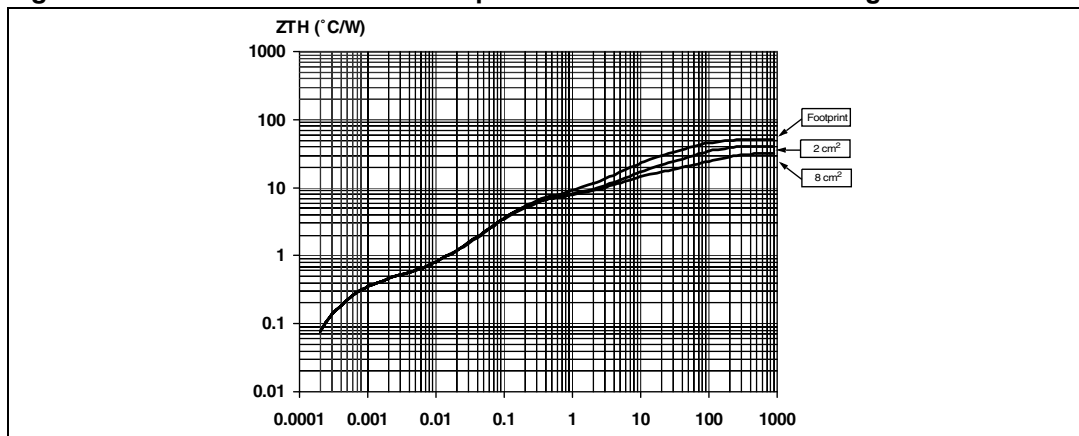


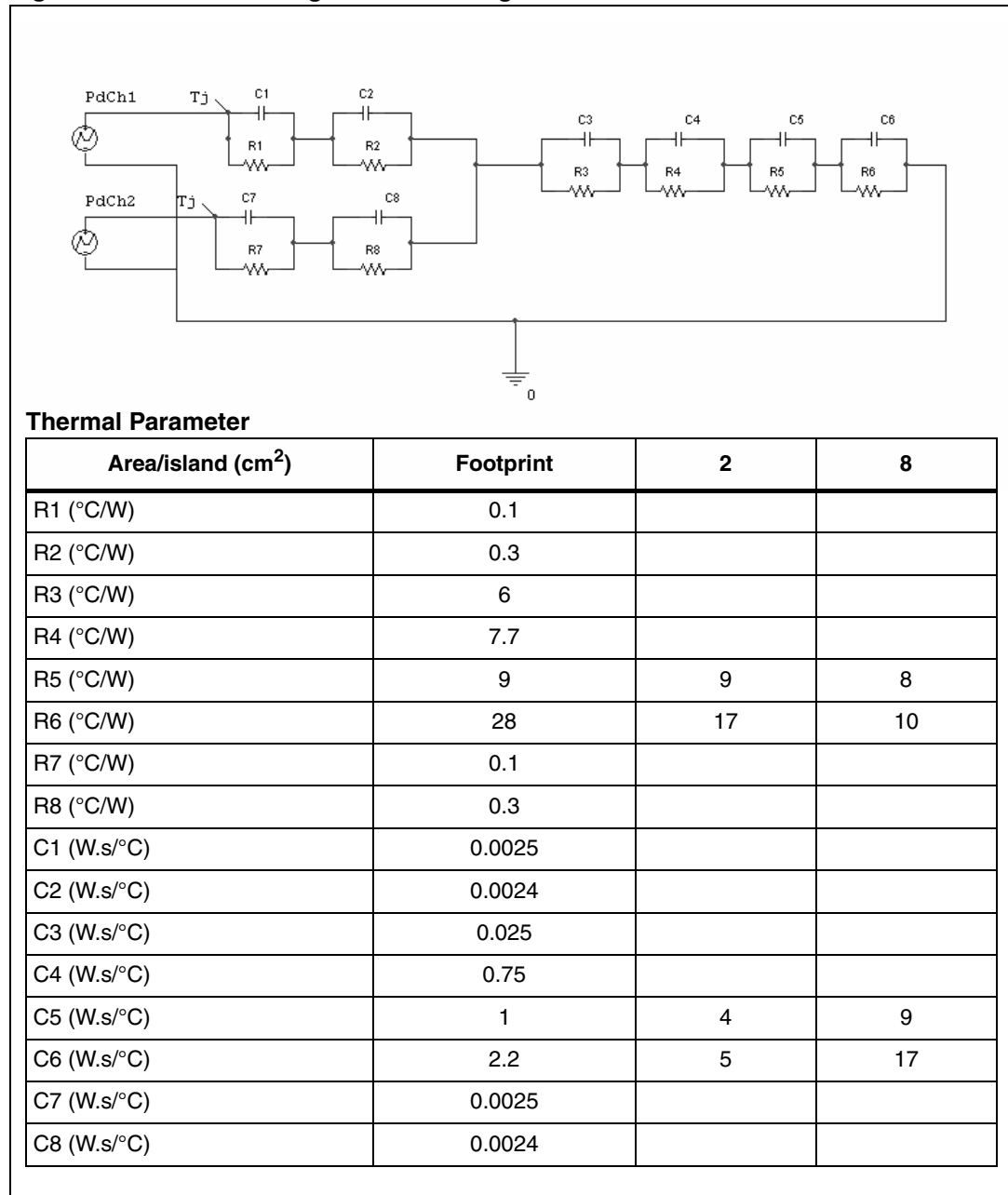
Figure 27. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse



Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 28. Thermal Fitting Model of a Single Channel HSD in PowerSSO-24

5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.1 Package Mechanical

Figure 29. PowerSSO-24™ Package Dimensions

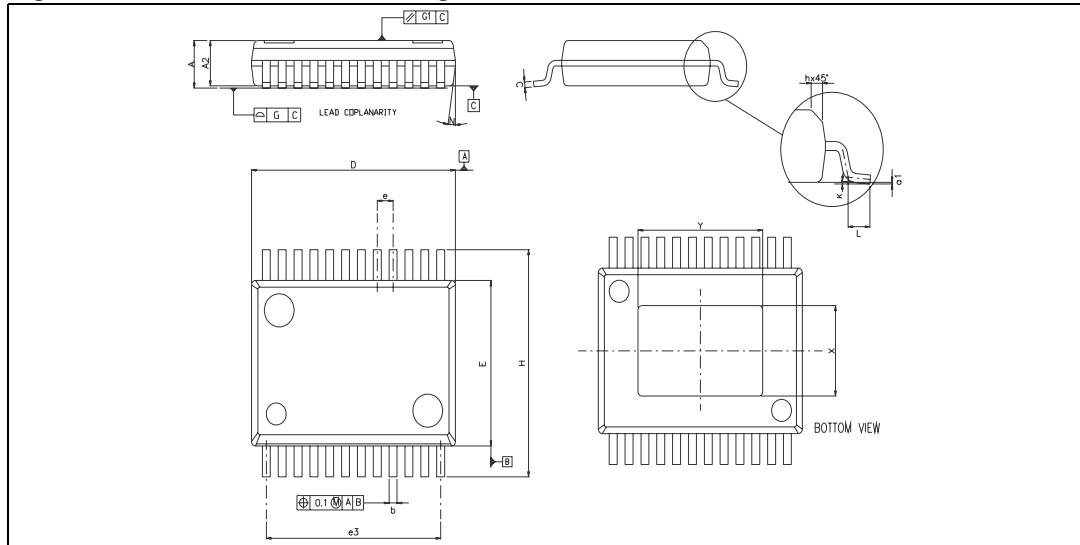


Table 11. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

5.2 Packing information

Figure 30. PowerSSO-24 Tube Shipment (No Suffix)

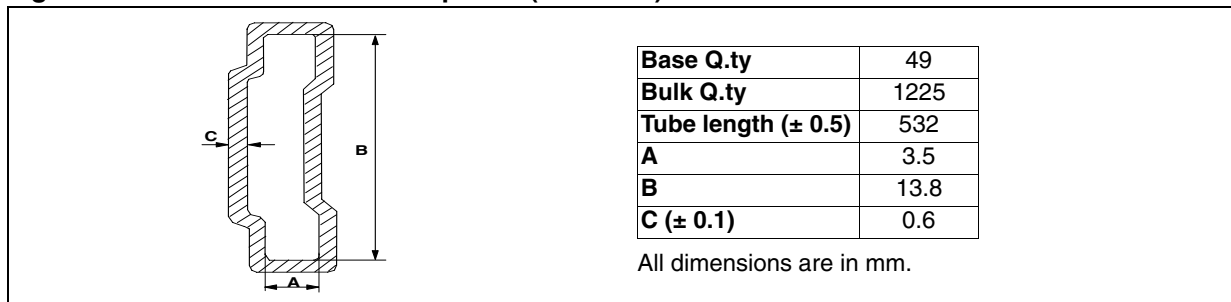
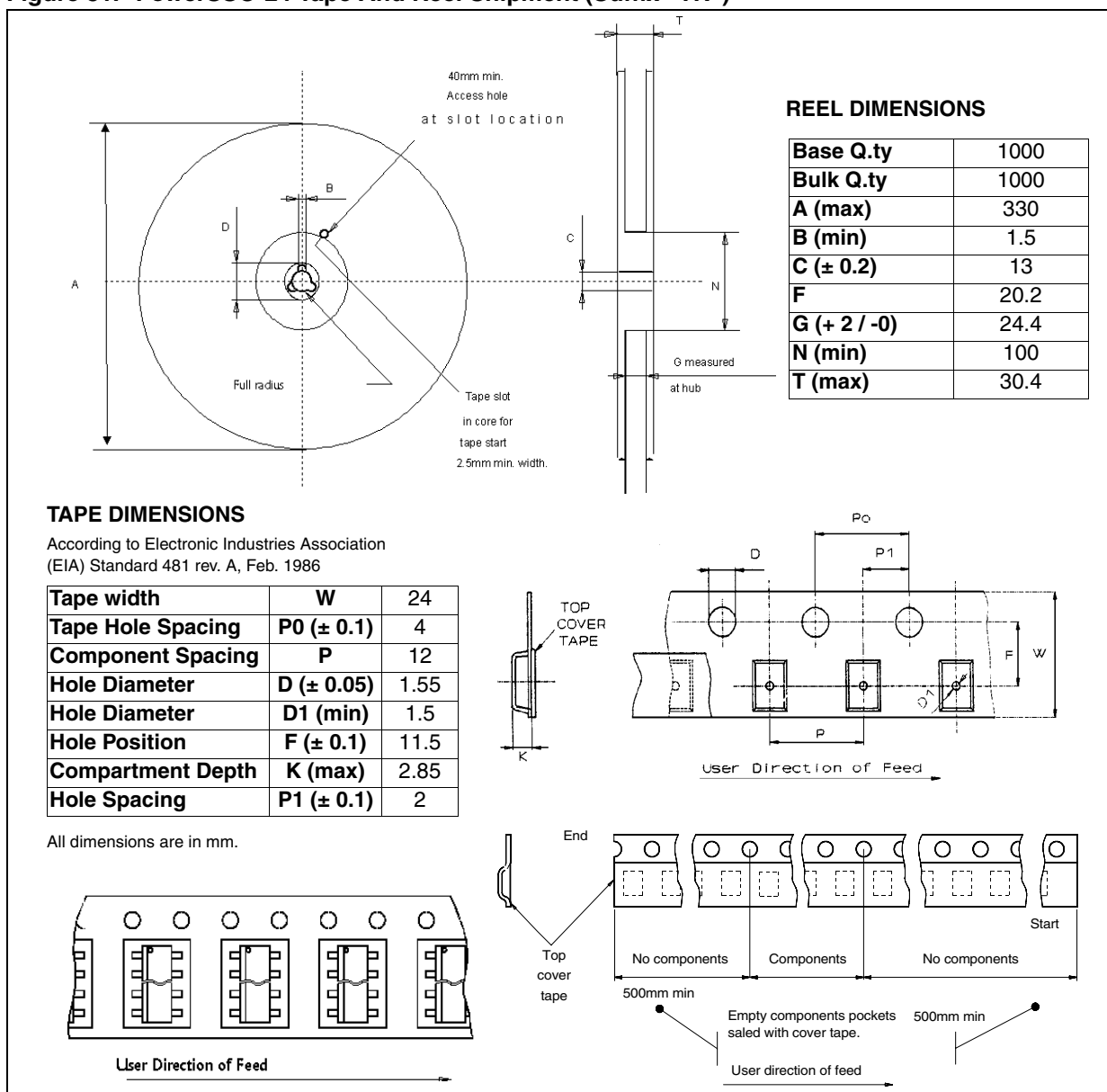


Figure 31. PowerSSO-24 Tape And Reel Shipment (Suffix "TR")



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
10-Apr-2006	1	Initial release.

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