μPD71054
Programmable Timer/Counter

Description

The μPD71054 is a high-performance, programmable counter for microcomputer system timing control. Three 16-bit counters, each with its own clock input, gate input, and OUT pin, can be clocked from DC to 8 MHz. Under software control, the μPD71054 can generate accurate time delays. Initialize the counter, and the μPD71054 counts the delay, and interrupts the CPU when the task is complete. This eliminates the need for software timing loops.

The μPD71054 contains three counters capable of binary or BCD operation. There are six programmable count modes. The counters operate independently and each can be set to a different mode. Use address lines A_1, A_0 to select a counter and perform a read/write operation.

Features

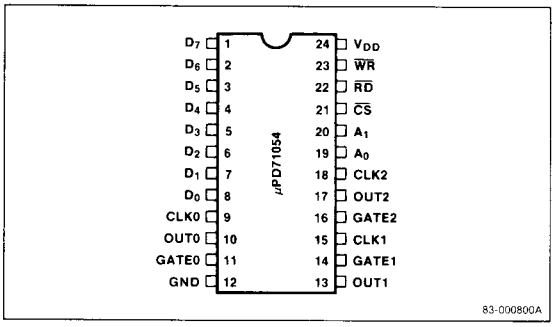
- ☐ Three independent 16-bit counters
- ☐ Six programmable counter modes
- ☐ Binary or BCD count
- ☐ Multiple latch command
- ☐ Clock rate DC (standby mode) to 8 MHz
- ☐ Low-power standby mode
- ☐ CMOS technology
- ☐ Single power supply, 5 V ±10%
- ☐ Industrial temperature range −40 to +85 °C
- ☐ 8 MHz and 10 MHz

Ordering Information

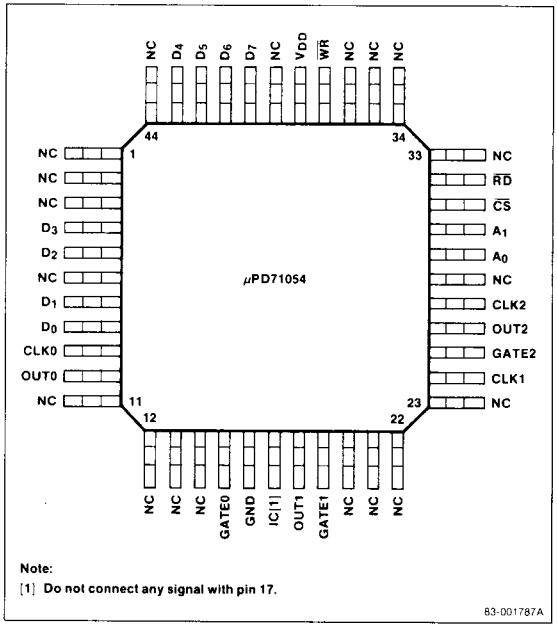
Part Number	Package Type
μPD71054C-8	24-pin plastic DIP
C-10	
G-8	44-pin plastic QFP (P44G-80-22)
GB-8	44-pin plastic QFP (P44GB-80-3B4)
GB-10	
L-8	28-pin PLCC
L-10	

Pin Configurations

24-Pin Plastic DIP



44-Pin Plastic QFP



Note:
[1] Do not connect any signal with pin 17.

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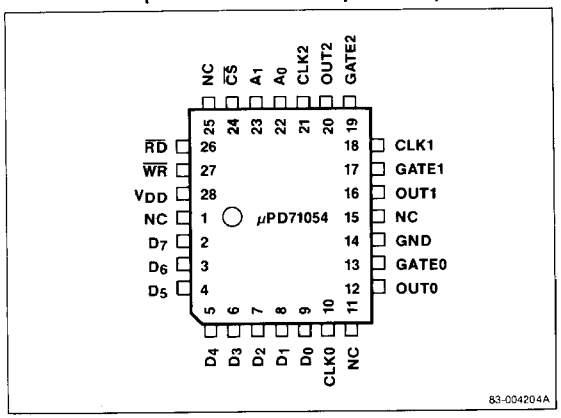
Pin Configurations (cont)

28-Pin PLCC (Plastic Leaded Chip Carrier)



Pin Identification

Symbol	Function
D_7-D_0	Three-state, bidirectional data bus
CLKn	Counter n clock output (n = 0-2)
OUTn	Counter n output (n = 0-2)
GATEn	Output to inhibit or trigger counter n (n = 0-2)
GND	Ground
IC	Internally connected
A_0-A_1	Select counter input 0, 1, or 2
$\overline{CS}$	Chip select
$\overline{RD}$	Read strobe
$\overline{WR}$	Write strobe
V_{DD}	+5 V
NC	Not connected

Pin Functions

D_7-D_0 [Data Bus]

These pins are an 8-bit three-state bidirectional data bus. This bus is used to program counter modes and to read status and count values. The data bus is active when $\overline{CS}$ = 0, and is high impedance when $\overline{CS}$ = 1.

CLKn [Counter Clock, n = 0-2]

These pins are the clock input that determine the count rate for counter n. The clock rate may be DC (standby mode) to 8 MHz.

OUTn [Counter Output, n = 0-2]

These are the output pins for counter n. A variety of outputs is available depending on the count mode. When the μPD71054 is used as an interrupt source, these pins can output an interrupt request signal.

GATEn [Counter Gate, n = 0-2]

These output pins inhibit or trigger counter n according to the mode selected.

A_1, A_0 [Address]

These input pins select the counter. A_1, A_0 equal to 00, 01, or 10 selects counter 0, 1, or 2, respectively. The control register is selected when A_1, A_0 equals 11. These pins are normally connected to the address bus.

$\overline{CS}$ [Chip Select]

When the $\overline{CS}$ input = 1, all the bits of the data bus become high impedance. $\overline{CS}$ must be low to access the μPD71054.

$\overline{RD}$ [Read Strobe]

The $\overline{RD}$ input must be low to read data from the μPD71054.

$\overline{WR}$ [Write Strobe]

The $\overline{WR}$ input must be low to write data to the μPD71054. The contents of the data bus are written to the μPD71054 at the rising edge of $\overline{WR}$.

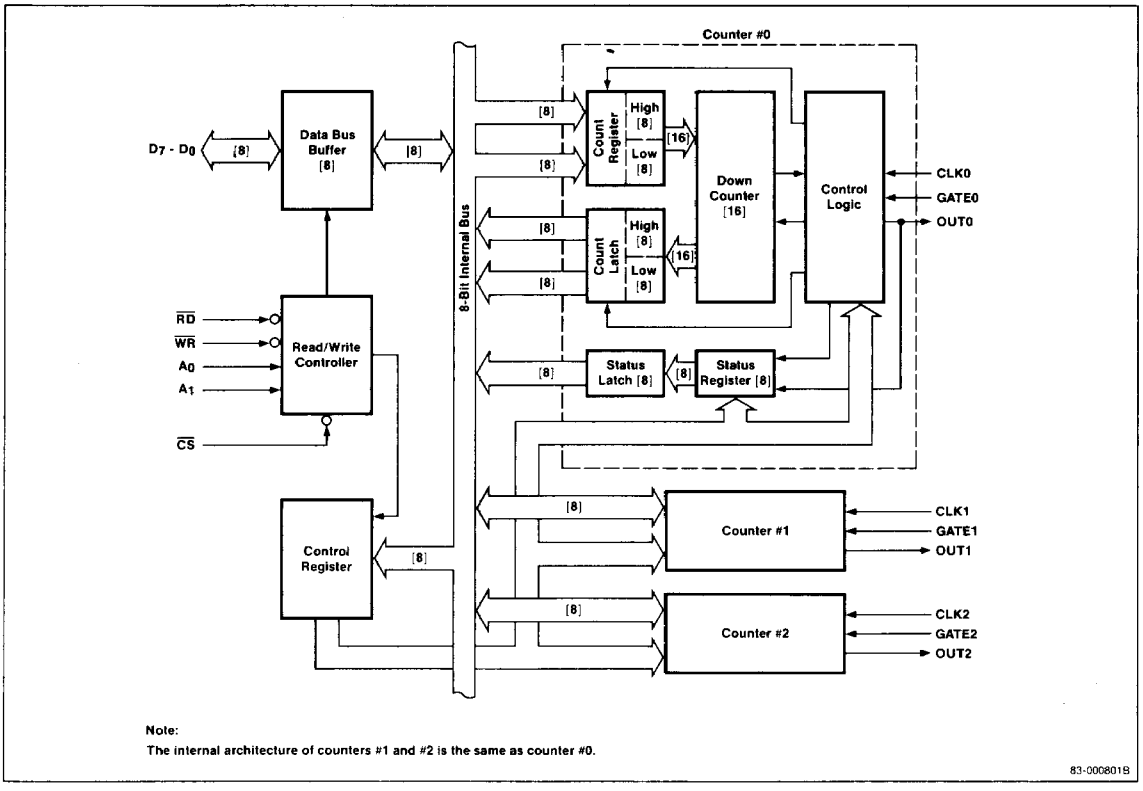
V_{DD} [Power]

+5 V.

GND [Ground]

Ground.

Block Diagram



Note:
The internal architecture of counters #1 and #2 is the same as counter #0.

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Block Functions

Data Bus Buffer

This is an 8-bit three-state bidirectional buffer that acts as an interface between the μPD71054 and the system data bus. The data bus buffer handles control commands, the count to be written to the count register, count data read from the count latch, and status data read from the status latch.

Read/Write Control

This circuit decodes signals from the system bus and sends control signals to other blocks of the μPD71054. A_1 and A_0 select one of the counters or the control register. A low signal on $\overline{RD}$ or $\overline{WR}$ selects a read or write operation. $\overline{CS}$ must be low to enable these operations.

Control Register

This is an 8-bit register into which is written the control command that determines the operating mode of the counter. Data is written to this register when the CPU executes an OUT command when A_1, A_0 = 11. The contents of this register cannot be read if the CPU executes an IN command when A_1, A_0 = 11. However, the multiple latch command allows you to read the mode and status of each counter.

Counter n [n = 0-2]

A 16-bit synchronous down counter performs the actual count operation within the counter. You can preset this counter and select binary or BCD operation.

The count register is a 16-bit register that stores the count when it is first written to the counter. The count is transferred to the down counter and a count operation for a specified number of counts begins.

The 8-bit width of the internal data bus permits the transfer of only eight bits at a time when the count is written to the count register. However, when data is written from the count register to the down counter, all 16 bits can be written at once. When the count is written to the count register while the counter is in read/write one byte mode, a 00H is written to the remaining byte of the register.

The count latch normally holds the current value of the down counter. If the contents of the down counter change, the contents of the count latch also change so that the two values are the same. When the μPD71054 receives a count latch command, the count latch latches the value of the down counter and holds it until the CPU can read it. When the data is read, the count latch returns to tracking the value of the down counter.

When the mode specified is written to the counter, the lower six bits of the control register are copied to the lower six bits of the 8-bit status register. The remaining two bits show the status of the OUT pin and the null count flag. When the multiple latch command is sent to the counter, the current value of the status register is latched into the status latch. This data is held in the latch until the CPU can read it.

The control logic controls each internal block according to the mode and the state of the CLK and GATE pins. The result is output to and sets the state of the OUT pin.

Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−40°C to 85°C
Storage temperature, T_{STG}	−65°C to +150°C
Power dissipation, PD_{MAX}	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = +25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		10	pF	fc = 1 MHz
I/O capacitance	$C_{I/O}$		20	pF	Unmeasured pins returned to 0 V

DC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5$ V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage high	V_{IH}	2.2		V_{DD} + 0.3	V	
Input voltage low	V_{IL}	−0.5		0.8	V	
Output voltage high	V_{OH}	0.7 x V_{DD}			V	$I_{OH} = -400$ μA
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.5$ mA
Input leakage current high	I_{LIH}			10	μA	$V_I = V_{DD}$
Input leakage current low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current high	I_{LOH}			10	μA	$V_O = V_{DD}$
Output leakage current low	I_{LOL}			−10	μA	$V_O = 0$ V
Supply current μPD71054	I_{DD1}			30	mA	Normal
	I_{DD2}		2	50	μA	Stand-by mode
μPD71054-10	I_{DD1}		10	20	mA	Normal
	I_{DD2}		2	50	μA	Stand-by mode

AC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = 5\ V \pm 10\%$

Parameter	Symbol	8 MHz Limits Min	8 MHz Limits Max	10 MHz Limits Min	10 MHz Limits Max	Unit	Test Conditions
Read Cycle							
Address set-up to $\overline{RD}\downarrow$	t_{SAR}	30		20		ns	
Address hold from $\overline{RD}\uparrow$	t_{HRA}	10		0		ns	
$\overline{CS}$ set-up to $\overline{RD}\downarrow$	t_{SCR}	0		0		ns	
$\overline{RD}$ low level width	t_{RRL}	150		95		ns	
Data delay from $\overline{RD}\downarrow$	t_{DRD}		120		85	ns	$C_L = 150$ pF
Data float from $\overline{RD}\uparrow$	t_{FRD}	10	85	10	65	ns	$C_L = 20$ pF; $R_L = 2$ kΩ
Data delay from address	t_{DAD}		220		185	ns	$C_L = 150$ pF
Read recovery time	t_{RV}	200		165		ns	
Write Cycle							
Address set-up to $\overline{WR}\downarrow$	t_{SAW}	0		0		ns	
Address hold from $\overline{WR}\uparrow$	t_{HWA}	0		0		ns	
$\overline{CS}$ set-up to $\overline{WR}\downarrow$	t_{SCW}	0		0		ns	
$\overline{WR}$ low level width	t_{WWL}	160		95		ns	
Data set-up to $\overline{WR}\uparrow$	t_{SDW}	120		95		ns	
Data hold from $\overline{WR}\uparrow$	t_{HWD}	0		0		ns	
Write recovery time	t_{RV}	200		165		ns	
CLK and Gate Timing							
CLK cycle time	t_{CYK}	125	DC	100	DC	ns	
CLK high level width	t_{KKH}	60		30		ns	
CLK low level width	t_{KKL}	60		45		ns	
CLK rise time	t_{KR}		25		25	ns	
CLK fall time	t_{KF}		25		25	ns	
GATE high level width	t_{GGH}	50		50		ns	
GATE low level width	t_{GGL}	50		50		ns	
GATE set-up to CLK $\uparrow$	t_{SGK}	50		40		ns	
GATE hold from CLK $\uparrow$	t_{HKG}	50		50		ns	
Clock delay from $\overline{WR}\uparrow$ (count transfer)	t_{DWK}	100		40		ns	$t_{KKH} \geq 125$ ns
		$225 - t_{KKH}$		40		ns	$t_{KKH} \leq 125$ ns
Clock set-up to $\overline{WR}\uparrow$ (latch)	t_{SKW}	85		60		ns	
GATE delay from $\overline{WR}\uparrow$	t_{DWG}	0		0		ns	
OUT delay from GATE $\downarrow$	t_{DGO}		120		100	ns	$C_L = 150$ pF
OUT delay from CLK $\downarrow$	t_{DKO}		150		100	ns	$C_L = 150$ pF
OUT delay from $\overline{WR}\uparrow$ (initial out)	t_{DWO}		295		240	ns	$C_L = 150$ pF

Notes:

(1) AC timing test points for output $V_{OH} = 2.2$ V, $V_{OL} = 0.8$ V

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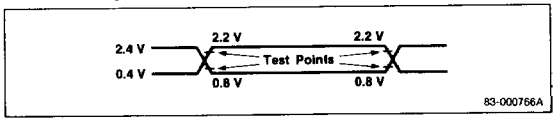
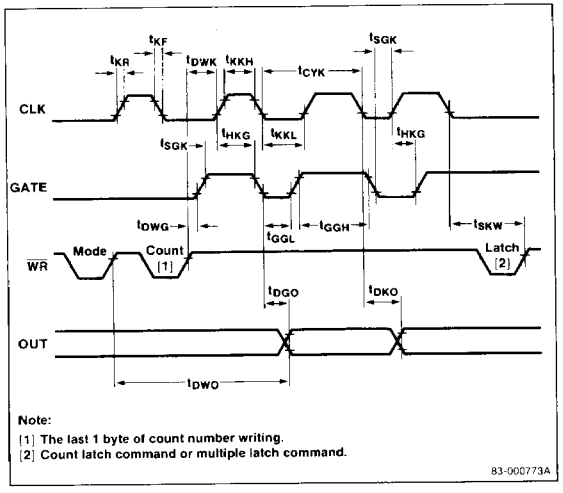
Timing Waveforms

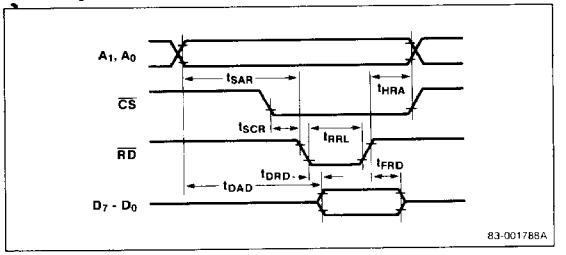
AC Test Input



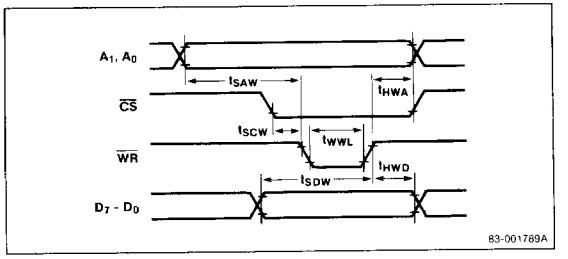
CLK and GATE Timing



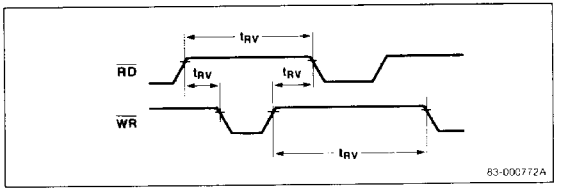
Read Cycle



Write Cycle



Read/Write Recovery



Functional Description

μPD71054 System Configuration Example

The CPU views the three counters and the control register as four I/O ports. A_1 and A_0 are connected to the A_1 and A_0 pins of the system address bus. $\overline{CS}$ is generated by decoding the address and $\overline{IO}$/MEM signals so that $\overline{CS}$ goes low when the address bus is set to the target I/O address and I/O is selected. These connections are shown in figure 1.

You can use the μPD71054 in memory-mapped I/O configurations. However, the decoding should be such that $\overline{CS}$ goes low when memory is selected.

Programming and Reading the Counter

The counter must be programmed and the operating mode specified before you can use the μPD71054. Once a mode has been selected for a counter, it operates in that mode until another mode is set. The count is written to the count register and when that data is transferred to the down counter, a new count operation begins. The current count and status can be read while the counter is in operation. Figure 2 outlines the steps of operation.

Programming the Counter

The μPD71054 is controlled by a microcomputer program. The program must write a control command to set the counter mode and write the count data that determines the length of the count operation. Table 1 shows the values for A_1 and A_0 that determine the target counter for write operations.

Table 1. Write Operations ($\overline{CS}$ = 0, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

A_1	A_0	Write Target
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word register

Control and Mode Setting

The control command must be written to set the counter mode before operating the counter. If a write operation is performed when A_1, A_0 = 11, a control command is written to the control register. Figure 3 shows the format of the 8-bit control command.

Bits SC1 and SC0 specify a counter or the multiple latch command. When a counter is chosen, the specifications described below apply to the counter.

Bits RMW1 and RMW2 specify the read/write operation to the counter or select the count latch command.

Bits CM2, CM1, and CM0 set the counter mode (0 to 5).

Bit BCD selects binary or BCD operation. The count may be 0 to FFFFH in binary mode or 0 to 9999 in BCD.

If a control command written to the counter specifies a mode, the lower six bits of the control command are copied to the lower six bits of the status register of the counter selected by SC1 and SC0. The mode selected remains in effect until a new mode is set. This is not true if the control command specifies the count latch or multiple latch command.

Writing the Count

The count is written to the counter after the mode is set. Set A_1, A_0 to specify the target counter as shown in table 1. A new count can be written to a counter at any time, but the read/write mode selected (when the mode was written) must be used when writing the count.

In high 1-byte and low 1-byte modes only, the higher or lower byte of the count register is written by the first write. The write operation ends and 00H is automatically written to the remaining byte by the μPD71054. In the 2-byte modes, the lower byte is written by the first write and the higher byte by the second.

For example, if the 2-byte count 8801H is written to a counter set in lower 1-byte mode, the lower byte (01H) is written first, followed by the higher byte (88H). Therefore, the data written to the count register is 0001H for the first write and 0088H for the second. This is shown in Table 2.

Table 2. Read/Write Mode and Count Write

Read/Write Mode	No. of Writes	Count Register Higher Byte	Count Register Lower Byte
Low 1-byte	1	00H	nnH
High 1-byte	1	nnH	00H
Low/High 2-byte	2	nnH (2nd write)	nnH (1st write)

nnH = Two-digit hexadecimal value

Reading the Counter

The following three methods allow you to read the contents of the down counter during operation. In particular, the multiple latch command reads the current count data and the counter mode or the state of the OUT pin. Table 3 shows the values of A_1, A_0 used to select the counter to be read.

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Figure 1. Typical System Configuration

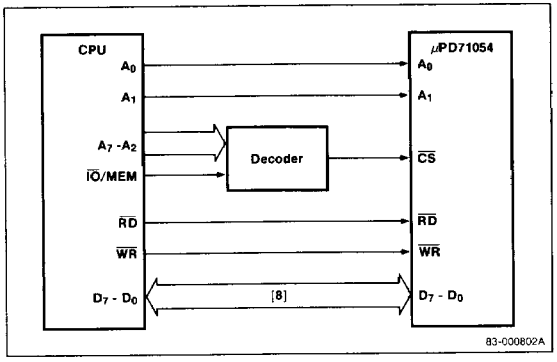


Figure 2. Basic Operating Procedure

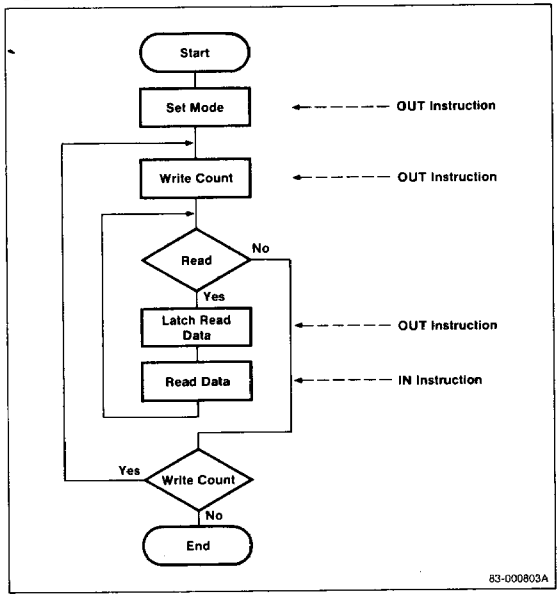


Figure 3. Control Register Format

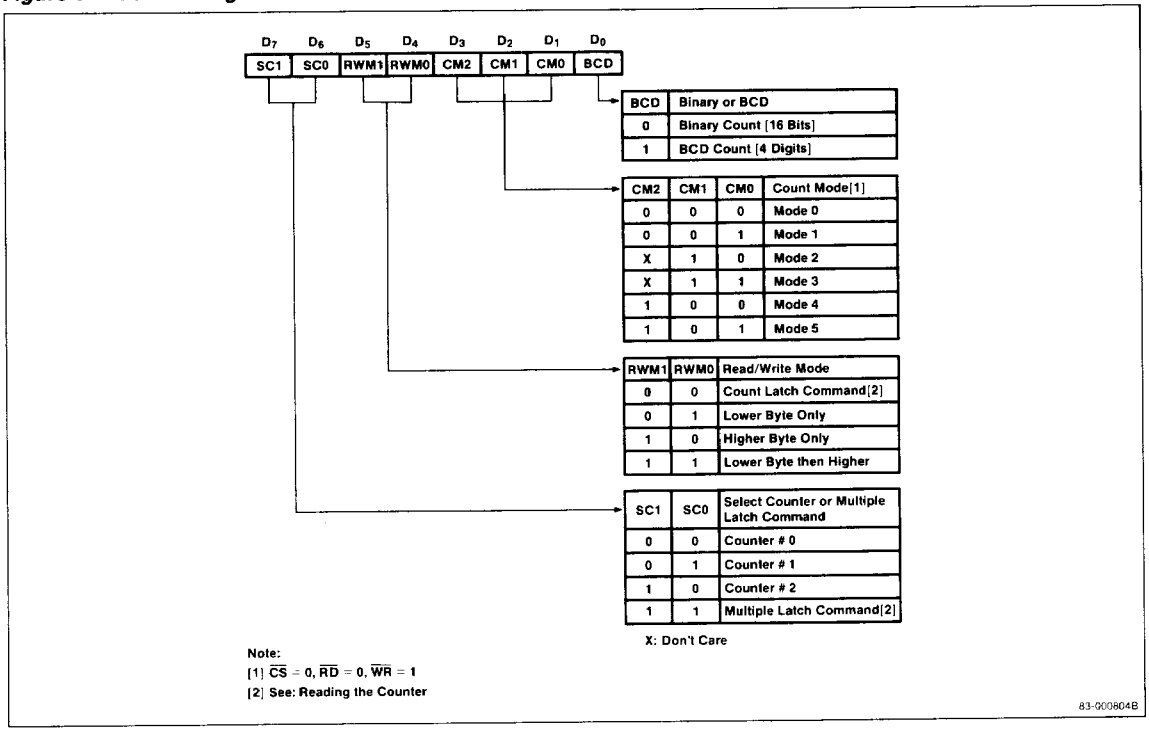


Table 3. Read Operations ($\overline{CS}$ = 0, $\overline{RD}$ = 0, $\overline{WR}$ = 1)

A_1	A_0	Read Target
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2

Directly Reading the Counter

You can read the current value of the counter by reading the counter selected by A_1, A_0 as shown in table 3. This involves reading the count latch; since the value of the down counter may change while the the count latch is read, this method may not provide an accurate reading. You must control the CLK or GATE input to stop the counter and read it for a correct reading.

Using the Count Latch Command

When the count latch command is executed, the current counter value is latched into the counter latch. This value is held by the latch until it is read or until a new mode is set. This provides an accurate reading of the counter value when the command is executed without affecting counter operation. Figure 4 shows the format for the count latch command.

If the counter value that was latched into the count latch is not read before a second count latch command is executed, the second command is ignored. This is because the counter value latched by the first command is held until it is read or until a new mode is set. When the data in the count latch is read, the latch is released and continues tracking the value of the down counter.

Using the Multiple Latch Command

When the multiple latch command is received, the counter value and status register for any counter may be selectively latched into the count latch and status latch. Bits D_1-D_5 of the multiple latch command specify the counter latching. The CPU can then read the status and counter value for the selected counter. Figure 5 shows the format for this command.

Bits CNT2, CNT1, and CNT0 correspond to counters 2, 1, and 0. The command is executed for all counters whose corresponding bit is 1. This allows the data for more than one counter to be latched by a single count latch command.

When the count bit is 0, the counter value of the selected counters is latched into the count latches.

When the status bit is 0, the status of the selected counters is latched into the status latches. Bits D_5-D_0 of the status register show the mode status of the counter. The output bit (D_7) shows the state of the OUT pin of that counter. These bits are shown in figure 6. The null count bit (D_6) indicates whether the count data is valid. When the count is transferred from the count register to the down counter, this bit changes to 0 to show that the data is valid. Table 4 shows how the null count flag operates.

Table 4. Null Count Flag Operation

Operation	Null Count Flag
Write control word for mode set	1
Write count to count register(1)	1
Transfer count from count register to down counter	0

Note:

(1) When 2-byte mode is selected, the flag becomes 1 when the second byte is written.

Figure 4. Control Register Format for Count Latch Command

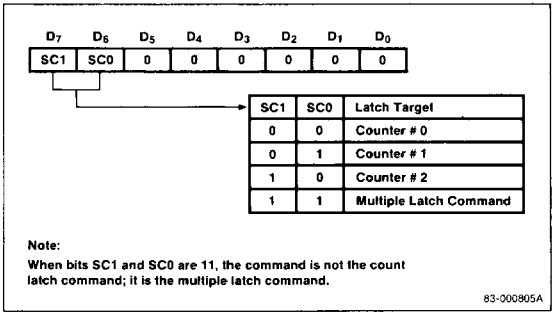
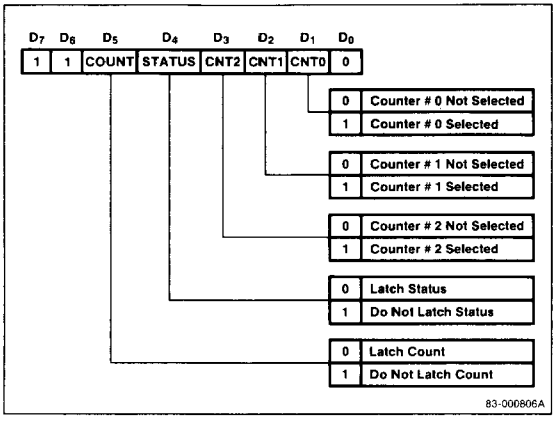


Figure 5. Control Register Format for Multiple Latch Command



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If the data that was latched is not read before a second multiple latch command is executed, the second command is ignored for those latches whose contents have not been read. This is because the data latched by the first command is held until it is read or until a new mode is set. When the data in the latch is read, the latch is released. See figure 7.

It is possible to latch both the count and status using two multiple latch commands. However, regardless of which data is latched first, the status is always read first. The count data is read by the next read operation (1- or 2-step read as determined by read/write mode). If additional read commands are received, the count data that has not been latched (the contents of the down counter as reflected by the current counter value) is read.

Read operations must be performed in accordance with read/write mode. In 2-byte mode, two bytes of data must always be read. This does not imply that the second byte must be read immediately after the first; other counter operations may be performed between the two reads. For example, you could read the lower byte, write a new lower byte, read the higher byte, and write a new higher byte.

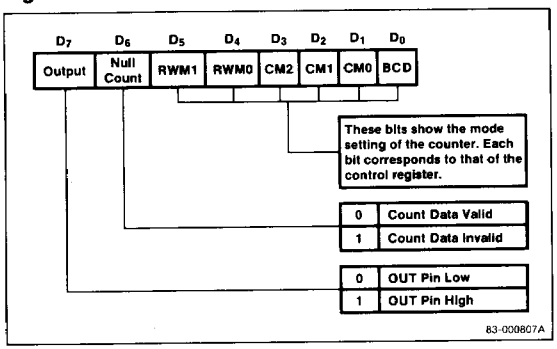
Definitions

CLK pulse refers to the time from the rising to the falling edge of the CLKn input.

Trigger refers to the rising edge of the GATEn input.

The GATEn input is sampled at each rising edge of the CLKn input. The GATE input can be level or rising edge sensitive. In the latter case, counter n's internal flip-flop is set at the rising edge of the GATE signal, sensed at the rising edge of the next CLK pulse, and reset immediately. This allows edge-triggering to be sensed whenever it occurs.

Figure 6. Status Data



Initial OUT refers to the state of the OUT pin immediately after the mode is set.

Gount transfer refers to the transfer from the count register to the down counter. The down counter is decremented at the falling edge of the CLK pulse.

Count zero is the state of the down counter when the counter is decremented to zero.

PCNT0, PCNT1, and PCNT2 are the I/O ports for counters 0, 1, and 2, respectively. PCTRL is the I/O port for the control command.

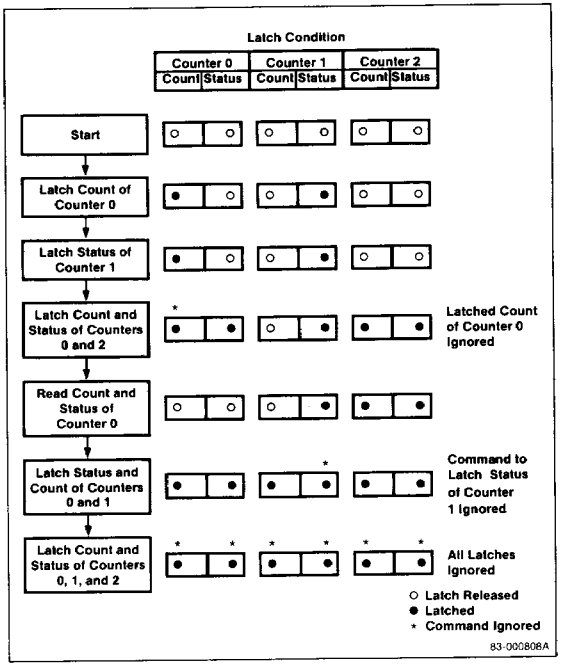
CW is the control command.

HB is the higher byte of the count.

LB is the lower byte of the count.

In the timing charts for each counter mode, counter 0 is in the read/write 1-byte and binary count mode. When no GATE signal appears in the charts, assume a high level signal. The value shown below the OUT signal is the counter value. The maximum value that can be set for the count in each mode is 0. When this value is set, a maximum value of 10000H (hexadecimal count) or 10000 (BCD count) is obtained.

Figure 7. Multiple Latch Command Execution Example



Counter Modes

Mode 0: Interrupt on End of Count. In this mode, the OUT output changes from low to high level when the end of the specified count is reached. See table 5 and figure 8.

Table 5. Mode 0 Operation

Function	Result
Initial OUT	Low level
GATE High	Count enable
GATE Low	Count disable
Count Write	The OUT pin goes low independent of the CLK pulse. In 2-byte mode, the count is disabled when the first byte is written. The OUT pin goes low. OUT goes low when a new mode or new count is written.
Count Transfer and Operation	When the count is written with GATE high: Transfer is performed at the first CLK pulse after the count value is written. The down counter is decremented beginning at the first CLK pulse after data transfer. If a count of n is set, the OUT pin goes high after n + 1 CLK pulses. When the count is written with GATE low: Transfer is performed at the first CLK pulse after the count is written. The down counter is decremented beginning at the first CLK pulse after the GATE signal goes high. If a count of n is set, OUT is low for a period of n CLK pulses after GATE goes high.
Count Zero	The signal at the OUT pin goes high. The count operation does not stop and counts down to FFFFH (hexadecimal) or 9999 (BCD) and continues to count down.
Minimum Count	1

Mode 0 Program Example. This subroutine causes a delay of 10004 (decimal, or 2710H) CLK pulses. In this program, counter 2 is set to 2-byte mode and binary count. See figure 9.

```
SUBR0:  MOV   AL,10110000B   ;set mode: counter 2,
                             ;2-byte mode,
        OUT   PCTRL,AL       ;count mode 0, binary
        MOV   AL,10H
        OUT   PCNT2,AL
        MOV   AL,27H         ;write count 10000 (decimal)
        OUT   PCNT2,AL
        RET
```

Mode 1: GATE Retriggerable One-Shot. In mode 1, the μPD71054 functions as a retriggerable one-shot. A low-level pulse triggered by the GATE input is output from the OUT pin. See table 6 and figure 10.

Table 6. Mode 1 Operation

Function	Result
Initial OUT	High level
GATE Trigger(1)	Count data is transferred at the CLK pulse after the trigger.
Count Write	The count is written without affecting the current operation.
Count Transfer and Operation	Transfer is performed at the first CLK pulse after the trigger. At the same time, the signal at the OUT pin goes low to start the one-shot pulse operation. The count is decremented beginning at the next CLK pulse. If a count of n is set, the one-shot output from the OUT pin continues for n CLK pulses.
Count Zero	The signal at the OUT pin becomes high. Count operation does not stop and wraps to FFFFH (hexadecimal) or 9999 (BCD) and continues to count.
Minimum Count	1

Note:

(1) The trigger is ignored when the count has not been written after the mode is set, or when only one byte of the count has been written in 2-byte count mode.

5d

Figure 8. Mode 0 Timing Chart

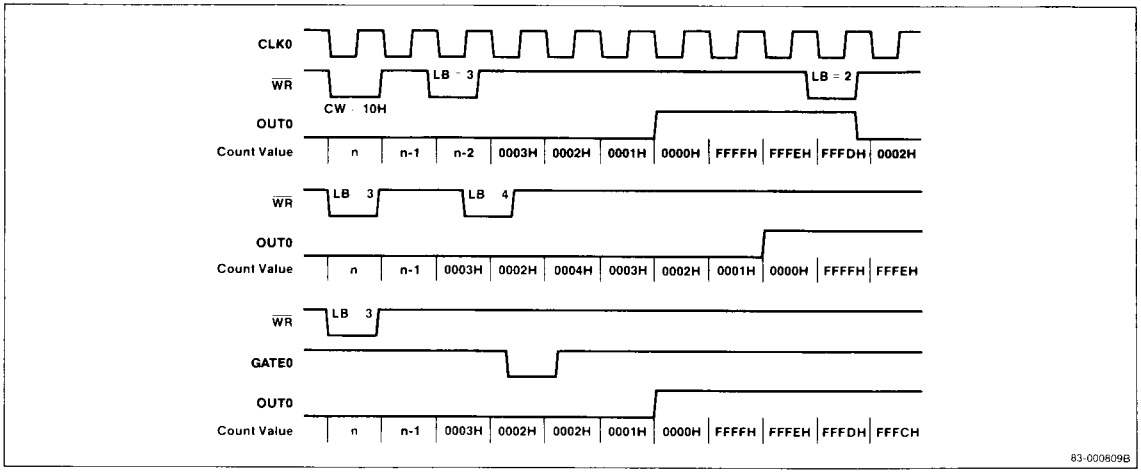


Figure 9. Mode 0 Program Example Timing Chart

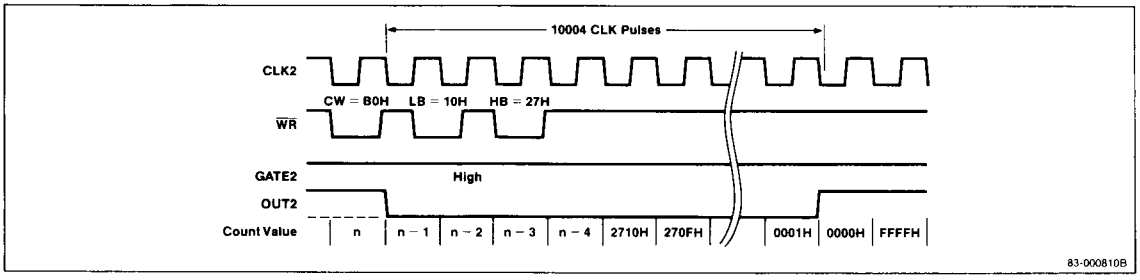
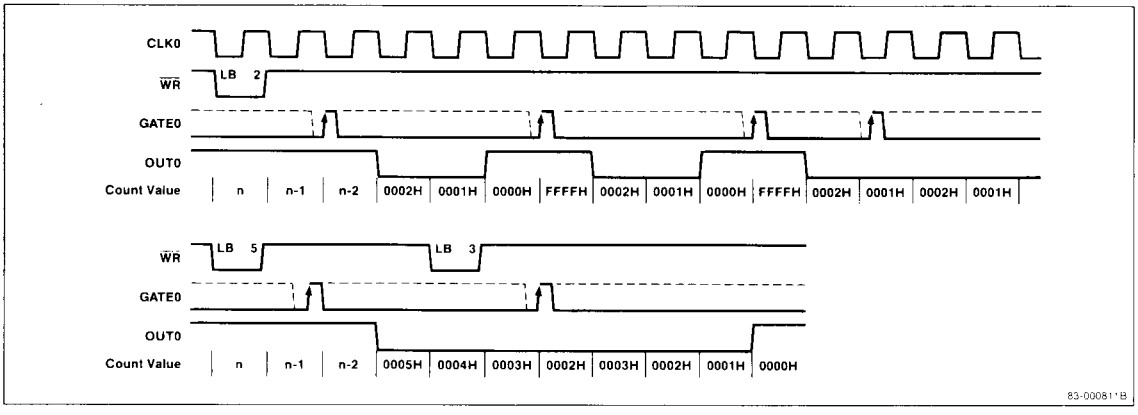


Figure 10. Mode 1 Timing Chart



Mode 1 Program Example. This subroutine waits until no trigger is generated for an interval of 200 or more CLK pulses after the first gate trigger and returns to the main program. Counter 1 is set to low-byte read/write mode and binary count. See figure 11.

```
SUBR1:  MOV   AL,01010010B  ;set mode: counter 1, low-byte
        OUT   PCTRL,AL      ;read/write mode, count mode 1,
        MOV   AL,200        ;binary
        OUT   PCNT1,AL      ;write low byte of count
        ;
FSTTRG: MOV   AL,11100100B  ;multiple latch command:
                            ;counter 1,
        OUT   PCNT1,AL      ;status
        IN    AL,PCNT1
        TEST1 AL,7          ;wait for first trigger
        BNZ   FSTTRG
        ;
WAIT:   MOV   AL,11100100B  ;multiple latch command:
                            ;counter 1,
        OUT   PCTRL,AL      ;status
        IN    AL,PCNT1
        TEST1 AL,7          ;wait until output goes high
        BZ    WAIT
        RET
```

Mode 2: Rate Generator. In mode 2, the signal from the OUT pin cyclically goes low for one clock period when the counter reaches 0001H. The counter operates as a frequency divider. See table 7 and figure 12.

Table 7. Mode 2 Operation

Function	Result
Initial OUT	High level
GATE High	Count enable
GATE Low	Count disabled. If GATE goes low when OUT is low, OUT will go high (independent of the CLK pulse).
GATE Trigger(1)	Transfer is performed at the first CLK pulse after the trigger.
Count Write	Count is written without affecting the current operation.
Count Transfer and Operation	Transfer is performed at the CLK pulse after the count is written following the mode setting. The counter is then decremented. Transfer is again performed at the first CLK pulse after the count becomes 1. When the trigger is used, transfer is performed at the next CLK pulse. When the contents of the down counter becomes 1, OUT goes low for one CLK pulse and returns to high. If a count of n is set, OUT repeats this sequence every n CLK pulses.
Count Zero	Never occurs in this mode.
Minimum Count	2

Note:

(1) The trigger is ignored when the count has not been written or when only one byte of the count has been written in 2-byte mode.

Figure 11. Mode 1 Program Example Timing Chart

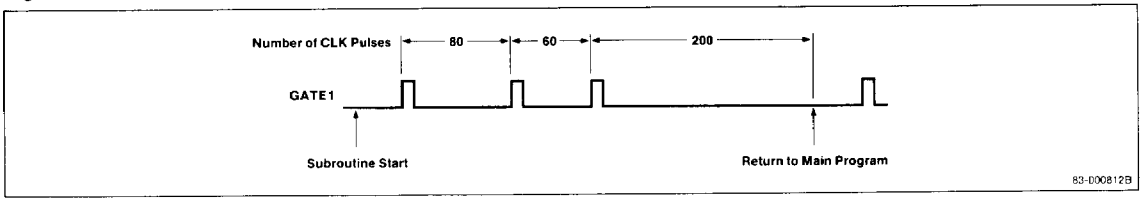
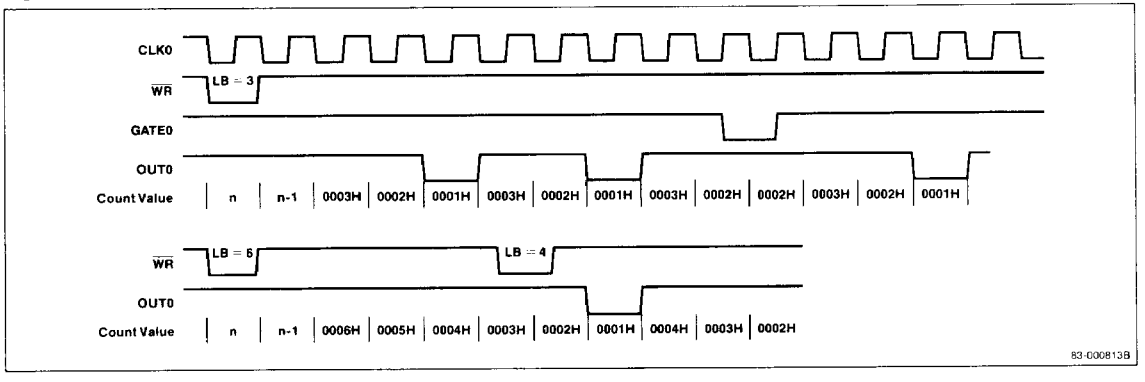


Figure 12. Mode 2 Operation Timing Chart



5d

Mode 2 Program Example. This subroutine generates an interrupt to the CPU each time 10000 (decimal) clock pulses elapse. Counter 0 is in 2-byte mode and binary counting. See figure 13.

```
SUBR3:  MOV  AL,00110100B    ;mode setting: counter 0, 2-byte
        OUT  PCTRL,AL        ;mode, count mode 2, binary
        MOV  AL,10H
        OUT  PCNT0,AL
        MOV  AL,27H          ;write count 10000 (decimal)
        OUT  PCNT0,AL
        RET
```

Mode 3: Square Wave Generator. Mode 3 is a frequency divider similar to mode 2, but with a different duty cycle. See table 8 and figure 14.

Figure 13. Mode 2 Configuration

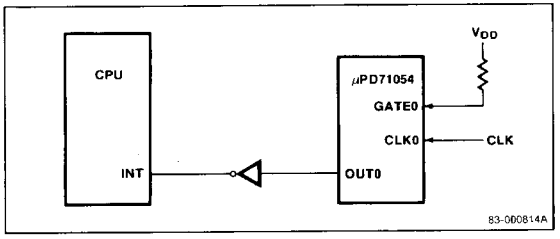


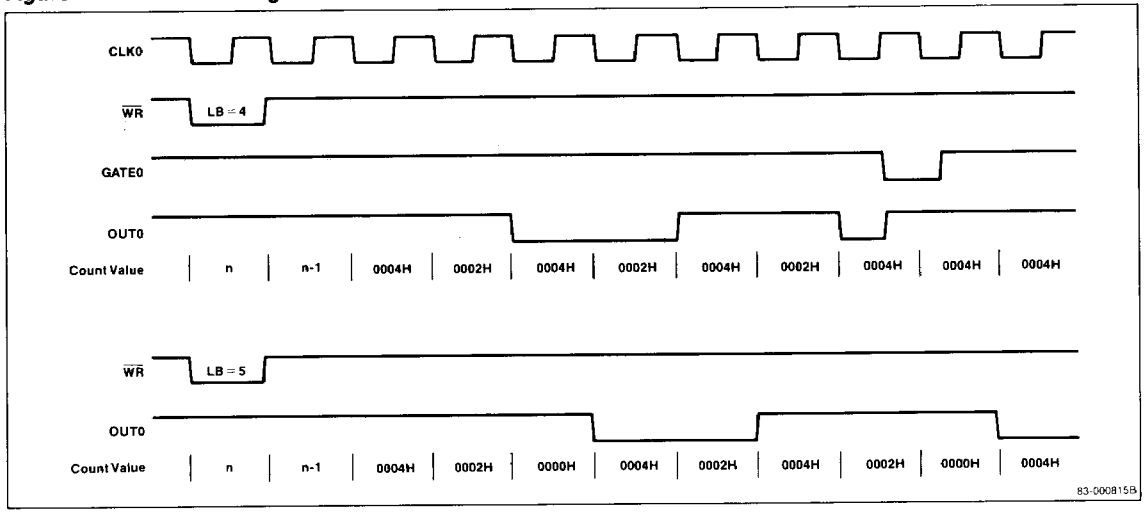
Table 8. Mode 3 Operation

Function	Result
Initial OUT	High level
GATE High	Count enable
GATE Low	Count disable. If GATE goes low when OUT is low, OUT will go high (independent of the CLK pulse).
GATE Trigger(1)	Transfer is performed at the first CLK pulse after the trigger.
Count Write	Current operation is not affected. The count is transferred at the end of the half-period of the current square wave and the OUT pin goes high.
Count Transfer and Operation	Count data is transferred at the first CLK pulse after the count write following the mode setting. Transfer is performed at the end of the current half-cycle and the OUT pin is inverted. Transfer is also performed at the CLK pulse after the trigger. The operation performed depends on whether count n is even or odd. When n is even, the count is decremented by two on each following clock pulse. At the end of the count of two, the count is again transferred and the OUT pin is inverted. This is taken as a half-cycle and repeated. When n is odd, n − 1 is transferred and the count is decremented by two on each following clock pulse. The half-cycle when the OUT pin is high continues until the end of count 0 and n − 1 is transferred again at the next CLK pulse. The half-cycle while OUT is low continues until the end of count 2. Thus, the half-cycle while OUT is high is one CLK longer than the half-cycle while OUT is low.
Count Zero	Occurs only when the count is odd.
Minimum Count	3

Note:

(1) The trigger is ignored when the count has not been written after the mode is set or when only one byte of count has been written in 2-byte mode.

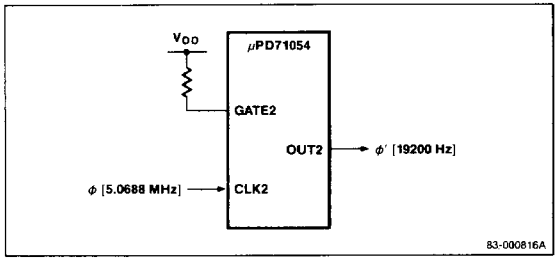
Figure 14. Mode 3 Timing Chart



Mode 3 Program Example. This subroutine divides the input CLK frequency (5.0688 MHz) by 264 to get a 19,200 Hz clock. Counter 2 is in 2-byte binary mode. See figure 15.

```
SUBR4:  MOV   AL,10110110B  ;mode setting: counter 2, 2-byte
        OUT   PCTRL,AL      ;mode, count mode 3, binary
        MOV   AL,08H
        OUT   PCNT2,AL
        MOV   A,01H         ;264 frequency division
        OUT   PCNT2,AL
        RET
```

Figure 15. Frequency Division

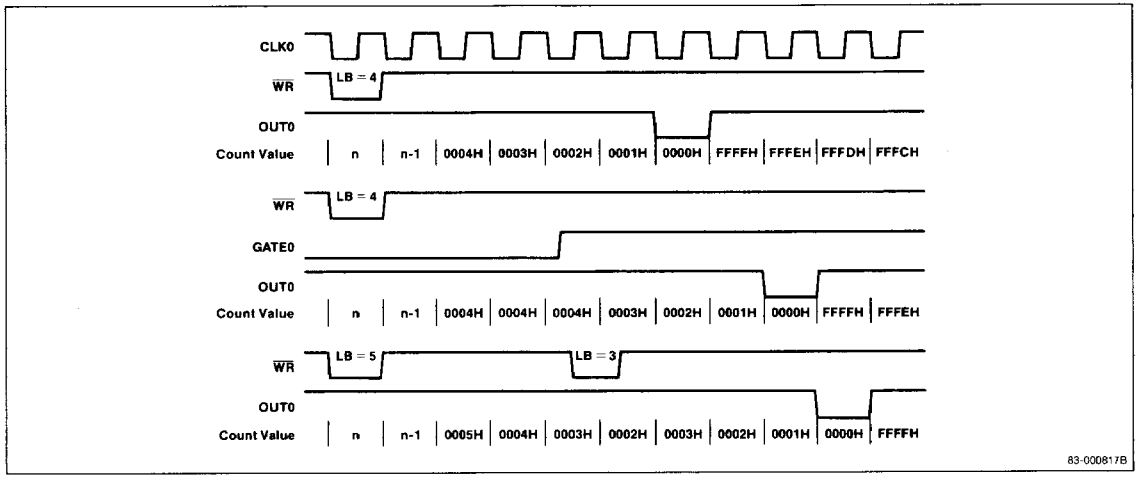


Mode 4: Software-Triggered Strobe. In mode 4, when the specified count is reached, OUT goes low for one CLK pulse. See table 9 and figure 16.

Table 9. Mode 4 Operation

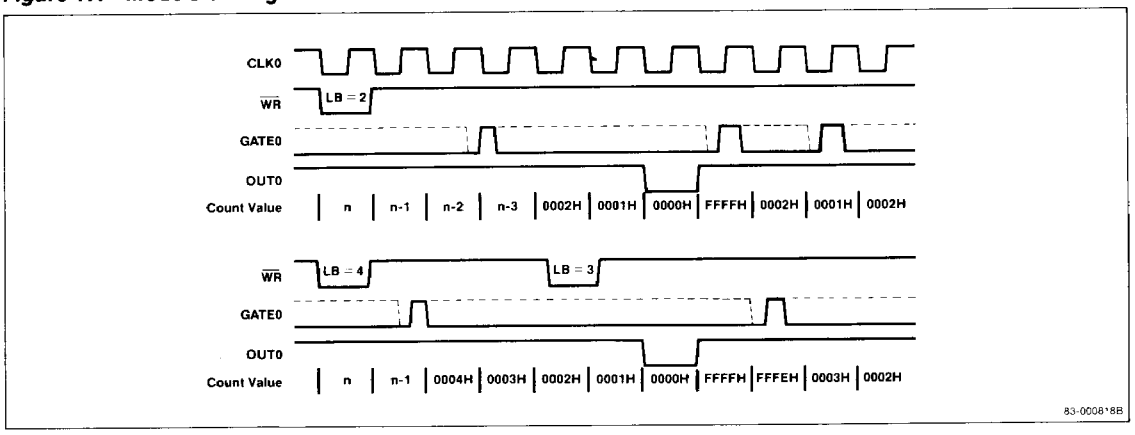
Function	Result
Initial OUT	High level
GATE High	Count enable
GATE Low	Count disable
Count Write	Count is transferred at the next CLK pulse when the count is written. In 2-byte mode, data is transferred after the second byte is written.
Count Transfer and Operation	Count is transferred at the first CLK following the count write. If GATE is high, the down counter begins to decrement from the next CLK. If GATE is low, decrement begins at the first CLK after GATE goes high.
Count Zero	OUT is low for one CLK pulse and returns to high. The down counter wraps to FFFFH (hexadecimal) or 9999 (BCD) without stopping counter operation.
Minimum Count	1

Figure 16. Mode 4 Timing Chart



5d

Figure 17. Mode 5 Timing Chart



Mode 5: Hardware-Triggered Strobe [Retriggerable]. Mode 5 is similar to mode 4 except that operation is triggered by the GATE input and can be retriggered. See table 10 and figure 17.

Table 10. Mode 5 Operation

Function	Result
Initial OUT	High level
GATE Trigger(1)	The count is transferred at the CLK pulse after the trigger. The GATE has no effect on the OUT signal.
Count Write	The count is written without affecting the current operation.
Count Transfer and Operation	Count is transferred at the first CLK pulse after a trigger, providing that the mode and count have been written. Decrement begins from the first CLK pulse after a data transfer. If a count of n is set, OUT goes low for n + 1 CLK pulses after the trigger.
Count Zero	OUT is low for one CLK and goes high again. The down counter counts to FFFFH (hexadecimal) or 9999 (BCD) without stopping the counter operation.
Minimum Count	1

Note:

(1) The trigger is ignored when the count has not been written after the mode is set or when only one byte has been written in 2-byte mode.

Mode 5 Program Example. Use mode 5 to add a fail-safe function to an interface. For example, the receiving equipment requests data by issuing a $\overline{REQ}$ signal to the sending equipment. The sending equipment responds by outputting data to the data bus and returning a $\overline{SEND}$ signal to the receiving equipment. In this type of system, if a malfunction exists in the sending equipment and no $\overline{SEND}$ signal is sent, the receiving equipment waits indefinitely for the $\overline{SEND}$ signal and system operation stops. The following subroutine remedies this situation. If no $\overline{SEND}$ signal is output within a given period (50 CLK cycles in this example) after the $\overline{REQ}$ signal is output, the system assumes the sending equipment is malfunctioning and a $\overline{FAIL}$ signal is sent to the receiving equipment.

```
SUBR5:  MOV   AL,00011010B   ;mode setting: counter 0, low
                             ;1-byte
        OUT   PCTRL,AL       ;mode, count mode 5, binary
        MOV   AL,50          ;set interval: 50 CLK pulses
        OUT   PCNT0,AL
        RET
```

Figure 18. Interface Fail-safe Example