

# Power management (dual transistors)

## EMF32 / UMF32N

DTA143T and 2SK3019 are housed independently in a EMT6 package.

### ●Application

Power management circuit

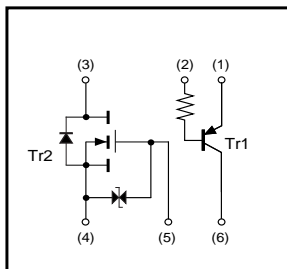
### ●Features

- 1) Power switching circuit in a single package.
- 2) Mounting cost and area can be cut in half.

### ●Structure

Silicon epitaxial planar transistor

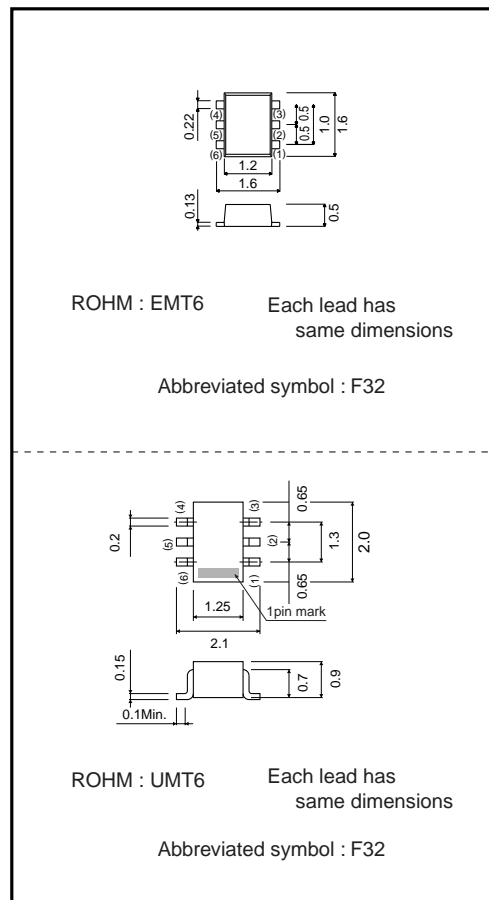
### ●Equivalent circuits



### ●Packaging specifications

Type	EMF32	UMF32
Package	EMT6	UMT6
Marking	F32	F32
Code	T2R	TR
Basic ordering unit (pieces)	8000	3000

### ●External dimensions (Unit : mm)



## Transistors

## ●Absolute maximum ratings (Ta=25°C)

Tr1

Parameter	Symbol	Limits	Unit
Collector-base voltage	V <sub>CB0</sub>	-50	V
Collector-emitter voltage	V <sub>CEO</sub>	-50	V
Emitter-base voltage	V <sub>EBO</sub>	-5	V
Collector current	I <sub>c</sub>	-100	mA
Power dissipation	P <sub>c</sub>	150(TOTAL)	mW *1
Junction temperature	T <sub>j</sub>	150	°C
Range of storage temperature	T <sub>stg</sub>	-55 to +150	°C

\*1 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

Parameter	Symbol	Limits	Unit
Drain-source voltage	V <sub>DSS</sub>	30	V
Gate-source voltage	V <sub>GSS</sub>	±20	V
Drain current	Continuous	I <sub>D</sub>	100 mA
	Pulsed	I <sub>DP</sub>	200 mA *1
Reverse drain current	Continuous	I <sub>DR</sub>	100 mA
	Pulsed	I <sub>DRP</sub>	200 mA *1
Total power dissipation	P <sub>D</sub>	150(TOTAL)	mW *2
Channel temperature	T <sub>ch</sub>	150	°C
Range of storage temperature	T <sub>stg</sub>	-55 to +150	°C

\*1 PW≤10ms Duty cycle≤50%

\*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

## ●Electrical characteristics (Ta=25°C)

Tr1

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV <sub>CB0</sub>	-50	-	-	V	I <sub>c</sub> =-50μA
Collector-emitter breakdown voltage	BV <sub>CEO</sub>	-50	-	-	V	I <sub>c</sub> =-1mA
Emitter-base breakdown voltage	BV <sub>EBO</sub>	-5	-	-	V	I <sub>E</sub> =-50μA
Collector cutoff current	I <sub>CB0</sub>	-	-	-0.5	μA	V <sub>CB</sub> =-50V
Emitter cutoff current	I <sub>EBO</sub>	-	-	-0.5	μA	V <sub>EB</sub> =-4V
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	-	-	-0.3	V	I <sub>c</sub> /I <sub>B</sub> =-5mA/-0.25mA
DC current transfer ratio	h <sub>FE</sub>	100	250	600	-	I <sub>c</sub> =-1mA, V <sub>CE</sub> =-5V
Input resistance	R <sub>1</sub>	3.29	4.7	6.11	kΩ	-
Transition frequency	f <sub>T</sub>	-	250	-	MHz	V <sub>CE</sub> =-10V, I <sub>E</sub> =5mA, f=100MHz *

\* Transition frequency of the device

Tr2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	-	-	±1	μA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	30	-	-	V	I <sub>D</sub> =10μA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	-	-	1.0	μA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V
Gate-threshold voltage	V <sub>GS(th)</sub>	0.8	-	1.5	V	V <sub>DS</sub> =3V, I <sub>D</sub> =100μA
Static drain-source on-state resistance	R <sub>DS(on)</sub>	-	5	8	Ω	I <sub>D</sub> =10mA, V <sub>GS</sub> =4V
		-	7	13	Ω	I <sub>D</sub> =1mA, V <sub>GS</sub> =2.5V
Forward transfer admittance	Y <sub>fs</sub>	20	-	-	ms	V <sub>DS</sub> =3V, I <sub>D</sub> =10mA
Input capacitance	C <sub>iss</sub>	-	13	-	pF	V <sub>DS</sub> =5V, V <sub>GS</sub> =0V, f=1MHz
Output capacitance	C <sub>oss</sub>	-	9	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>	-	4	-	pF	
Turn-on delay time	t <sub>d(on)</sub>	-	15	-	ns	
Rise time	t <sub>r</sub>	-	35	-	ns	I <sub>D</sub> =10mA, V <sub>DD</sub> ≐5V, V <sub>GS</sub> =5V, R <sub>L</sub> =500Ω, R <sub>GS</sub> =10Ω
Turn-off delay time	t <sub>d(off)</sub>	-	80	-	ns	
Fall time	t <sub>f</sub>	-	80	-	ns	

Transistors

●Electrical characteristic curves

Tr1

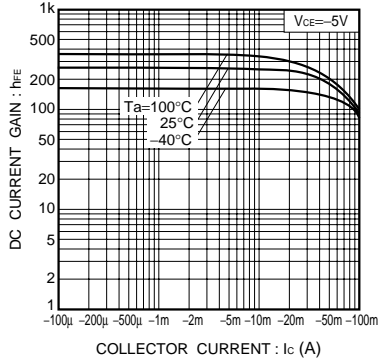


Fig.1 DC current gain vs. collector current

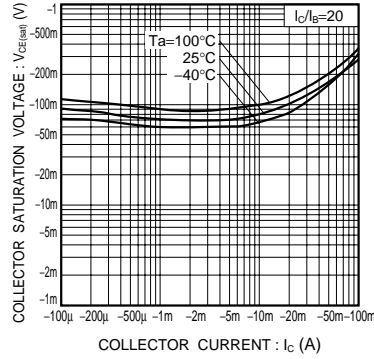


Fig.2 Collector-emitter saturation voltage vs. collector current

Tr2

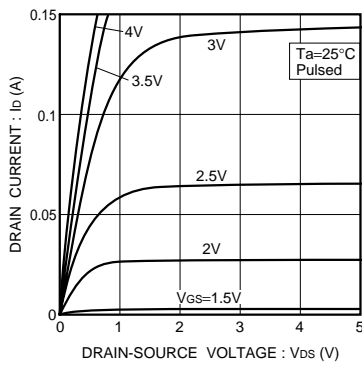


Fig.3 Typical output characteristics

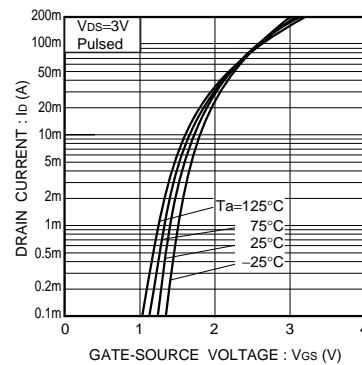


Fig.4 Typical transfer characteristics

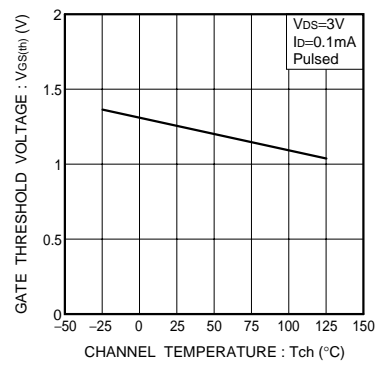


Fig.5 Gate threshold voltage vs. channel temperature

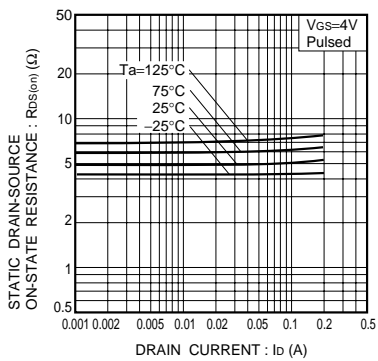


Fig.6 Static drain-source on-state resistance vs. drain current ( I )

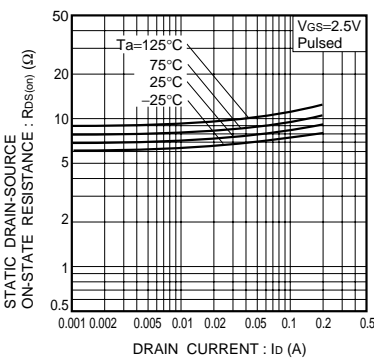


Fig.7 Static drain-source on-state resistance vs. drain current ( II )

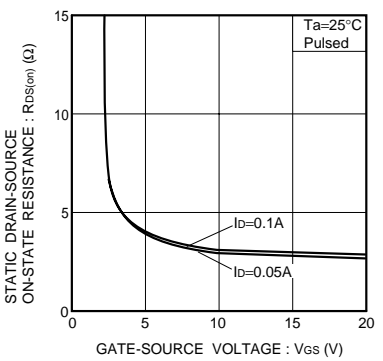


Fig.8 Static drain-source on-state resistance vs. gate-source voltage

Transistors

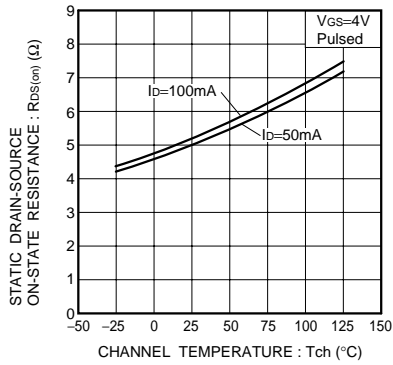


Fig.9 Static drain-source on-state resistance vs. channel temperature

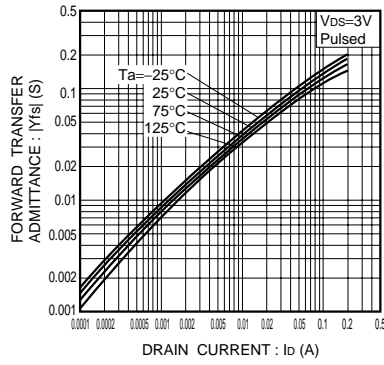


Fig.10 Forward transfer admittance vs. drain current

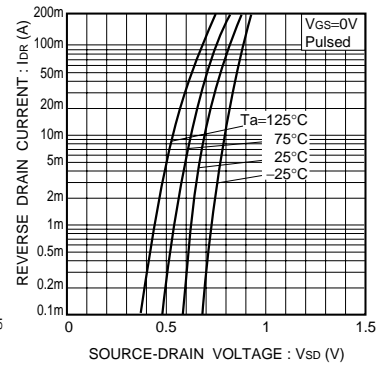


Fig.11 Reverse drain current vs. source-drain voltage ( I )

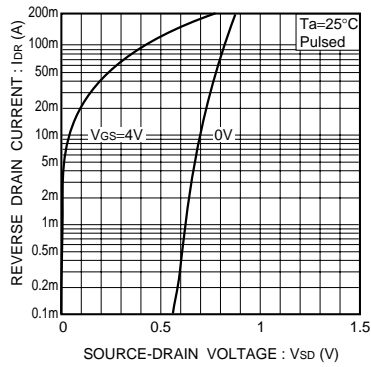


Fig.12 Reverse drain current vs. source-drain voltage ( II )

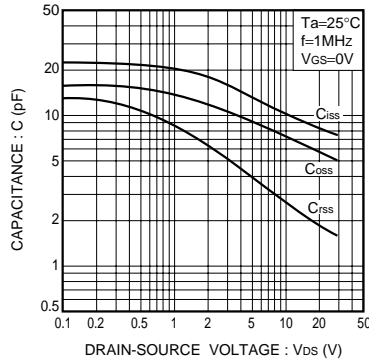


Fig.13 Typical capacitance vs. drain-source voltage

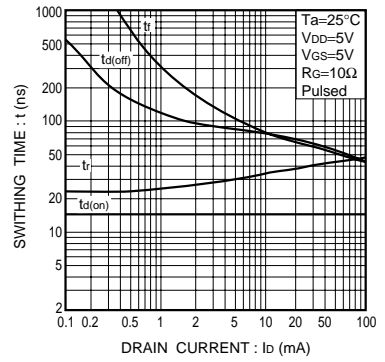


Fig.14 Switching characteristics

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