100-MHz Quadrature Demodulator

Description

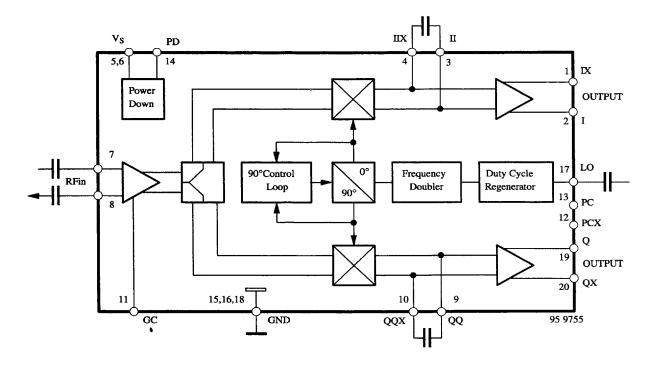
U2791B silicon monolithic integrated circuit is a quadrature demodulator that is manufactured using TELEFUNKEN's advanced UHF technology. This demodulator features a frequency range from $100-1000 \, \text{MHz}$, low current consumption, selectable

gain, power down mode and is adjustment free. The IC is suitable for direct conversion and image rejection applications in digital radio systems up to 1 GHz such as cellular radio, cordless telephone, cable TV and satellite TV systems.

Features

- Supply voltage 5 V (typ.)
- Very low power consumption 125 mW (typ.)
- Very good image rejection by means of phase control loop for precise 90° phase shifting
- Duty cycle regeneration for single ended LO input signal
- Low LO input level –10 dBm (typ.)
- LO frequency from 100 MHz to 1 GHz
- Power down mode
- 25 dB gain control

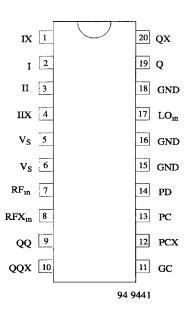
Block Diagram



Rev. A2: 04.05.1995

8 8920096 0012467 193

Pin Description



Pin	Symbol	Function
1	IX	IX output
2	I	I output
3	II	II low pass filter I
4	IIX	IIX low pass filter I
5	Vs	Supply voltage
6	Vs	Supply voltage
7	RF _{in}	RF input
8	RFX _{in}	RFX input
9	QQ	QQ low pass filter Q
10	QQX	QQX low pass filter Q
11	GC	GC gain control
12	PCX	PCX phase control
13	PC	PC phase control
14	PD	PD power down
15	GND	Ground
16	GND	Ground
17	LO _{in}	LO input
18	GND	Ground
19	Q	Q output
20	QX	QX output

Absolute Maximum Ratings

	Parameters	Symbol	Value	Unit
Supply voltage	Pins 5 and 6	V _S	6	37
Input voltage	Pins 7, 8 and 17	Vi	0 to V _S	v
Junction temperature Storage temperature range		T _i	125	90
		T _{sto}	-40 to 125	~ ℃

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage range Pins 5 and 6	Vs	4.75 to 5.25	v
Ambient temperature range	T _{amb}	-40 to 85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO-20	R _{thJA}	140	K/W

■ 892009b 00%8458 027 **■**

Rev. A2: 04.05.1995

TELEFUNKEN Semiconductors

Electrical Characteristics

Test conditions (unless otherwise specified); $V_S=5~V$, $T_{amb}=25^{\circ}C$, referred to test circuit System impedance $Z_O=50~\Omega$, fiLO = 950 MHz, PiLO = -10 dBm

Parameters	Test Conditions / Pins	Symbol	Min.	Тур.	Max.	Unit
Supply voltage range	Pins 5 and 6	Vs	4.75		5.25	v
Supply current	Pins 5 and 6	I _S		32		mA
Power Down Mode, PD						
"OFF"mode supply current	$V_{PD} \le 0.5 \text{ V}$ Pins 5, 6 $V_{PD} = 1.0 \text{ V}$ Pin 14 Note 1	IsPD		≤ 1 20		μА
Switch Voltage (Pin 14)						
"Power ON"		VPON	4			
"Power DOWN"		VPOFF			1	V
LO Input, LO _{in} (Pin 17)						
Frequency range		fiLO	100		1000	MHz
Input level	Note 2	PiLO	-12	-10	-5	dBm
Input impedance	See figure 5	ZiLO		50		Ω
Voltage standing wave ratio	See figure 2	VSWRLO		1.2	2	
Duty cycle range		LODCR	0.4		0.6	
RF Input, RF _{in}						•
Noise figure (DSB) symmetrical output	@ 950 MHz Note 3 @ 100 MHz Pins 7 and 8	NF		12 10		dB
Frequency range	Pins 7 and 8	fiRF	100		1000	MHz
-1 dB input compression point	Pins 7 and 8 High gain Low gain	ICPHG ICPLG		-8 +3.5		
2nd order IIP	Pins 7 and 8	IIP2HG		35		1
Input 3rd order IIP	Pins 7 and 8 High gain Low gain	IIP3HG IIP3LG		+3 +13		dBm
LO leakage	Pins 7 and 8 Symmetric input Asymmetric input	LOL		≤ -60 ≤ -55		
Input impedance	See figure 6 Pins 7 and 8	ZiRF		500Ω 0.8pF		
I/O Outputs	Emitter follower I = 0.6 mA	I, IX / Q, QX				
3 dB-bandwidth w/o external C	Note 4 Pins 1, 2, 19, 20	BWI/Q	≥ 30			MHz
I/Q amplitude imbalance	Pins 1, 2, 19, 20	AII/Q		≤±0.2		dB
I/Q quadrature error	Pins 1, 2, 19, 20	QEI/Q		≤±1.5		Deg
I/Q maximum output swing	Pin 1, 2, 19, 20 Symm. output $R_L > 5 k\Omega$	Max I/Q			2	V _{PP}
DC output voltage	Pins 1, 2, 19, 20	VOUT		2.8	1	V
DC output offset voltage	Note 5 Pins 1, 2, 19 and 20	VOFSI/Q I/IX Q/QX		≤ 30		mV
Output impedance	Pins 1, 2, 19 and 20	Zout		50		Ω

Rev. A2: 04.05.1995

Electrical Characteristics (Cont'd)

Parameters	Test Conditions / Pins	Symbol	Min.	Тур.	Max.	Unit	
Gain Control, GC							
Control range power gain gain high/gain low	Pin 11	GCR PGH/GGL		25 23/–2		dB	
Switch voltage							
"Gain high"	Pin 11	GCVHigh			1		
"Gain low"	Note 6 Pin 11	GCVLow				V	
Settling Time, ST					·	1	
Power "OFF" ~ "ON"		STON		< 4		μѕ	
Power "ON" - "OFF"		STOFF		< 4			

Notes

- During power down status a load circuitry with dc-isolation to GND is assumed otherwise a current of I ≈ (V_S −0.8 V) /RI has to be added to the above power down current for each output I, IX, Q, QX.
- 2. The required LO-Level is a function of the LO-frequency (see figure 4).
- Measured with input matching. For 950 MHz the optional transmission line T3 at the RF input may be used for this purpose. Noise figure
 measurements without using the differential output signal result in a worse noise figure.
- 4. Due to test board parasitics this bandwidth is reduced and not equal for I, IX, Q, QX. If symmetry and full bandwidth is required the low-pass pins 3, 4, 9 and 10 should be isolated from the board. The bandwidth of the I/Q outputs can be increased further by using a resistor between the pins 3, 4, 9 and 10. This resistors shunt the internal loads of RI \sim 5.4 k Ω The decrease in gain here has to be considered.
- Output emitter follower internal acurrent I = 0.6 mA allows only small voltage swing with a 50 Ω load. For low signal distortion the load
 impedance should be RI ≥ 5 kΩ
- 6. The low gain status is achieved with an open or high ohmic pin 11. A recommended application circuit is shown in figure 1.

Test Circuit

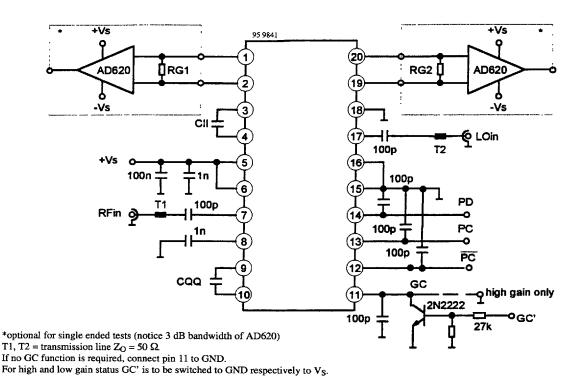
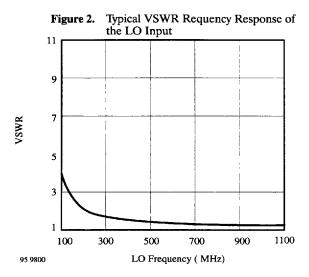


Figure 1.



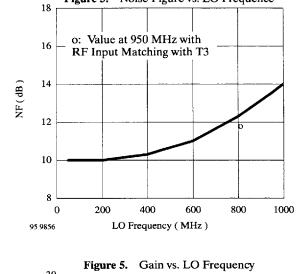
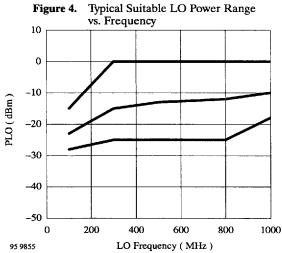
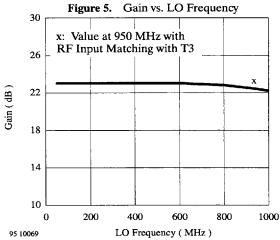
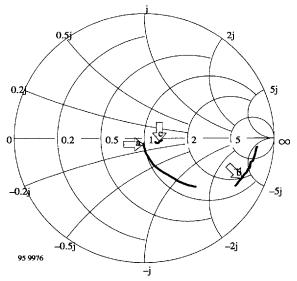


Figure 3. Noise Figure vs. LO Frequence

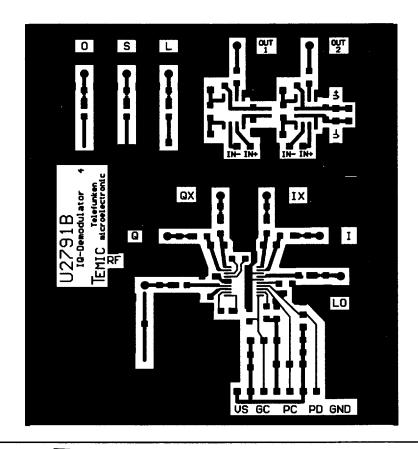






- Figure 6. Typical S11 frequency response of the
 a: LO input, LO frequency from 100 MHz to 1100 MHz, marker: 950 MHz b: RF input, RF frequency from 100 MHz to 1100 MHz, marker: 950 MHz
 - c: I/Q outputs, baseband frequency from 5 MHz to 55 MHz, marker: 25 MHz.

Board Layout

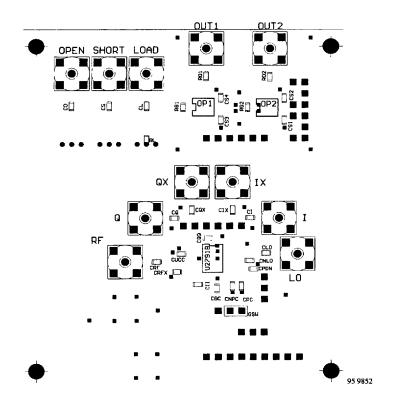


94 9698

8920096 0012472 550

Rev. A2: 04.05.1995

Board Layout



External Components

CUCC 100 nF **CRFX** 1 nF 100 pF CLO **CNLO** 0Ω **CRF** 100 pF CII, CQQ optional external lowpass filters **T**3 transmission line for RF-input matching to connect optionally CI, CIX, optional for ac-coupling at

CQ, CQX baseband outputs CPDN 100 pF

CGC 100 pF CPC 100 pF CNPC 100 pF GSW gain switch

Calibration Part

 $\begin{array}{cc} \text{CO, CS, CL} & 100 \text{ pF} \\ \text{RL} & 50 \text{ } \Omega \end{array}$

Conversion to Single Ended Output

OP1, OP2 AD620

RG1, RG2 prog. gain, see datasheet, for 5.6 k Ω a

gain of 1 to 50 Ω is achieved together

with RD1 and RD2

RD1, RD2 450 Ω CS1, CS2 100 nF CS3, CS4, 100 nF

Description of Evaluation Board

Board material:

epoxy; $\epsilon r = 4.8$, thickness = 0.5 mm transmission lines: $Z_O = 50 \Omega$

The Board Offers the Following Functions

- The test circuit for the U2791B:
 - The supply voltage and the control inputs GC, PC and PD are connected via a plug strip. The control input voltages can be generated via external potentiometers; then the inputs should be ac-grounded (time requirements in burst-mode for power up have to be considered).
 - The outputs I, IX, Q, QX are dc coupled via an plug strip or can be ac-connected via SMB plugs for high frequency tests e.g. noise figure or s-parameter measurement. The pins II, IIX, QQ, QQX allow user definable filtering with 2 external capacitors CII, CQQ.

- Also the offsets of both channels can be adjusted with two potis or resistors.
- The LO- and the RF-inputs are ac-coupled and connected via SMB plugs. If transmission line T3 is connected to the RF-input and ac-grounded at the other end, gain and noise performance can be improved (input matching to 50 Ω).
- The complementary RF-input is ac-coupled to Gnd (CRFX = 1 nF).
- A calibration part, which allows to calibrate an s-parameter analyzer direct to the in- and outputsignals ports of the U2791B.
- For single ended measurements at the demodulator outputs, two OP's (e.g., AD620 or other) can be configured with programmable gain; together with an output-divider network RD = 450 Ω to RL = 50 Ω , direct measurements with 50 Ω load-impedances are possible at frequencies < 100 kHz.

Dimensions in mm

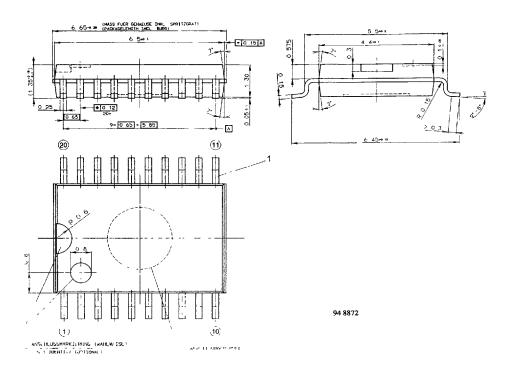


Figure 7. SSO-20 Package

We reserve the right to make changes to improve technical design without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany Telephone: 49 (0)7131 67 2831, Fax Number: 49 (0)7131 67 2423