TMPZ84C112AN-6 / AF-6 T-49-19-07

1. OUTLINE AND FEATURES

The TMPZ84C112A is a high-performance, low power consumption 8-bit microcomputer created with Toshiba CMOS silicon technology.

The TMPZ84C112A consists of a Toshiba CMOS TMPZ84C00A core with built-in input/output ports, timer and a 256-byte RAM. The TMPZ84C112A is available in a 64-pin shrink dual inline package or a 64-pin flat package and is extremely effective in promoting system miniaturization and low current consumption.

The CPU is fully Z80 compatible and can thus be used with existing software resources and development tools. It is possible to set only the built-in CPU to high impedance with the $\overline{\text{BUSREQ}}/\overline{\text{EV}}$ pin used for debugging to enable real time development by connecting a Z80 in-circuit emulator with the TMPZ84C112A mounted on the target PCB.

- The TLCS-Z80 CPU has built-in input/output ports (21 or 23 depending on the mode), a one-channel free-running timer and a 256-byte RAM.
- Wide operating frequency range : DC to 6.144MHz
- Wide operating voltage range : 4.5V to 5.5V
- Wide operating temperature range : −10 °C to +70 °C.
- Three (23 bit maximum) built-in input/output ports.
  Ports PA, PB : each nibble can be set for input or output.
  Port PC : each bit can be set for input or output.
- Built-in 256-byte RAM, two types of program mapping.
- Compact 64-pin shrink dual inline package (TMPZ84C112AN-6) or compact 64-pin flat package (TMPZ84C112AF-6).
- The Toshiba RTE80 real time emulator and commercially available Z80 ICE (In-Circuit Emulator) can be used.
- A Toshiba adaptor board (BM8029) can be used.

Note : Z80 is a trademark of Zilog Inc., U.S.A.

2. PIN ASSIGNMENT AND FUNCTIONS

2.1 Pin Assignment (Top View)

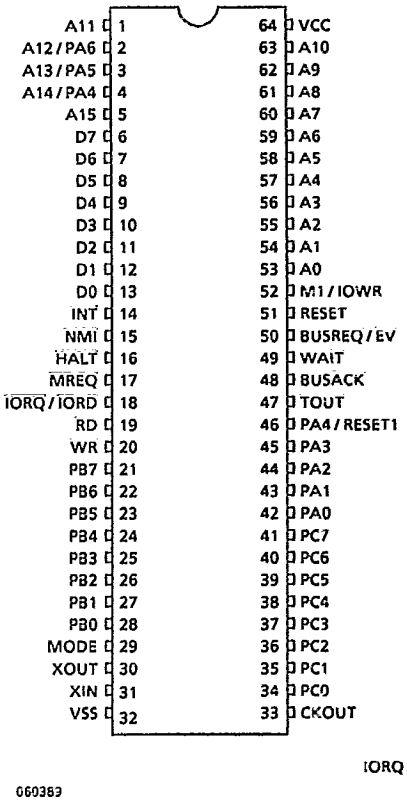

Figure 2.1 TMPZ84C112AN-6

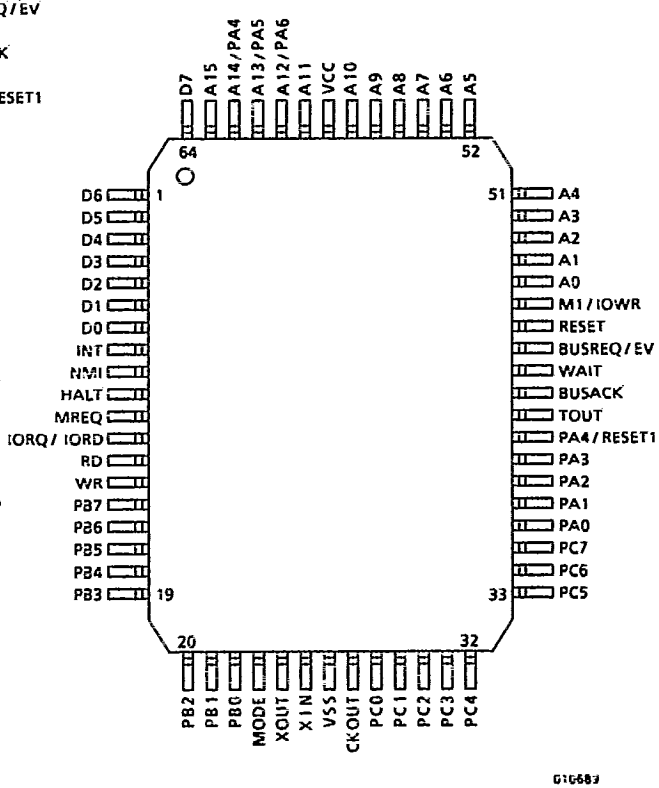

Figure 2.2 TMPZ84C112AF-6

2.2 Pin Names and Functions

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PIN	Q'ty (Number)	TYPE	FUNCTION	
			MODE PIN = "0" (MODE 0)	MODE PIN = "1" (MODE 1)
D0~D7	8	Input/Output 3-State	An 8-bit bi-directional data bus. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
A0~A11 A15	13	Output 3-State	A 13-address bus. Used to set addresses for memory and input/output ports. The refresh addresses are output to the lower 7 bits during refresh. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
A12 / PA6 A13 / PA5 A14 / PA4	3	Output 3-State/ Input/Output 3-State	Functions as bit 12 ~ bit 14 of the address bus. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	Functions as bit 4 ~ bit 6 of PA (port A).
$\overline{M1}$ / $\overline{IOWR}$	1	Output 3-State	This signal indicates machine cycle 1. "0" is output together with the $\overline{MREQ}$ signal during the op code fetch cycle. "0" is output together with the $\overline{IORQ}$ signal during the interrupt acknowledge cycle.	"0" is output when both the Z80 CPU $\overline{IORQ}$ and $\overline{WR}$ signals are "0". That is, "0" is output during output instruction execution.
			High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
$\overline{IORQ}$ / $\overline{IORD}$	1	Output 3-State	The input/output request signal. "0" is output during input/output operations. "0" is also output together with the $\overline{M1}$ signal during the interrupt acknowledge cycle.	"0" is output when both the Z80 CPU $\overline{IORQ}$ and $\overline{RD}$ signals are "0". That is, "0" is output during input instruction execution.
			High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
$\overline{RD}$	1	Ouput 3-State	The read signal. This signal reports when the CPU is reading data from memory or input/output. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
$\overline{WR}$	1	Output 3-State	The write signal. This signal reports when the CPU is writing data to memory or input/output. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
$\overline{MREQ}$	1	Output 3-State	The memory request signal. This signal reports the memory access cycle. "0" is output during the memory refresh cycle to report that memory is being refreshed. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	
$\overline{HALT}$	1	Output	"0" is output when the CPU executes the HALT instruction and enters halt status. High impedance output is possible using the $\overline{BUSREQ}/\overline{EV}$ pin.	

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PIN	Q'ty (Number)	TYPE	FUNCTION	
			MODE PIN = "0" (MODE 0)	MODE PIN = "1" (MODE 1)
$\overline{NMI}$	1	Input	The non-maskable interrupt request signal. This interrupt request has a higher priority than maskable interrupts. Interrupt enable/disable cannot be set with software.	
$\overline{INT}$	1	Input	The maskable interrupt request signal. Interrupt enable/disable can be set with software.	
$\overline{WAIT}$	1	Input	The wait request signal. This signal reports to the CPU that the specified memory or input/output is not ready to transfer data.	
$\overline{RESET}$	1	Input	A reset signal. The TMPZ84C112A internal reset signal.	A reset signal. The TMPZ84C112A internal CPU-only reset signal.
$\overline{BUSREQ}$ / $\overline{EV}$	1	Input	This signal has two meanings. BUSREQ signal : The bus request signal. This signal sets the CPU address bus, data bus, MREQ, IORQ, RD, WR and IORD to high impedance output. EV signal : This signal is used during development to set HALT, M1 and IOWR to high impedance output. This signal becomes valid when the BUSREQ/EV pin is latched at "0" during RESET pin rise. Normally, the BUSREQ/EV pin is used fixed at "0" during evaluation (development).	
$\overline{BUSACK}$	1	Output	The bus acknowledge signal. This signal reports when the BUSREQ signal is received and the CPU address bus, data bus and control signal are at high impedance in relation to the peripheral LSI.	
PA0~PA3	4	Input/Output 3-State	A general-purpose input/output port (port A) with which each nibble can be set for either input or output by program. Output is latched.	
PA4 / $\overline{RESET1}$	1	Input/Output 3-State /Input	Bit 4 of port A.	A reset signal. This signal resets all but the TMPZ84C112A internal CPU.
PB0~PB7	8	Input/Output 3-State	A general-purpose input/output port (port B) each nibble of which can be set for either input or output by program. Output is latched.	
PC0~PC7	8	Input/Output 3-State	A general-purpose input/output port (port C) each nibble of which can be set for either input or output by program. Output is latched.	
TOUT	1	Output	The 15-bit free-running timer output pin. The output pulse width differs depending on the externally connected pin (TMPZ84C112A).	
MODE	1	Input	TMPZ84C112A mode setting input. MODE pin = "0" : mode 0 is set. MODE pin = "1" : mode 1 is set.	

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PIN	Q'ty (Number)	TYPE	FUNCTION	
			MODE PIN = "0" (MODE 0)	MODE PIN = "1" (MODE 1)
XIN XOUT	2	Input Output	The oscillator connecting pin. Connect an oscillator with a frequency double that of the TMPZ84C112A operating clock (system clock).	
CKOUT	1	Output	The single-phase clock output. Divides by two and outputs the frequency of the oscillator connected to the XIN, XOUT pins. Used for clock input to other peripheral ICs.	
VCC	1		The power supply pin (+ 5V).	
VSS	1		The GND pin (0V).	

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3. FUNCTION DESCRIPTION

3.1 Block Diagram

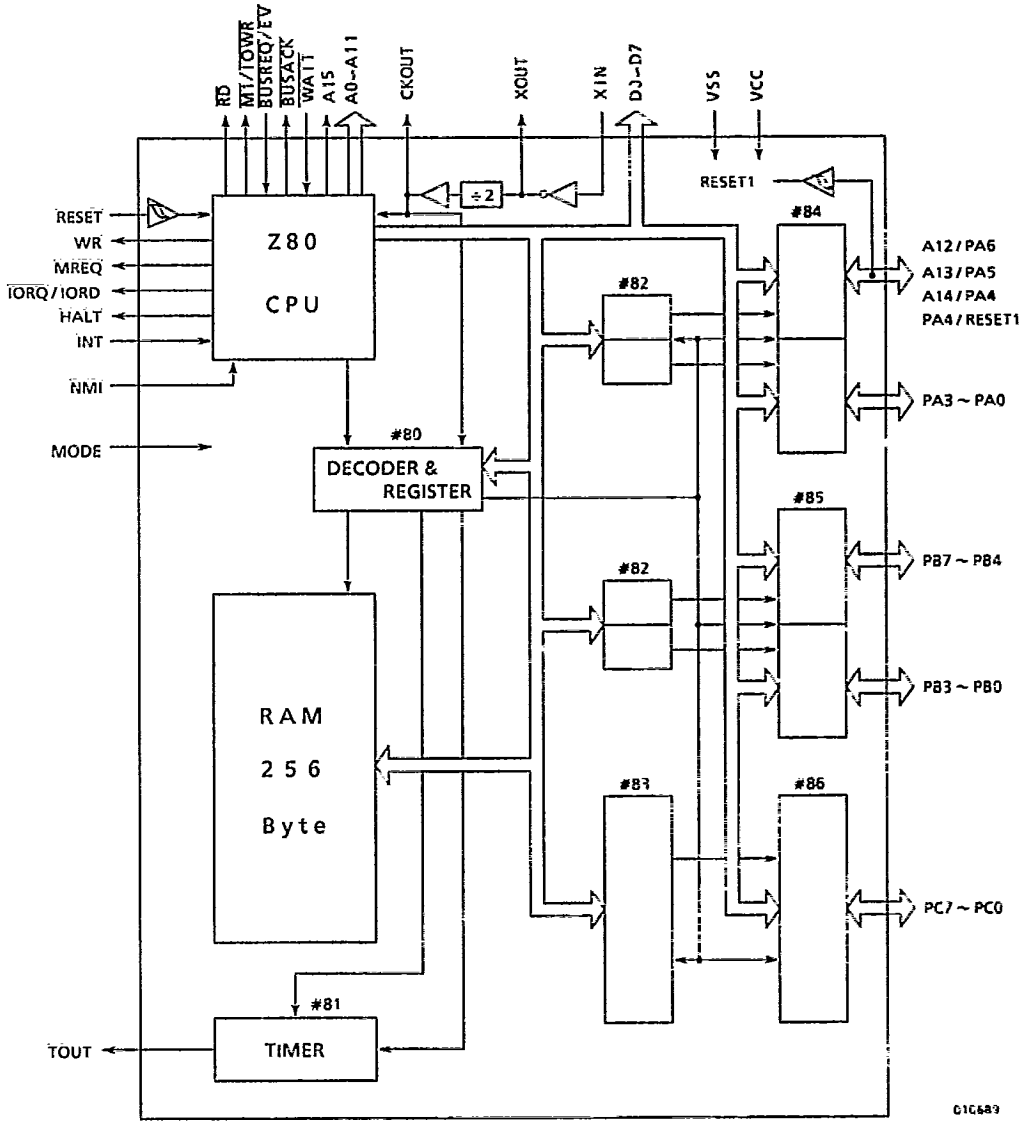


Figure 3.1.1 TMPZ84C112AN-6 / AF-6 Block Diagram

3.2 CPU Operation

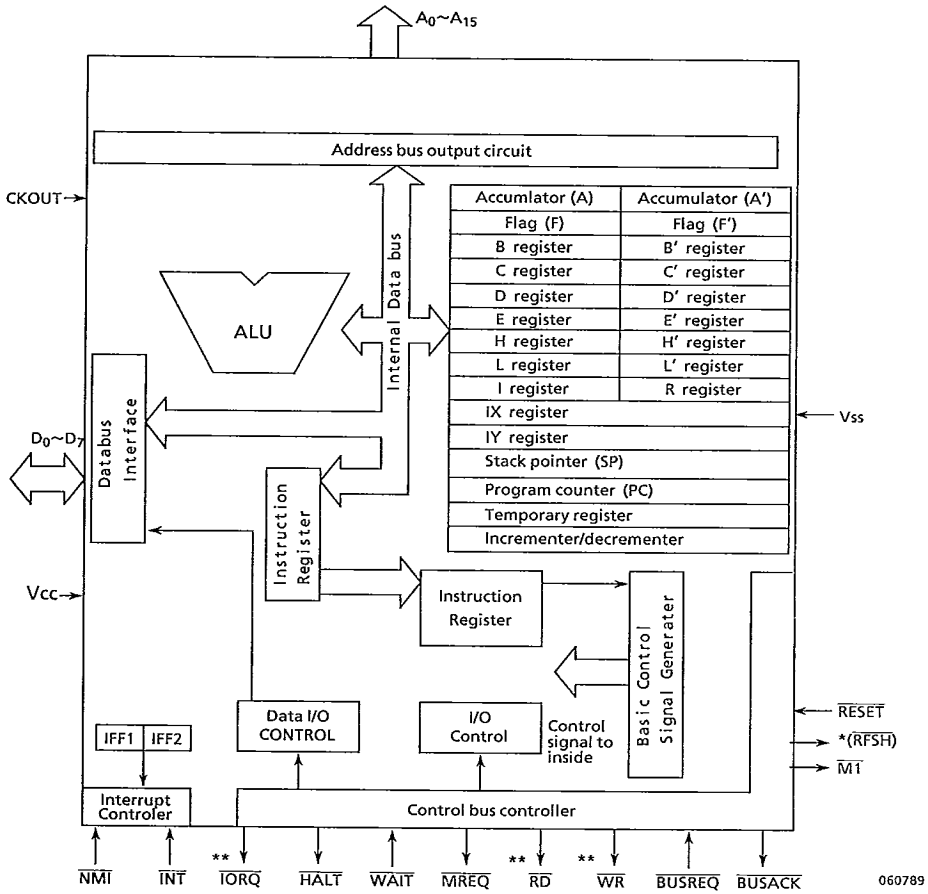
The following is an explanation of the system configuration and functions of the CPU of the TMPZ84C112A.

This CPU is fully compatible with the CMOS Z80MPU (TMPZ84C00A) of the TLCS-Z80 series, but the $\overline{RFSH}$ signal is not connected to an external pin.

As concerns the details, please refer to be chapter of TMPZ84C00A.

3.2.1 Block Diagram of The CPU

Figure 3.2.1 shows the block diagram of the CPU.



* The $\overline{RFSH}$ signal is not connected to an external pin.

** During mode 1 : The $\overline{IORD}$ signal is created from the $\overline{IORQ}$ signal and $\overline{RD}$ signal and connected to an external pin.

Figure 3.2.1 Block Diagram of The CPU

- External Pin Signals for Different Modes

The signals output to external pins by the TMPZ84C112A by means of mode control using the MODE pin differ as shown in Figure 3.2.20.

Pin \ Mode	Mode 0 (MODE = 0)	Mode 1 (MODE = 1)
A12/PA6 ~ A14/PA4	A12 ~ A14	PA6 ~ PA4
$\overline{IORQ}$ / $\overline{IORD}$	IORQ	IORD
M1 / $\overline{IOWR}$	M1	IOWR
PA4 / $\overline{RESET1}$	PA4	RESET1

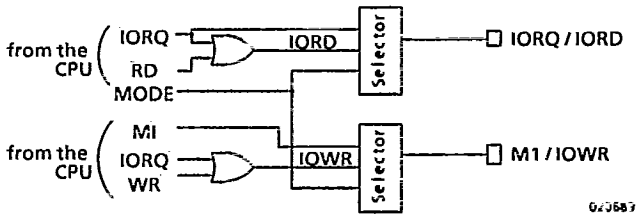


Figure 3.2.20 External Signal at Each Mode

3.3 I/O Map

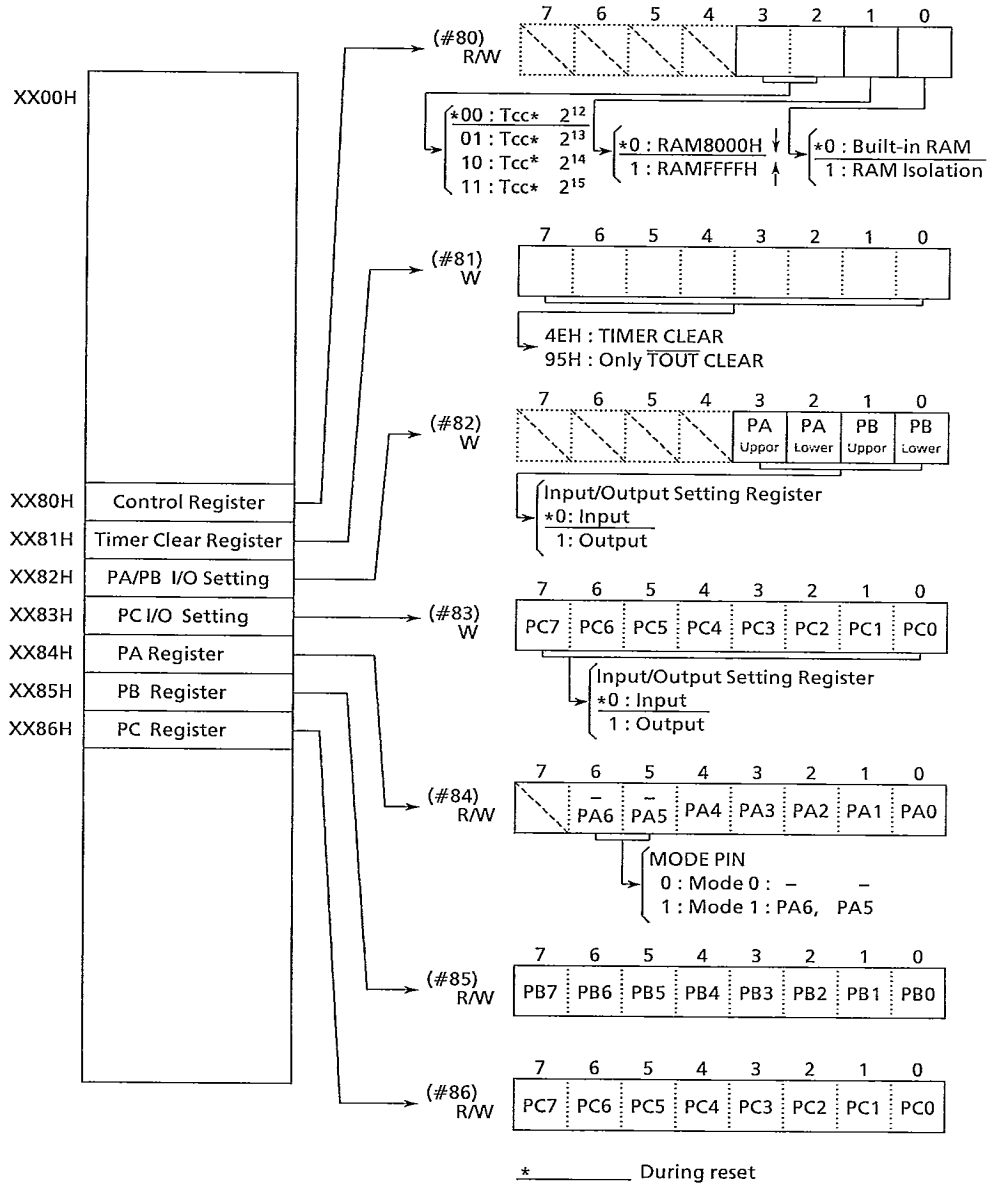


Figure 3.3.1 I/O Map

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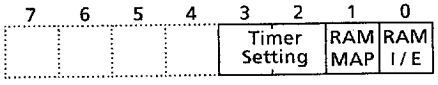
3.4 Input/Output Register Operation

3.4.1 Control Register



- Fixed at address 80 in the input/output area (accessed by the input/output instruction).
- Both read and write are possible.
- The upper 4 bits are '0000' when read.

(1) Bit 0 (RAM I/E) {built-in RAM/RAM isolation}

0 : built-in RAM (built-in RAM used)
1 : RAM isolation (built-in RAM not used)
— During reset Mode 0 : performed by the $\overline{\text{RESET}}$ pin.
Mode 1 : performed by the $\overline{\text{RESET1}}$ pin.

- This bit (RAM I/E) functions in conjunction with the setting of the MODE pin of the external input pin. That is, this bit is effective only when the MODE pin input is "0" (mode 0) and determines whether or not the built-in RAM is used.
  This bit is not effective when the MODE pin input is "1" (mode 1) and the built-in RAM is used, regardless of its settings.

(2) Bit 1 (RAM MAP) {specifies mapping of the built-in RAM}

0 : the built-in RAM is assigned to an area starting at address 8000H of the memory map, that is, from address 8000H to address 80FFH.
1 : the built-in RAM is assigned to an area ending at address FFFFH of the memory map, that is, from address FF00H to address FFFFH.
— During reset Mode 0 : performed by the $\overline{\text{RESET}}$ pin.
Mode 1 : performed by the $\overline{\text{RESET1}}$ pin.

- This bit (RAM MAP) functions in conjunction with the setting of the MODE pin of the external input pin and bit 0 (RAM I/E) at address 80H.
  When the MODE pin input is "1" (mode 1), the built-in RAM is assigned from address 8000H to address 80FFH of the memory map, regardless of the setting of this bit and bit 0 at address 80H.
  When the MODE pin input is "0" (mode 0), settings are valid only when bit 0 (RAM I/E) at address 80H is "0" (built-in RAM). When bit 0 (RAM MAP) is assigned from address 8000H to address 80FFH; when bit 1 (RAM MAP) is "1", it is assigned from address FF00H to address FFFFH. When bit 0 (RAM I/E) at address 80H is "1" (RAM isolation), however, the built-in RAM is ineffective.
  Table 3.4.1 shows these relationships.

Table 3.4.1 Relationship between the MODE pin, the RAM map bit (#80 (1)) and the RAM I/E (#80 (0)) bit

	MODE PIN		RAM MAP #80 <1>		RAM I/E #80 <0>	
	"0" Mode 0	"1" Mode 1	"0" 8000H ↓	"1" FFFFH ↑	"0" Built-in	"1" Isolation
① Mode 1 Built-in RAM fixed at addresses 8000H~80FFH.	1 (Mode 1)		×		×	
② Mode 0 Built-in RAM mapped to addresses 8000H~80FFH.	0 (Mode 0)		0 (8000H~80FFH)		0 (Built-in)	
③ Mode 0 Built-in RAM mapped to addresses FF00H~FFFFH.	0 (Mode 0)		1 (FF00H~FFFFH)		0 (Built-in)	
④ Mode 0 No built-in RAM (no access of built-in RAM).	0 (Mode 0)		×		1 (Isolation)	

× : This bit is not effective

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Note : When MODE pin=1 (mode 1), pins A14/PA4~A12/PA6 are used as PA4~PA6; therefore, RAM addresses A14~A12 are not decoded, thus creating a shadow RAM.

(3) Bit 3, Bit 2 (Timer Setting)

Bit 3	Bit 2		
0	0	:	$Tcc * 2^{12}$
0	1	:	$Tcc * 2^{13}$
1	0	:	$Tcc * 2^{14}$
1	1	:	$Tcc * 2^{15}$

– During reset Mode 0 : Reset by the $\overline{\text{RESET}}$ pin.
Mode 1 : Reset by the $\overline{\text{RESET1}}$ pin.

This register sets the number of 15-bit timer output stages.
Timer output is connected to the $\overline{\text{TOUT}}$ pin.
When the MODE pin is set to mode 1, this bit is reset by the $\overline{\text{RESET1}}$ pin.
Table 3.4.2 shows the relationship between operating frequency and timer output time.

Table 3.4.2 Operating Frequency and $\overline{\text{TOUT}}$ Output Time

Operating Frequency (CKOUT Output Frequency)	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2
	0	0	0	1	1	0	1	1
	2^{12}		2^{13}		2^{14}		2^{15}	
Tcc = 3.25MHz	1.25ms		2.51ms		5.03ms		10.06ms	
Tcc = 4.0MHz	1.02ms		2.05ms		4.1ms		8.2ms	
Tcc = 6.0MHz	0.68ms		1.37ms		2.74ms		5.47ms	

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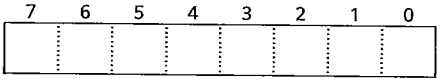
3.4.2 Timer Clear Command Register



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- Fixed at address 81H in the input/output area (accessed by the output instruction).
- Only write is possible.
- There is no influence from the $\overline{\text{RESET}}$ or $\overline{\text{RESET1}}$ pins.

(1) Bit 7~Bit 0 (Timer Clear Command Register)

- Used to clear the built-in 15-bit timer with software.
  The built-in timer is cleared and starts counting again from "0" when the data '4EH' is written to address 81H in the input/output area.
  This clear command sets the $\overline{\text{TOUT}}$ pin to "H" level.
- The $\overline{\text{TOUT}}$ pin can only be set to "H" level without clearing the built-in timer by writing the data '95H' to address 81H in the input/output area.

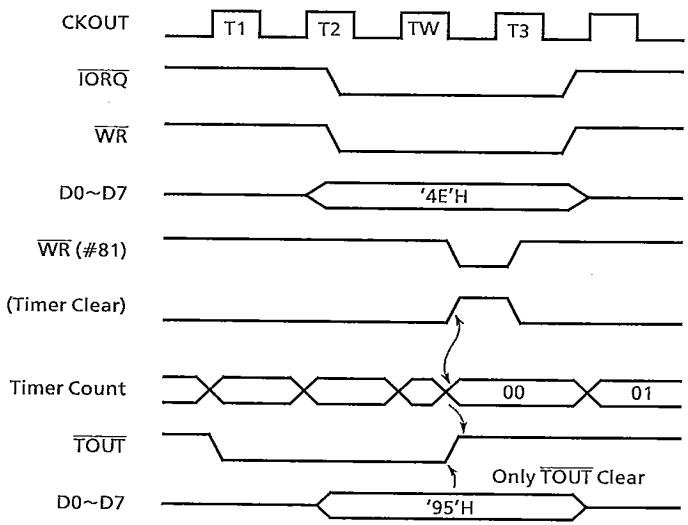

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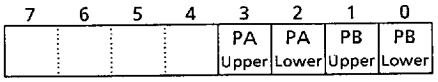
Figure 3.4.1 Clear Timing of the Timer Counter

3.4.3 Port A (PA), Port B (PB) Input/Output Setting Register



#82 [W]

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- Fixed at address 82H in the input/output area (accessed by the output instruction).
- Only write is possible.

(1) Bit 1~Bit 0 (PB7~PB0 Input/Output Control)

These bits set each nibble of the port B (PB7~PB0) upper bits (PB7~PB4) and lower bits (PB3~PB0) for input or output.

Bit 0 : sets PB3~PB0 (lower) input/output.
Bit 1 : sets PB7~PB4 (upper) input/output.
0 : sets input mode
1 : sets output mode
- During reset Mode 0 : performed by the $\overline{\text{RESET}}$ pin.
  Mode 1 : performed by the $\overline{\text{RESET1}}$ pin.

(2) Bit 3~Bit 2 (PA6~PA0 Input/Output Control)

These bits set each nibble of the port A (PA6~PA0) upper bits (PA6~PA4) and lower bits (PA3~PA0) for input or output.

Bit 2 : sets PA3~PA0 (lower) input/output.
Bit 3 : sets PA6~PA4 (upper) input/output.

MODE pin = "0" (mode 0)
: PA4 only
MODE pin = "1" (mode 1)
: PA6~PA4

0 : sets input mode
1 : sets output mode
- During reset Mode 0 : performed by the $\overline{\text{RESET}}$ pin.
  Mode 1 : performed by the RESET1 pin.

3.4.4 Port C (PC) Input/Output Setting Register

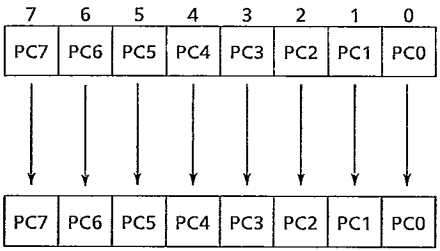
7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

#83 [W]

- Fixed at address 83H in the input/output area (accessed by the output instruction).
- Only write is possible.

(1) Bit 7~Bit 0 (PC7~PC0 Input/Output Control)

This register sets each bit of port C (PC7~PC0) for input or output.



The bits of the PC7~PC0 input/output setting register and PC7~PC0 register have a one-to-one correspondence. (Each bit can be set for input or output.)

0 : sets input mode
1 : sets output mode

During reset Mode 0 : performed by the $\overline{\text{RESET}}$ pin.
Mode 1 : performed by the $\overline{\text{RESET1}}$ pin.

3.4.5 Port A Register (PA7~PA0)

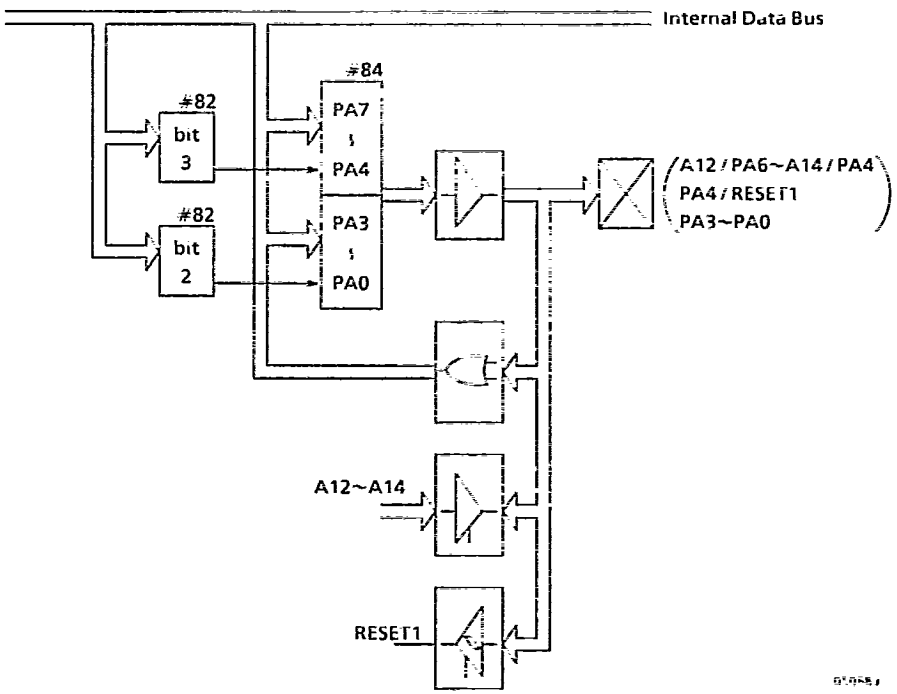
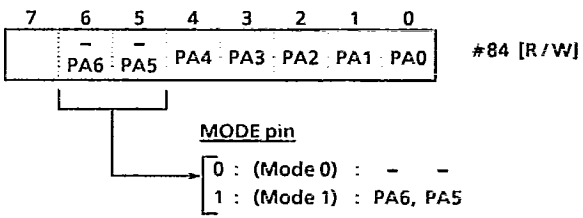


Figure 3.4.2 PA Port Block Diagram



- Fixed at address 84H in the input/output area (accessed by the input/output instruction).
- Both read and write are possible.
- The port A register is cleared to zero (0) by the reset operation.
  - Mode 0 : performed by the RESET pin.
  - Mode 1 : performed by the RESET1 pin.

(1) Bit 3~Bit 0 (PA3~PA0 Register)

This is PA3~PA0 Register.

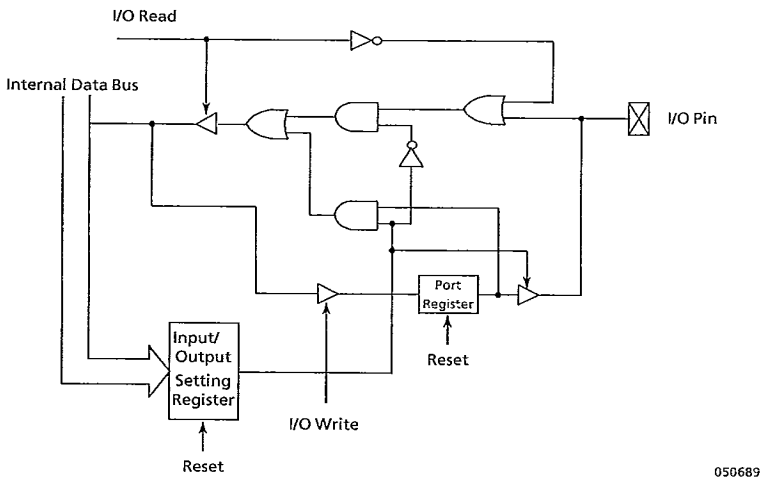


Figure 3.4.3 I/O Port Logic

Mode 0

- The $\overline{\text{RESET}}$ pin clears the input/output setting register to zero (0) and sets pins PA3~PA0 to the input mode.
- The $\overline{\text{RESET}}$ pin clears the PA3~PA0 port register to zero (0).

Mode 1 (no influence from the $\overline{\text{RESET}}$ pin)

- The $\overline{\text{RESET1}}$ pin clears the input/output setting register to zero (0) and sets pins PA3~PA0 to the input mode.
- The $\overline{\text{RESET1}}$ pin clears the PA3~PA0 port register to zero (0).

Input/output operation

- The input/output pin status can be read by executing the input instruction at the input mode setting.
- The port register contents can be read by executing the input instruction at the output mode setting.
- When "1" is written to the port register and then the input/output setting register is set to output to switch the input/output pin mode from input to output and to output "1", the previous data will not be output and no spikes will be generated in the port.
- The input/output setting of PA3~PA0 is determined by PA lower input/output setting register #82<2>.

(2) Bit 6~Bit 4 (PA6~PA4)

The PA6~PA4 register.

Figure 3.4.2 shows the input/output section block diagram and Figure 3.4.3 shows the input/output port logic circuit.

Mode 0

- The $\overline{\text{RESET}}$ pin clears the input/output setting register to zero (0) and sets pin PA4 to the input mode.
- The $\overline{\text{RESET}}$ pin clears the PA4 port register to zero (0).

Mode 1 (no influence from the $\overline{\text{RESET}}$ pin)

- The $\overline{\text{RESET1}}$ pin clears the input/output setting register to zero (0) and sets pins PA6~PA4 to the input mode.
- The $\overline{\text{RESET1}}$ pin clears the PA6~PA4 port register to zero (0).

Input/output operation

- The input/output pin status can be read by executing the input instruction at the input mode setting.
- The port register contents can be read by executing the input instruction at the output mode setting.
- When "1" is written to the port register and then the input/output setting register is set to output to switch the input/output pin mode from input to output and to output "1", the previous data will not be output and no spike will be generated in the port.
- The input/output setting of PA6~PA4 is determined by PA upper input/output setting register #82<3>.
- The number of PA ports differs depending on the MODE pin status.

MODE pin = "0" (Mode 0)

7	6	5	4	3	2	1	0
			PA4	PA3	PA2	PA1	PA0

- The 5-bit port for PA4~PA0.
- Data input to bit 7 - bit 5 by the input instruction are indeterminate.

MODE pin = "1" (Mode 1)

7	6	5	4	3	2	1	0
	PA6	PA5	PA4	PA3	PA2	PA1	PA0

- The 7-bit port for PA6~PA0.
- Data input to bit 7 by the input instruction are indeterminate.

Figure 3.4.4 shows the port input timing cycle chart and Figure 3.4.5 shows the output timing chart.

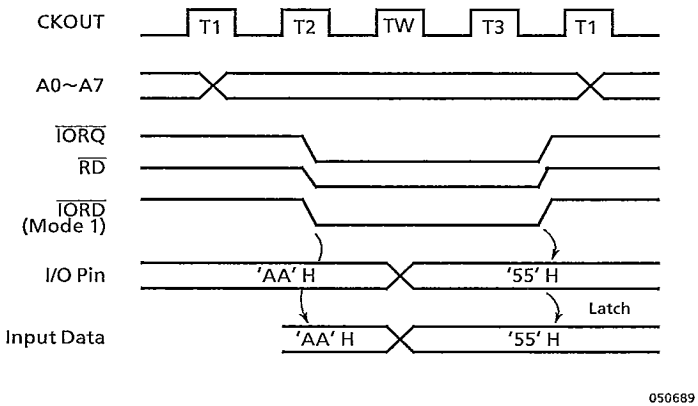


Figure 3.4.4 Input Cycle

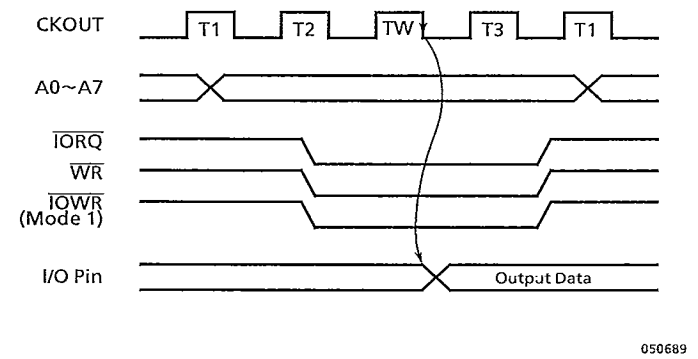


Figure 3.4.5 Output Cycle

3.4.6 Port B Register (PB7~PB0)

7	6	5	4	3	2	1	0	
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	#85 [R / W]

- Fixed at address 85H in the input/output area (accessed by the input/output instruction).
- Both read and write are possible.

Figure 3.4.6 shows the input/output section block diagram and Figure 3.4.3 shows the input/output port logic circuit.

Mode 0

- The $\overline{\text{RESET}}$ pin clears the input/output setting register to zero (0) and sets pins PB7~PB0 to the input mode.
- The $\overline{\text{RESET}}$ pin clears the PB7~PB0 port register to zero (0).

Mode 1 (no influence from the $\overline{\text{RESET}}$ pin)

- The $\overline{\text{RESET1}}$ pin clears the input/output setting register to zero (0) and sets pins PB7~PB0 to the input mode.
- The $\overline{\text{RESET1}}$ pin clears the PB7~PB0 port register to zero (0).

Input/output operation

- The input/output pin status can be read by executing the input instruction at the input mode setting.
- The port register contents can be read by executing the input instruction at the output mode setting.
- When "1" is written to the port register and then the input/output setting register is set to output to switch the input/output pin mode from input to output and to output "1", the previous data will not be output and no spike will be generated in the port.
- The input/output settings for PB3~PB0 are determined by PB lower input/output setting register #82<0>; the input/output settings for PB7~PB4 are determined by PB upper input/output setting register #82<1>.

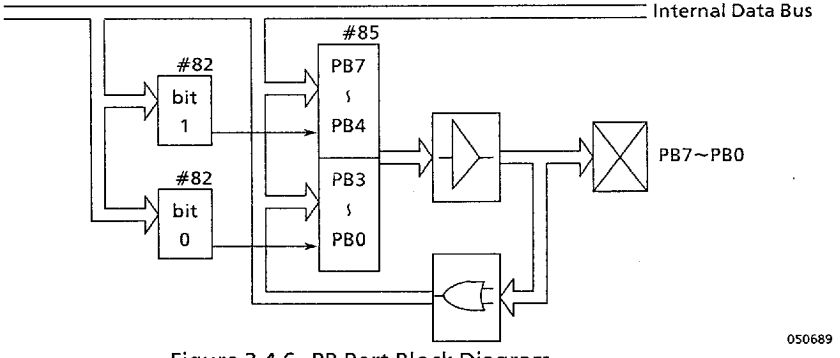


Figure 3.4.6 PB Port Block Diagram

3.4.7 Port C Register (PC7~PC0)

7	6	5	4	3	2	1	0	
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	#86 [R / W]

- Fixed at address 86H in the input/output area (accessed by the input/output instruction).
- Both read and write are possible.

Figure 3.4.7 shows the input/output section block diagram and Figure 3.4.3 shows the input/output port logic circuit.

Mode 0

- The $\overline{\text{RESET}}$ pin clears the input/output setting register to zero (0) and sets pins PC7~PC0 to the input mode.
- The $\overline{\text{RESET}}$ pin clears the PC7~PC0 port register to zero (0).

Mode 1 (no influence from the $\overline{\text{RESET}}$ pin)

- The $\overline{\text{RESET1}}$ pin clears the input/output setting register to zero (0) and sets pins PC7~PC0 to the input mode.
- The $\overline{\text{RESET1}}$ pin clears the PC7~PC0 port register to zero (0).

Input/output operation

- The input/output pin status can be read by executing the input instruction at the input mode setting.
- The port register contents can be read by executing the input instruction at the output mode setting.
- When "1" is written to the port register and then the input/output setting register is set to output to switch the input/output pin mode from input to output and to output "1", the previous data will not be output and no spike will be generated in the port.
- The input/output settings for PC7~PC0 are given a one-to-one correspondence to the PC port bits by the PC7~PC0 input/output setting registers #83<7> ~#83<0>.

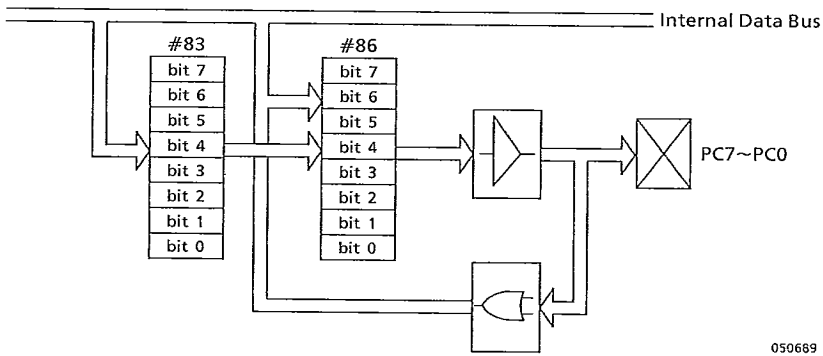


Figure 3.4.7 PC Port Block Diagram

3.4.8 Timer

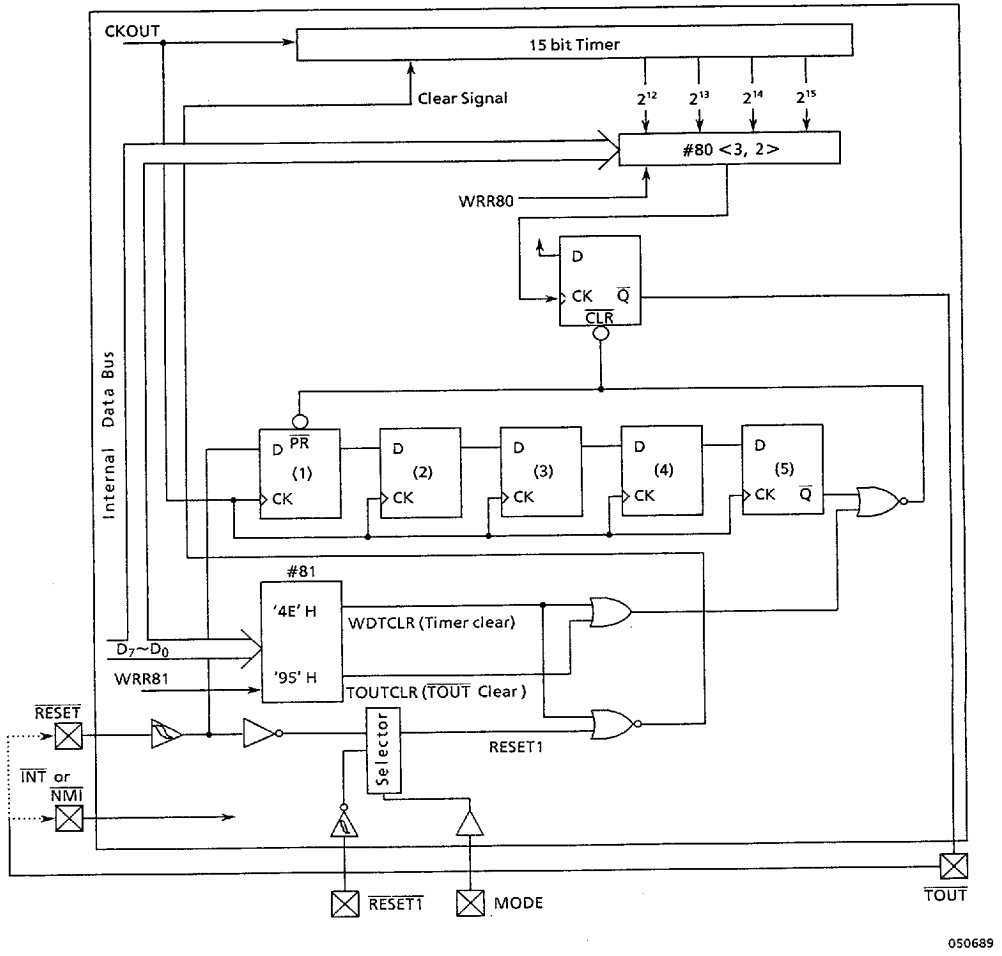


Figure 3.4.8 Timer Logic

- This is a 15-bit free-running timer which counts in synchronization with the rise of the CKOUT signal. Any of the stage 12~stage 15 timer outputs can be selected by the timer selection register (#80<3, 2> and output to the $\overline{TOUT}$ pin.

$\overline{\text{TOUT}}$ pin operation

This timer cannot be enabled or disabled by software. That is, this timer is always enabled.

The $\overline{\text{TOUT}}$ pin outputs a "0" level signal after the time (2^{12}, 2^{13}, 2^{14}, 2^{15}) selected with the timer selection register (#80<2, 3> has elapsed.

As shown below, there are two output pulse widths, depending on the method of connecting the $\overline{\text{TOUT}}$ pin.

(1) With the $\overline{\text{TOUT}}$ Pin Connected to the $\overline{\text{RESET}}$ Pin

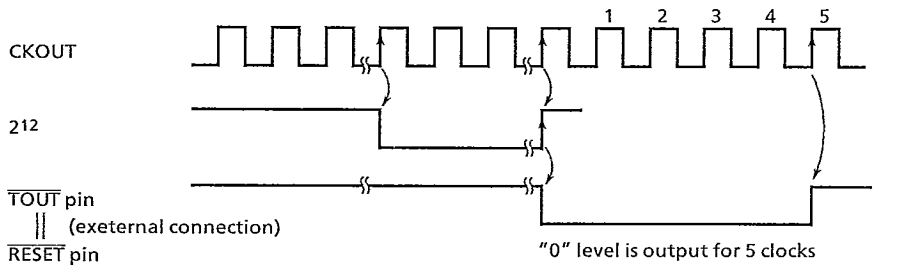


Figure 3.4.9 $\overline{\text{TOUT}}$ Output Timing (1)

(2) With the $\overline{\text{TOUT}}$ pin connected to other than the $\overline{\text{RESET}}$ pin

The "0" level output continues until cleared by software (writing '4E'H or '95'H to the timer clear command register (#81)) or a reset is caused by the $\overline{\text{RESET}}$ pin (mode 0) or $\overline{\text{RESET1}}$ pin (mode 1).

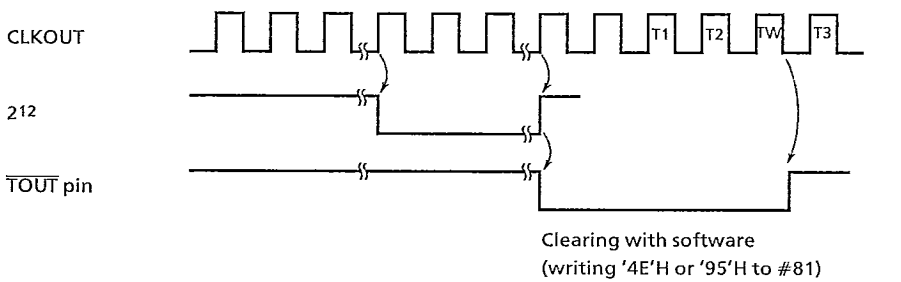


Figure 3.4.10 $\overline{\text{TOUT}}$ Output Timing (2)

3.4.9 Clock Generation

A stable clock signal can be output to the output pin (CKOUT) and built-in devices by connecting an oscillator with double the operating frequency between XIN and XOUT.

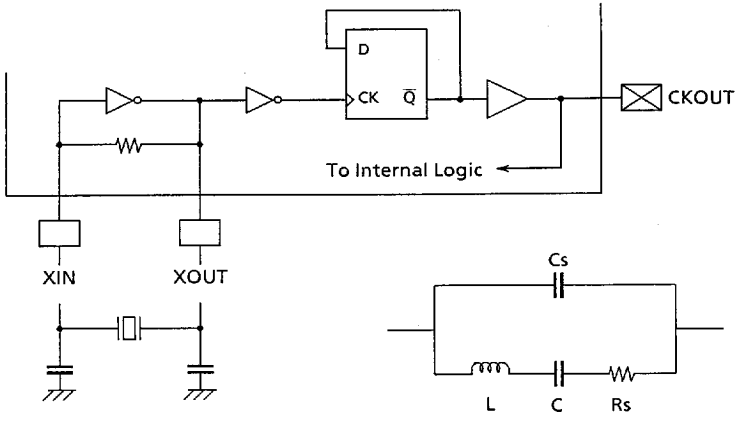


Figure 3.4.11 (a) Crystal Connection

Figure 3.4.11 (b) Oscillator Equivalent Circuit

Note : CKOUT wiring caution

The drive capacity of the 112A CKOUT output is greater than that of the other output pins to enable high-speed operation. Consequently, distortion occurs in the output waveform when long wiring is connected to the CKOUT pin and due to the L component of the wiring and capacitor discharge.

Note that CKOUT signal waveform distortion can result in system misoperation.

(1) When using a crystal oscillator, use the Tokyo Denpa MR8000-C20 (oscillation frequency: 8MHz) or MR12000-C20 (oscillation frequency: 12MHz) which have the following characteristics.

Oscillation Frequency f : 8MHz
Crystal oscillator "MR8000-C20"
CS ≦ 4PF
RS ≦ 30Ω
CIN = 22pF COUT = 33pF

f : 12Hz
Crystal oscillator "MR12000-C20"
CS ≦ 4PF
RS ≦ 25Ω
CIN = COUT = 33pF

(2) For the ceramic oscillator, use the Murata's CSA8.00 MT100 (oscillation frequency 8 MHz) or CSA12.0MT100 (oscillation frequency 12MHz) or the equivalent:

Oscillation ferquency	f : 8MHz	CIN=COUT=30pF
	f : 12MHz	CIN=COUT=30pF

3.4.10 Evaluator Functions

The TMPZ84C112A has a pin ($\overline{\text{BUSREQ}}/\overline{\text{EV}}$ pin) which can isolate the CPU so that it can function as an evaluator chip. This pin makes it possible to electrically isolate the built-in CPU (with high impedance) and perform emulations by receiving signals from an ICE (In-Circuit Emulator).

In this case, after the $\overline{\text{BUSREQ}}/\overline{\text{EV}}$ pin is set to "0" and a reset is applied with the $\overline{\text{RESET}}$ pin, the built-in CPU executes one machine cycle and becomes electrically isolated. After that, all sections of the device except the CPU are operated by instructions from the ICE CPU.

Table 3.4.3 shows the signal names for the isolated CPU and Figure 3.4.12 shows the signal timing.

Table 3.4.3 Isolated Pin Names

Isolation timing condition $\overline{\text{BUSREQ}}/\overline{\text{EV}}=0$	Isolated pin name
$\overline{\text{RESET}}$ signal rise	$\overline{\text{M1}}/\overline{\text{IOWR}}$, $\overline{\text{HALT}}$ pins
After 1 machine cycle	Pins A00~A15, D0~D7, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}/\overline{\text{IORD}}$

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Note : Caution is required because the $\overline{\text{BUSACK}}$ pin cannot be isolated.

In other words, the emulation mode or normal mode (the built-in Z80 operates) is determined at the rise of the $\overline{\text{RESET}}$ signal input to the TMPZ84C112A. That is, inputting "0" to the $\overline{\text{BUSREQ}}/\overline{\text{EV}}$ pin sets the evaluation mode and inputting "1" sets the normal mode.

The built-in CPU of the TMPZ84C112A is thus set to high impedance and the mode and status in which operation is performed by an external Z80 CPU are called "evaluation mode" and "inactive status". The mode and status in which the built-in Z80 CPU of the TMPZ84C112A operates are called "normal mode" and "active status".

The electrical characteristics in 4. and the timing in 5. are called, respectively, "active status" and "inactive status".

The signal which sets pins $\overline{M1}/\overline{IOWR}$ and HALT to high impedance status is made effective by latching the $\overline{BUSREQ}/EV$ pin signal to "0" with the $\overline{RESET}$ pin rise signal. Because of that, fix the $\overline{BUSREQ}/EV$ pin at "0" level when developing systems to be used in the evaluation status.

Due to the above, do not heedlessly change the $\overline{RESET}$ pin signal in any status.

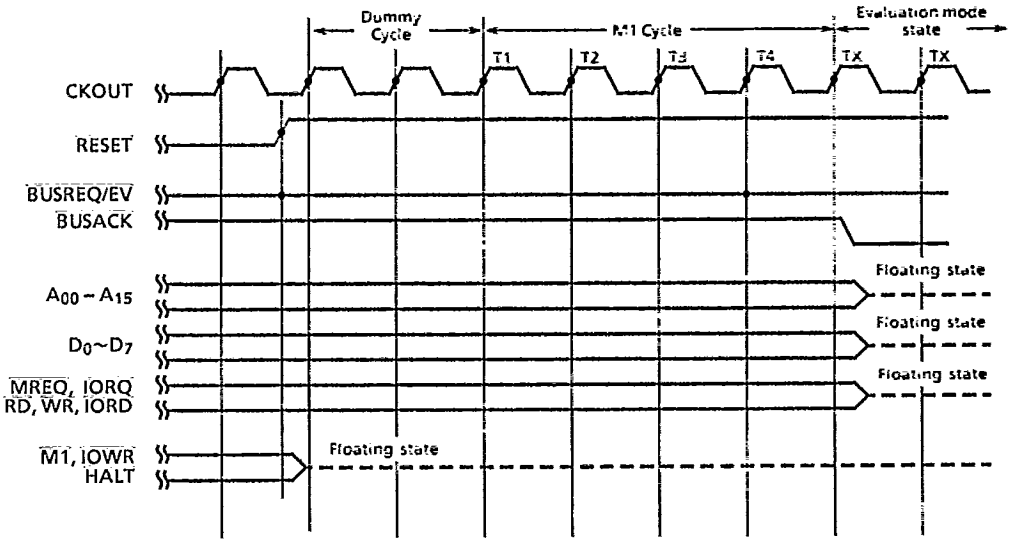

Figure 3.4.12 Evaluation Timing

The status in which the CPU is electrically isolated by high impedance is also called "inactive status", and the electrical characteristics and timing are indicated in the "inactive status" part.

Figure 3.4.13 shows the method of using an adaptor board (BM8029) to interface with the target system.

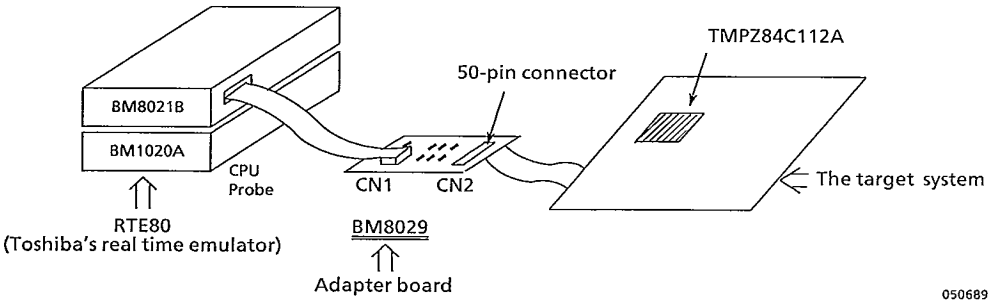

Figure 3.4.13 Typical connection

(For details, refer to the BM8029 instruction manual.)

The following is a simple explanation concern-ing the adaptor board (BM8029) and target PCB.

(a) Since the TMPZ84C112A in the target system is used as the emulator LSI and an emulator is also used, the built-in CPU is replaced by the emulator by releasing all buses (using high impedance).

The emulator interface circuit can isolate the emulator using a switch in the BM8029, thus making the adaptor board operate independently. Functionally, independent operation is equivalent to that of the TMPZ84C112A.

(b) The BM8029 internal connections are shown in the table below.

CN1 : ICE Connections (40-pin DIP socket)

Signal name	Pin no.		Signal name
A11	1	40	A10
A12	2	39	A9
A13	3	38	A8
A14	4	37	A7
A15	5	36	A6
CLK	6	35	A5
D4	7	34	A4
D3	8	33	A3
D5	9	32	A2
D6	10	31	A1
VCC	11	30	A0
D2	12	29	GND
D7	13	28	RFSH
D0	14	27	M1
D1	15	26	RESET
INT	16	25	BUSREQ
NMI	17	24	WAIT
HALT	18	23	BUSACK
MREQ	19	22	WR
IORQ	20	21	RD

CN2 : Target System Connections (50-pin connector)

Signal name	Pin no.		Signal name
*3 U-BUSACK	1	2	BUSACK
NC	3	4	WAIT
*3 U-BUSREQ/U-EV	5	6	BUSREQU/EV
NC	7	8	RESET
M1/iOWR	9	10	*1 TEST1
NC	11	12	A0
A1	13	14	A2
A3	15	16	A4
A5	17	18	A6
A7	19	20	A8
A9	21	22	A10
VCC	23	24	A11
*2 A12	25	26	*2 A13
*2 A14	27	28	A15
NC	29	30	D7
D6	31	32	D5
D4	33	34	D3
D2	35	36	D1
D0	37	38	*1 TEST2
INT	39	40	NMI
HALT	41	42	MREQ
IORQ/iORD	43	44	*3 U-RD
	45	46	NC
	47	48	MODE
	49	50	CLK OUT

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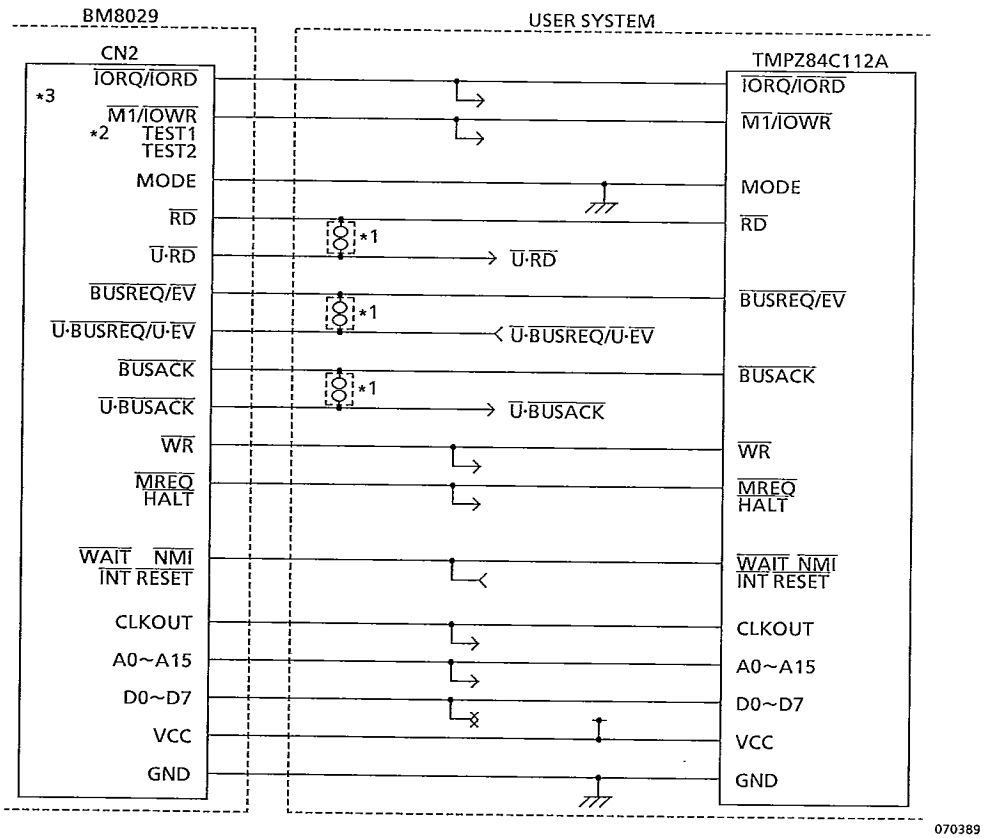
*1 : The TEST1 and TEST2 pins are used for tests, so do not connect anything to them.
*2 : Do not connect anything toA12-A14when the TMPZ84C112A is operating in mode 1.
*3 : The U-RD, U-BUSREQ/U-EV and U-BUSACK signals are used by the customer.

Figure 3.4.4 (a) BM8029 Pin Connection Table

(d) For target system connection, a 50-pin connector is available for direct connection to the pins of the TMPZ84C112A in the target system.

The target system can be connected by soldering directly to the TMPZ84C112A signals or by using a connector. Select in accordance with the amount of space on the target system board.

(e) Figure 3.4.13 shows connection to the adaptor board (BM8029) when the TMPZ84C112A is used in mode 0.



* The symbols ->, -< and -X indicate connection to devices in the user system other than the TMPZ84C112A.

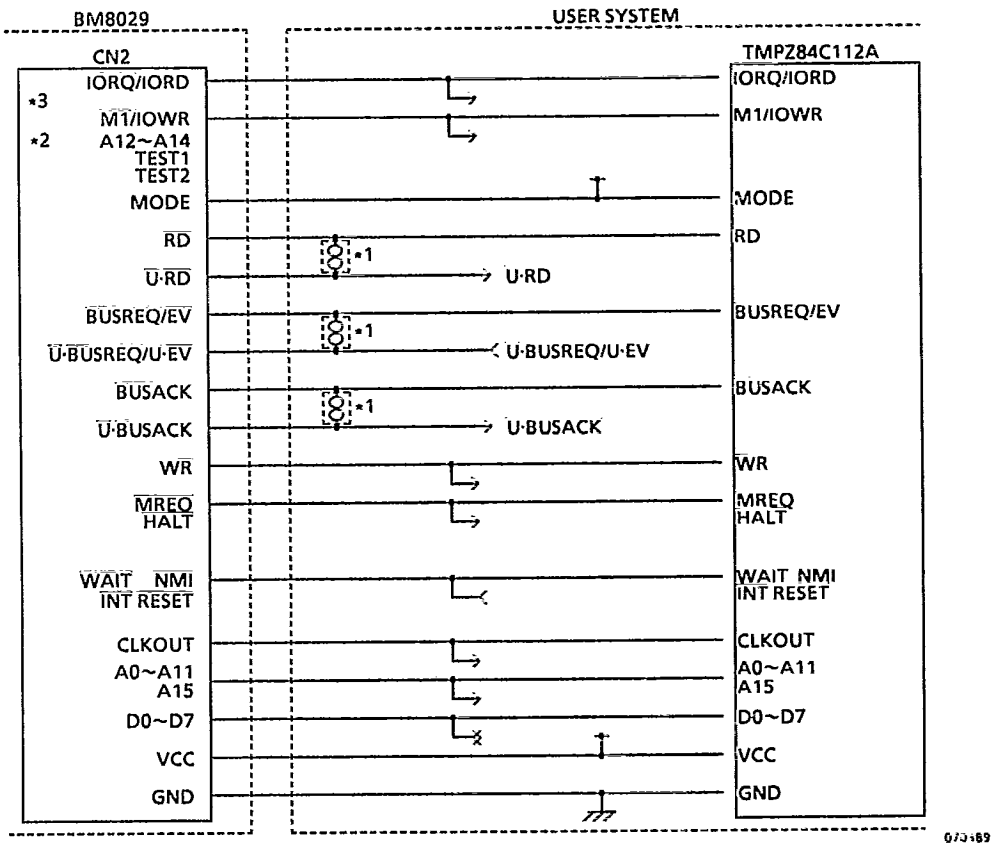
*1:Connect when the adaptor board is not connected.

*2:The TEST1 and TEST2 pins are not connected to anything.

*3:The $\overline{IORQ}/\overline{IORD}$ and $\overline{M1}/\overline{IOWR}$ pins operate as the $\overline{IORQ}$ and $\overline{M1}$ pins in mode 0.

Figure 3.4.13 Typical Mode 0 Connection

(f) Figure 3.4.14 shows connection to the adaptor board (BM8029) when the TMPZ84C112A is used in mode 1.



* The symbols ->, -< and -X indicate connection to devices in the user system other than the TMPZ84C112A.

*1:Short when the adaptor board is not connected.

*2:The A12 - A14, TEST1 and TEST2 pins are not connected to anything.

*3:The IORQ/IORD and M1/IOWR pins operate as the IORD and IOWR pins in mode1.

Figure 3.4.14 Typical Mode 1 Connection

The evaluation mode (active status) or normal mode (active status) (the built-in Z80 operates) is determined at the rise of the $\overline{\text{RESET}}$ signal input to the TMPZ84C112A. That is, inputting "0" to the $\overline{\text{BUSREQ}}$/$\overline{\text{EV}}$ pin sets the inactive status and inputting "1" sets the active status.

Inactive status : used when developing a system which operates the Z80 CPU of the I.C.E.

Active status : operates the built-in Z80 CPU.

Mode 0/mode 1 can be set using the MODE pin in any status.

Table 3.4.5 shows the various states and their conditions for the TMPZ84C112A.

Table 3.4.5 TMPZ84C112A Status

Condition \ Status	Inactive status		Active status	
$\overline{\text{BUSREQ}}$/$\overline{\text{EV}}$ pin status at the $\overline{\text{RESET}}$ pin rise.	0		1	
MODE pin status	Mode 0	Mode 1	Mode 0	Mode 1
	0	1	0	1

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The following is a simple description of the development of a system using the TMPZ84C112A.

The following reference materials and development tools are available.

1. 8-bit microcomputer, TLCS-Z80 Development System Manual.
2. Adaptor board (BM8029)
   BM8029 Instruction Manual.

3.4.11 Using the RESET and RESET1 Pins

MODE pin = "1" (Mode 1)

[Example]

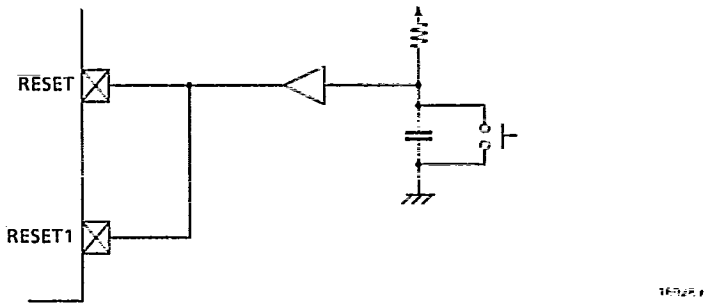

Figure 3.4.15 Example 1

MODE pin = "1" (Mode 1)

[Example]

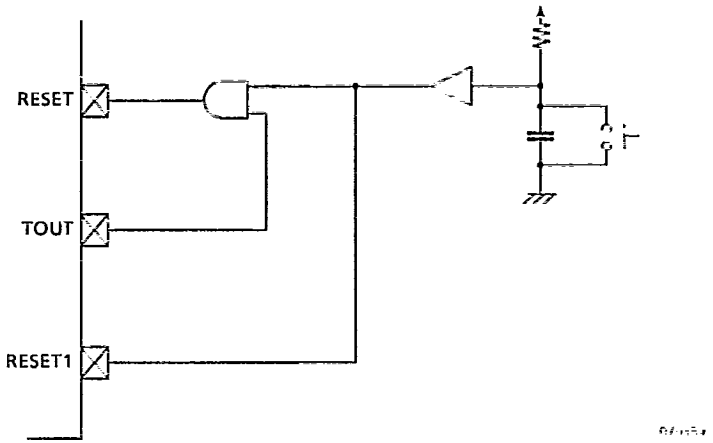

Figure 3.4.16 Example 2

When MODE pin = "0" (mode 0), the PA4/RESET1 pin becomes PA4.

4. ELECTRICAL CHARACTERISTICS

4.1 MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	−0.5~+7.0	V
V_{IN}	Input Voltage	−0.5~V_{CC}+0.5	V
P_D	Power Dissipation (Ta=85°C)	250	mV
T_{SOLDER}	Soldering Temperature (10sec)	260	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−10~70	°C

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4.2 DC ELECTRICAL CHARACTERISTICS

$T_{OPR}=-10°C\sim70°C$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$

SYMBOL	ITEM	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{ILC}	Low level Clock input voltage (During external input)			−0.3	—	0.6	V
V_{IHC}	High level Clock input voltage (During external input)			$V_{CC}-0.6$	—	$V_{CC}+0.3$	V
V_{ILS}	Input Low level voltage ($\overline{RESET}$, $\overline{RESET1}$)	$V_{CC}\geqq4.5V$		0	—	V_{CC}*0.25	V
V_{IHS}	Input High level voltage ($\overline{RESET}$, $\overline{RESET1}$)	$V_{CC}\geqq4.5V$		V_{CC}*0.75	—	V_{CC}	V
V_{IL1}	Input Low level voltage (MODE)			0	—	V_{CC}*0.3	V
V_{IH1}	Input High level voltage (MODE)			V_{CC}*0.7	—	V_{CC}	V
V_{IL}	Input Low level voltage			−0.5	—	0.6	V
V_{IHI}	Input High level voltage			2.3	—	V_{CC}	V
V_{OL}	Output Low voltage	$I_{OL}=2.0mA$		—	—	0.4	V
V_{OH1}	Output High voltage (I)	$I_{OH}=-1.6mA$		2.4	—	—	V
V_{OH2}	Output High voltage (II)	$I_{OH}=-250\mu A$		$V_{CC}-0.8$	—	—	V
I_{LI}	Input Leakage Current	$V_{SS}\leqq V_{IN}\leqq V_{CC}$		—	—	±10	μA
I_{LO}	3-State Output Leakage Current in Flat	$V_{SS}+0.4\leqq V_{OUT}\leqq V_{CC}$		—	—	±10	μA
I_{CC1}	Power supply Current	$V_{CC}=5V$ f_{CLK}=(Note 1) $V_{IHC}=V_{IH}=V_{IH1}$ $=V_{HS}=V_{CC}-0.2V$ $V_{ILC}=V_{IL}=V_{IL1}$ $=V_{LS}=0.2V$	4MHz	—	10	20	mA
			6.144 MHz	—	15	25	mA

Note 1: $f_{CLK}=1/T_{CC}$ (MIN)

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4.3 AC Electrical Characteristics (Active State 1/3)

$T_{OPR}=-10°C\sim70°C$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$

No.	SYMBOL	PARAMETER	CKOUT = 4MHZ		CKOUT = 6.144MHZ		UNIT
			MIN.	MAX.	MIN.	MAX	
1	TcC	Clock Cycle Time	250	DC	162	DC	ns
2	TwCh	Clock Pulse Width (High)	110	DC	65	DC	ns
3	TwCl	Clock Pulse Width (Low)	110	DC	65	DC	ns
4	TfC	Cock Fall Time	—	30	—	20	ns
5	TrC	Clock Rise Time	—	30	—	20	ns
6	TdCr (A)	Clock ↑ to Address Valid Delay	—	110	—	90	ns
7	TdA (MREQf)	Address Valid to MREQ ↓ Delay	65	—	35	—	ns
8	TdCf (MREQf)	Clock ↓ to MREQ ↓ Delay	—	85	—	70	ns
9	TdCr (MREQr)	Clock ↑ to MREQ ↑ Delay	—	85	—	70	ns
10	TwMREQh	MREQ Pulse Width (High)	110	—	65	—	ns
11	TwMREQl	MREQ Pulse Width (Low)	220	—	135	—	ns
12	TdCf (MREQr)	Clock ↓ to MREQ ↑ Delay	—	85	—	70	ns
13	TdCf (RDf)	Clock ↓ to RD ↓ Delay	—	95	—	80	ns
14	TdCr (RDr)	Clock ↑ to RD ↑ Delay	—	85	—	70	ns
15	TsD (Cr)	Data Setup Time to Clock ↑	35	—	30	—	ns
16	ThD (RDr)	Data Hold Time to RD ↑	0	—	0	—	ns
17	TsWAIT (Cf)	WAIT Setup Time to Clock ↓	70	—	60	—	ns
18	ThWAIT (Cf)	WAIT Hold Timer after Clock ↓	10	—	10	—	ns
19	TdCr (M1f)	Clock ↑ to M1 ↓ Delay	—	100	—	80	ns
20	TdC r(M1r)	Clock ↑ to M1 ↑ Delay	—	100	—	80	ns
21	TdCf (RDr)	Clock ↓ to RD ↑ Delay	—	85	—	70	ns
22	TdCr (RDf)	Clock ↑ to RD ↓ Delay	—	85	—	70	ns
23	TsD (Cf)	Data Setup to Clock ↓ during M2, M3, M4 or M5 Cycle	50	—	40	—	ns
24	TdA (IORQf)	Address Stable prior IORQ ↓	180	—	110	—	ns
25	TdCr (IORQf)	Clock ↑ to IORQ ↓ Delay	—	75	—	65	ns
26	TdCf (IORQr)	Clock ↓ to IORQ ↑ Delay	—	85	—	70	ns
27	TdD (WRf)	Data Stable Prior to WR ↓	80	—	25	—	ns
28	TdCf (WRf)	Clock ↓ to WR ↓ Delay	—	80	—	70	ns
29	TwWR	WR Pulse Width	220	—	135	—	ns

AC Electrical Characeristics (Active State 2/3)

No.	SYMBOL	PARAMETER	CKOUT = 4MHZ		CKOUT = 6.144MHZ		UNIT
			MIN.	MAX.	MIN.	MAX.	
30	TdCf (WRr)	Clock ↓ to $\overline{WR}$ ↑ Delay	—	80	—	70	ns
31	TdD (WRf)	Data Stable Prior to $\overline{WR}$ ↓	-10	—	-55	—	ns
32	TdCr (WRf)	Clock ↑ to $\overline{WR}$ ↓ Dealy	—	65	—	60	ns
33	TdWRr (D)	Data Stable from $\overline{WR}$ ↑	60	—	30	—	ns
34	TdCf (HALT)	Clock ↓ to $\overline{HALT}$ ↑ or ↓	—	300	—	260	ns
35	TwNMI	$\overline{NMI}$ Pulse Width	120	—	120	—	ns
36	TsBUSREQ (Cr)	$\overline{BUSREQ}$ Setup Time to Clock ↑	50	—	50	—	ns
37	ThBUSREQ (Cr)	$\overline{BUSREQ}$ Hold Time after CLock ↑	10	—	10	—	ns
38	TdCr (BUSACKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay	—	100	—	90	ns
39	TdCf (BUSACKr)	Clock ↓ to BUSACK ↑ Delay	—	100	—	90	ns
40	TdCr (Dz)	Clock ↑ to Data Float Delay	—	90	—	80	ns
41	TdCr (CTz)	Clock ↑ to Control Outputs Float Delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	—	80	—	70	ns
42	TdCr (Az)	Clock ↑ to Address Float Delay	—	90	—	80	ns
43	TdCr (A)	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to Address Hold Time	80	—	35	—	ns
44	TsRESET (Cr)	$\overline{RESET}$ to Clock ↑ Setup Time	60	—	60	—	ns
45	ThRESET (Cr)	$\overline{RESET}$ to Clock ↑ Hold Time	10	—	10	—	ns
46	TsINTf (Cr)	$\overline{INT}$ to Clock ↑ Setup Time	80	—	70	—	ns
47	TsINTr (Cr)	$\overline{INT}$ to Clock ↑ Hold Time	10	—	10	—	ns
48	TdM1f (IORQf)	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ Delay	565	—	365	—	ns
49	TdCf (IORQf)	Clock ↓ to $\overline{IORQ}$ ↓ Delay	—	85	—	70	ns
50	TdCr (IORQr)	Clock ↑ to $\overline{IORQ}$ ↑ Delay	—	85	—	70	ns
51	TdCf (D)	Clock ↓ Data Valid Delay	—	150	—	130	ns
52	TdCf (POUT)	Clock ↓ to Port Data Delay	—	400	—	300	ns
53	TSPIN (IORDf)	Port Input Setup Time to $\overline{IORQ}$, $\overline{RD}$ ↓	0	—	0	—	ns
54	Th PIN	Port Input Hold Time to $\overline{IORQ}$, $\overline{RD}$ ↑	0	—	0	—	ns
55	TdC (TOUTf)	Clock ↑ to $\overline{TOUT}$ ↓ Delay	—	240	—	160	ns
56	Td (TOUTr)	Clock ↑ to $\overline{TOUT}$ ↑ Delay	—		—	165	ns

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AC Electrical Characeristics (Active State 3/3)

No.	SYMBOL	PARAMETER	CKOUT = 4MHZ		CKOUT = 6.144MHZ		UNIT
			MIN.	MAX.	MIN.	MAX.	
57	TcTOUTT	TOUT Cycle<#80<3, 2>> Mode 0 : 00 Mode 1 : 01 Mode 2 : 10 Mode 3 : 11	Typ. T1 * 2^{14} T1 * 2^{15} T1 * 2^{14} T1 * 2^{15}		Typ. T1 * 2^{14} T1 * 2^{15} T1 * 2^{14} T1 * 2^{15}		ns
58	Tdcr(IOWRf)	Clock ↑ to IOWR ↓ Delay	–	80	–	70	ns
59	Tdcf (IOWRf)	Clock ↓ to IOWR ↑ Delay	–	90	–	75	ns
60	Tdcr (IORDf)	Clock ↑ to IORD ↓ Delay	–	90	–	75	ns
61	Tdcf (IORDf)	Clock ↓ to IORD ↑ Delay	–	90	–	75	ns

Note 1: AC Test condition (1) VCC=5V±10%,
VIH=2.4V, VIL=0.4V, VIHC=VCC-0.6V,
VILC=0.6V, VOH=2.2V, VOL=0.8V

4.4 Timing Diagram (Active State)

Figure 4.4.1 to 4.4.9 show the basic timing of respective operations. Numbers shown in the Figures correspond with those in the AC ELECTRICAL CHARACTERISTICS Table in 4.3.

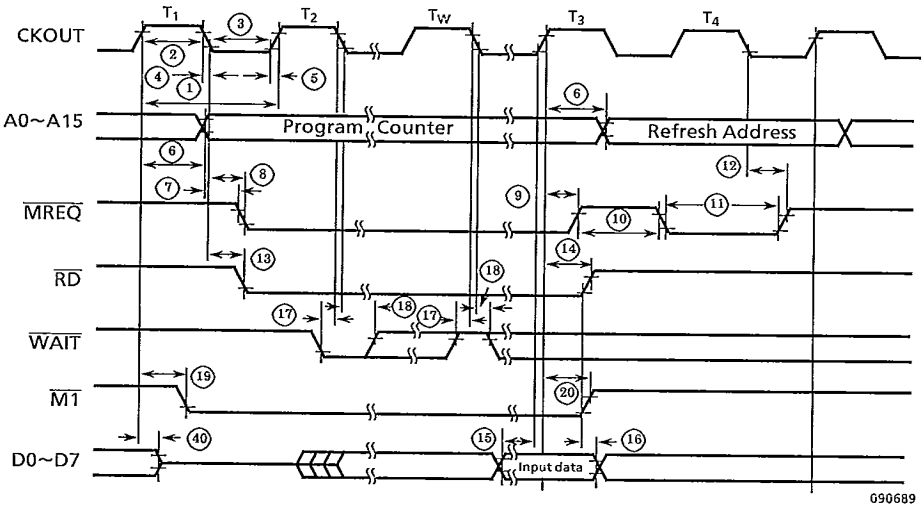


Figure 4.4.1 OP-Code Fetch Cycle

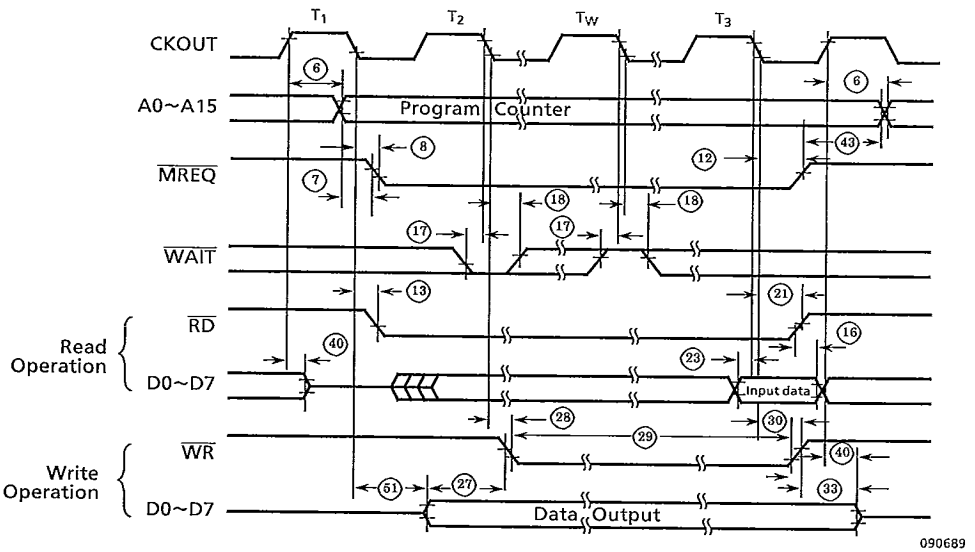
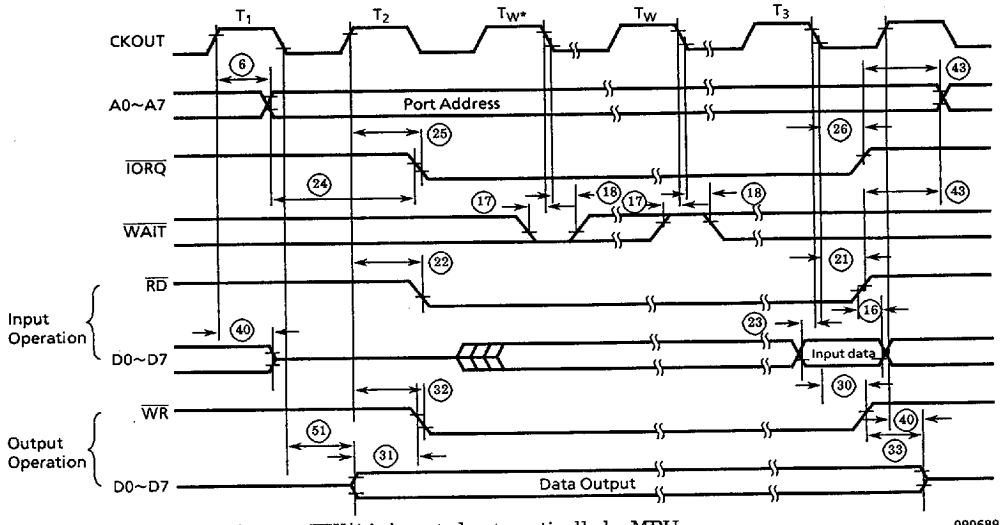


Figure 4.4.2 Memory Read/Write Cycle



Note : 1 wait state (TW*) is inserted autematically by MPU.

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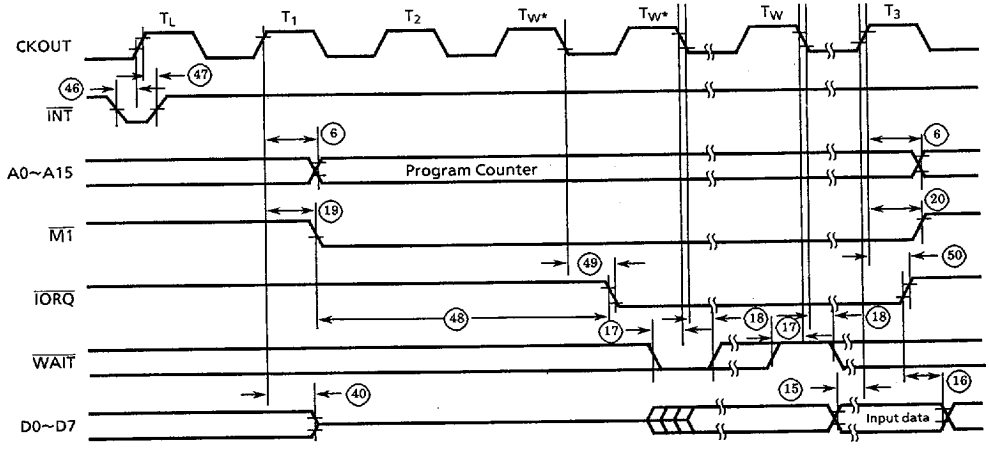
Figure 4.4.3 Input/Output Cycle



Note 1 : TL is the final state of the preceding instruction.
Note 2 : 2 wait state (TW*) is inserted automatically by MPU.

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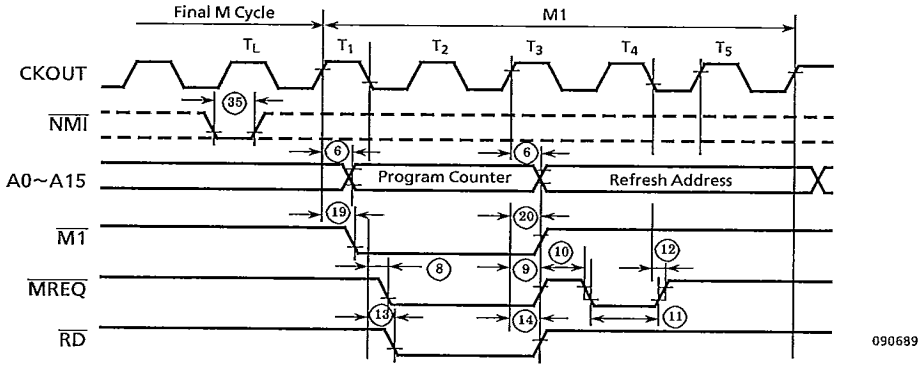
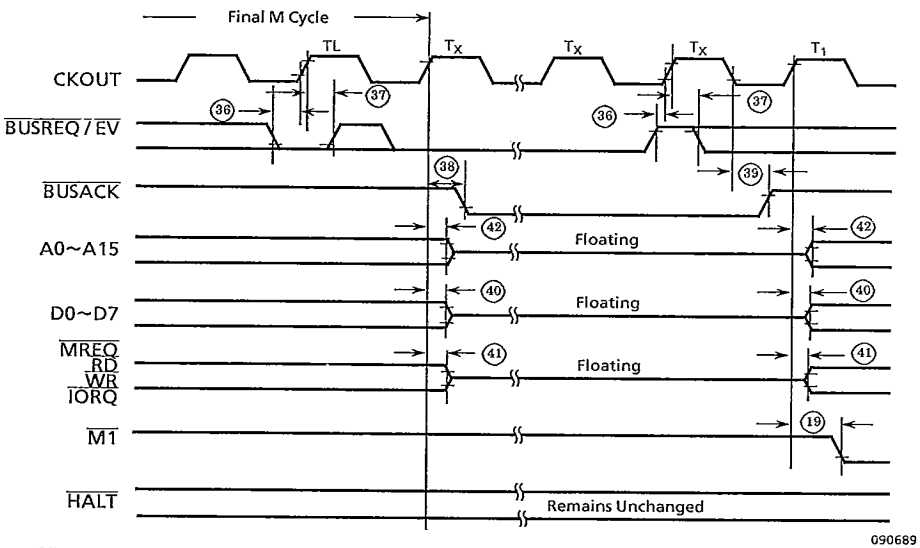
Figure 4.4.4 Interrupt Request/Acknowledge Cycle



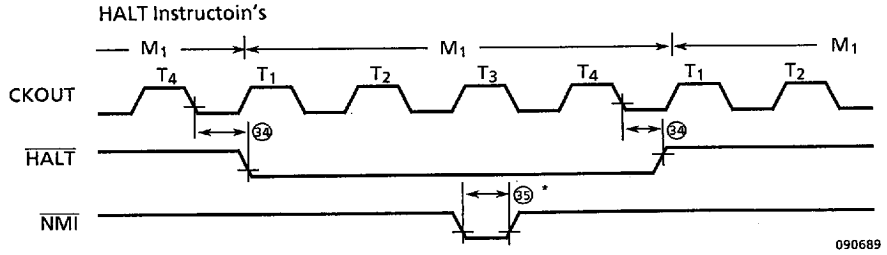
Note : $\overline{NMI}$ is asynchronous input but in order to assure the positive response in the following cycle, $\overline{NMI}$ trailing edge signal must be generated keeping abreast of the leading edge of preceding TL state.

Figure 4.4.5 Non-Maskable Interrupt Request Cycle



Note 1 : TL is the final state of any machine cycle.
Note 2 : TX is optional clock used by requested peripheral LSI.

Figure 4.4.6 Bus Request/Acknowledge Cycle



Note : $\overline{INT}$ signal is also used for releasing from the halt state.

Figure 4.4.7 HALT Acknowledge Cycle

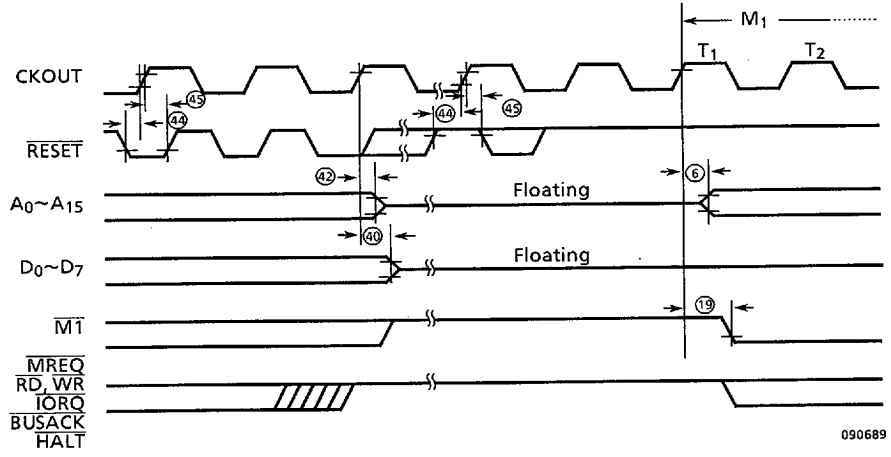


Figure 4.4.8 Reset Cycle

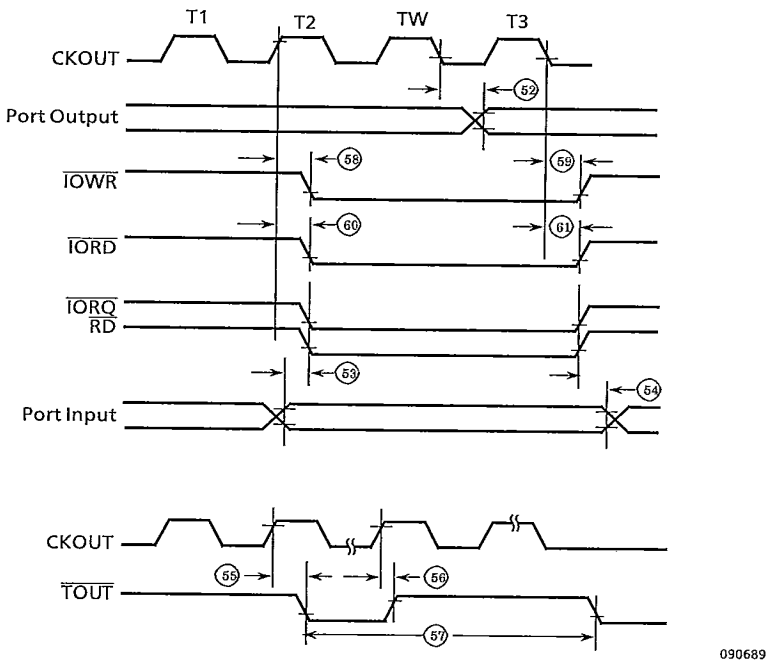


Figure 4.4.9 Input/Output Timing

4.5 AC ELECTRICAL CHARACTERISTICS (Inactive State)

$T_{OPR} = -10°C \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

No.	SYMBOL	PARAMETER	CKOUT = 4MHz		CKOUT = 6.144MHZ		UNIT
			MIN.	MAX.	MIN.	MAX.	
1	TcC (OUT)	Clock Cycle Time (Output)	250	DC	162	DC	ns
2	TwCh (OUT)	Clock Pulse Width (High Output)	110	DC	65	DC	ns
3	TwCl (OUT)	Clock Pulse Width (Low Output)	110	DC	65	DC	ns
4	TfC (OUT)	Clock Fall Time (Output)	—	30	—	20	ns
5	TrC (OUT)	Clock Rise Time (Output)	—	30	—	20	ns
6	TdCf (POUT)	Clock ↓ to Port Data Delay	—	400	—	300	ns
7	TSPIN (IORDf)	Port Input Setup Time to $\overline{IORQ}$, $\overline{RD}$ ↓	0	—	0	—	ns
8	Th PIN	Port Input Hold Time to $\overline{IORQ}$, $\overline{RD}$ ↑	0	—	0	—	ns
9	TdC (TOUTf)	Clock ↑ to $\overline{TOUT}$ ↓ Delay	—	240	—	160	ns
10	Td (TOUTr)	Clock ↑ to $\overline{TOUT}$ ↑ Delay	—	250	—	165	ns
11	TcTOUTT	$\overline{TOUT}$ Cycle <#80<3, 2>> Mode 0 : 00 Mode 1 : 01 Mode 2 : 10 Mode 3 : 11	Typ. $T1 * 2^{12}$ $T1 * 2^{13}$ $T1 * 2^{14}$ $T1 * 2^{15}$		Typ. $T1 * 2^{12}$ $T1 * 2^{13}$ $T1 * 2^{14}$ $T1 * 2^{15}$		ns

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Note 1: AC Test condition (1) VCC = 5V ± 10%,
VIH = 2.4V, VIL = 0.4V, VIHC = VCC-0.6V
VILC = 0.6V, VOH = 2.2V, VOL = 0.8V

4.6 AC Timing Diagram (Inactive State)

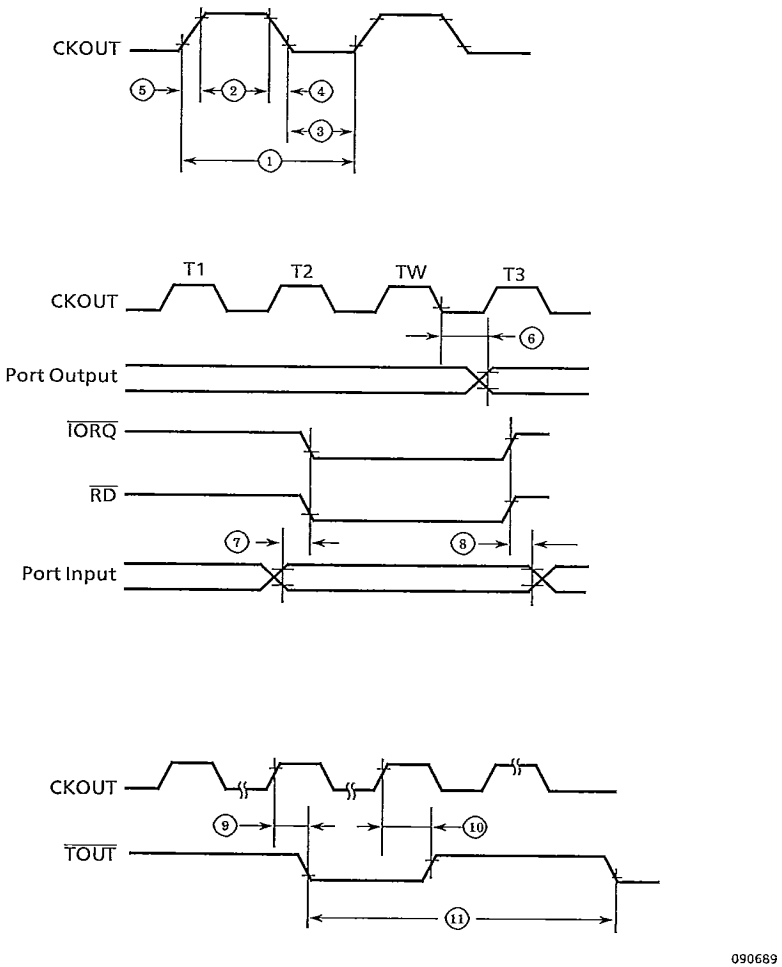

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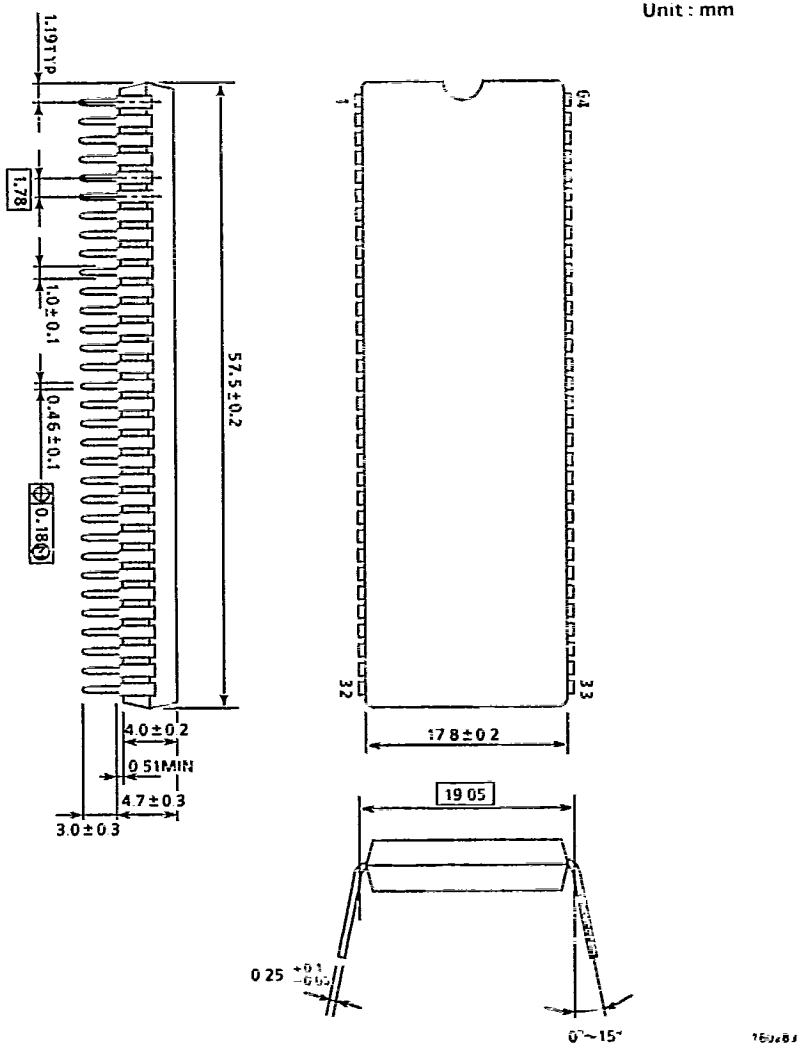
Figure 4.6.1 Input/Output Timing

5. EXTERNAL DIMENSIONS TMPZ84C112AN-6

5.1 DIP Package (SDIP64-P-750)

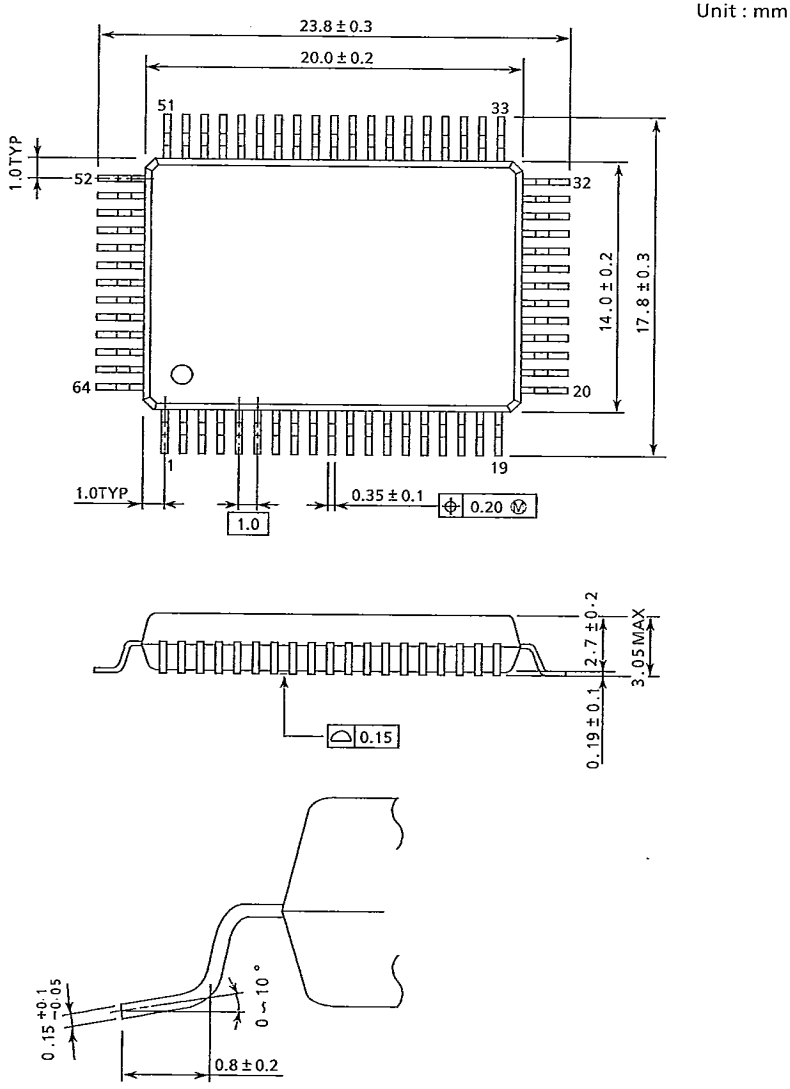
Unit : mm



Note : All the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.64 leads.

5.2 QFP Package (QFP64-P-1420A)

Unit : mm



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