- **1.6 to 2.7 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Hot-Plug Protection**
- **High-Performance 80-Pin BGA Microstar Junior™ Package (GQE)**
- **2.5-V Power Supply for Low Power Operation**
- **Programmable Preemphasis Levels on Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **On-Chip 8-bit/10-bit Encoding/Decoding, Comma Detect**
- **On-Chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **Low Power: < 500 mW**
- **3 V Tolerance on Parallel Data Input Signals**
- **16-Bit Parallel TTL Compatible Data Interface**
- **Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link**
- **Industrial Temperature Range (–40°C to 85°C RCP Package Only)**
- **Loss of Signal (LOS) Detection**
- **Integrated 50-Ω Termination Resistors on RX**

description

The TLK2711 is a member of the *WizardLink* transceiver family of multigigabit transceivers, intended for use in ultrahigh-speed bidirectional point-to-point data transmission systems. The TLK2711 supports an effective serial interface speed of 1.6 Gbps to 2.7 Gbps, providing up to 2.16 Gbps of data bandwidth.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over parallel solutions, as well as scalability for higher data rates in the future.

The TLK2711 performs data conversion parallel-to-serial and serial-to-parallel. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.7 Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (TXCLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8b/10b) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (TXCLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (RXCLK). It then decodes the 20-bit wide data using the 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0-15). The outcome is an effective data payload of 2 Gbps to 2.5 Gbps (16 bits data x the frequency).

The TLK2711 is provided in two packages options: a 80-pin ball grid array MicroStar Junior package and a 64-pin VQFP (RCP) package.

The TLK2711 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, providing the protocol device with a functional self-check of the physical interface.

description (continued)

The TLK2711 has a loss of signal (LOS) detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.

The TLK2711 allows users to implement redundant ports by connecting receive data bus terminals from two TLK2711 devices together. Asserting the LCKREFN to a low state will cause the receive data bus terminals, RXD[0:15], RXCLK, RKLSB, and RKMSB to go to a high-impedance state. This places the device in a transmit-only mode since the receiver is not tracking the data.

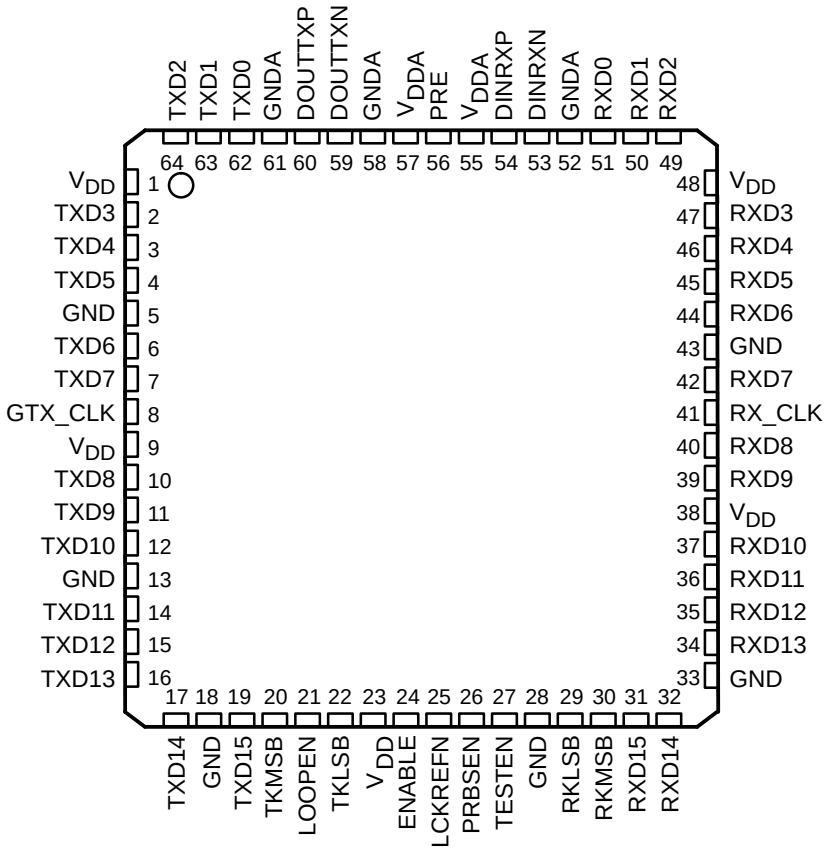
The TLK2711 uses a 2.5-V supply. The I/O section is 3 V compatible. With the 2.5-V supply the chipset is very power efficient, consuming less than 450 mW typically. The TLK2711 is characterized for operation from –40°C to 85°C (RCP only).

The TLK2711 is designed to be hot-plug capable. An on-chip power-on reset circuit holds the RXCLK low and goes to high impedance on the parallel side output signal terminals as well as TXP and TXN during power up.

GQE PACKAGE
(TOP VIEW)

9	8	7	6	5	4	3	2	1	
GND	TXD1	TXP	TXN	PRE	RXP	RXN	RXD1	GND	J
TXD3	TXD2	TXD0	GNDA	VDDA	GNDA	RXD0	RXD2	RXD3	H
TXD5	TXD4	VDD	VDD	VDD	GND	GND	RXD4	RXD5	G
TXD6	TXD7	VDD	VDD	VDD	GND	GND	RXD6	RXD7	F
TXCLK	VDD	VDD	VDD	VDD	GND	GND	RXCLK	RXD8	E
TXD8	TXD9	VDD	VDD	VDD	GND	GND	RXD11	RXD9	D
TXD10	TXD11	VDD	VDD	VDD	GND		RXD12	RXD10	C
TXD12	TXD13	TKMSB	LOOPEN	LCKREFN	TESTEN	RKMSB	RXD14	RXD13	B
GND	TXD14	TXD15	TKLSB	ENABLE	PRBSEN	RKLSB	RXD15	GND	A
9	8	7	6	5	4	3	2	1	

RCP PACKAGE
(TOP VIEW)



block diagram

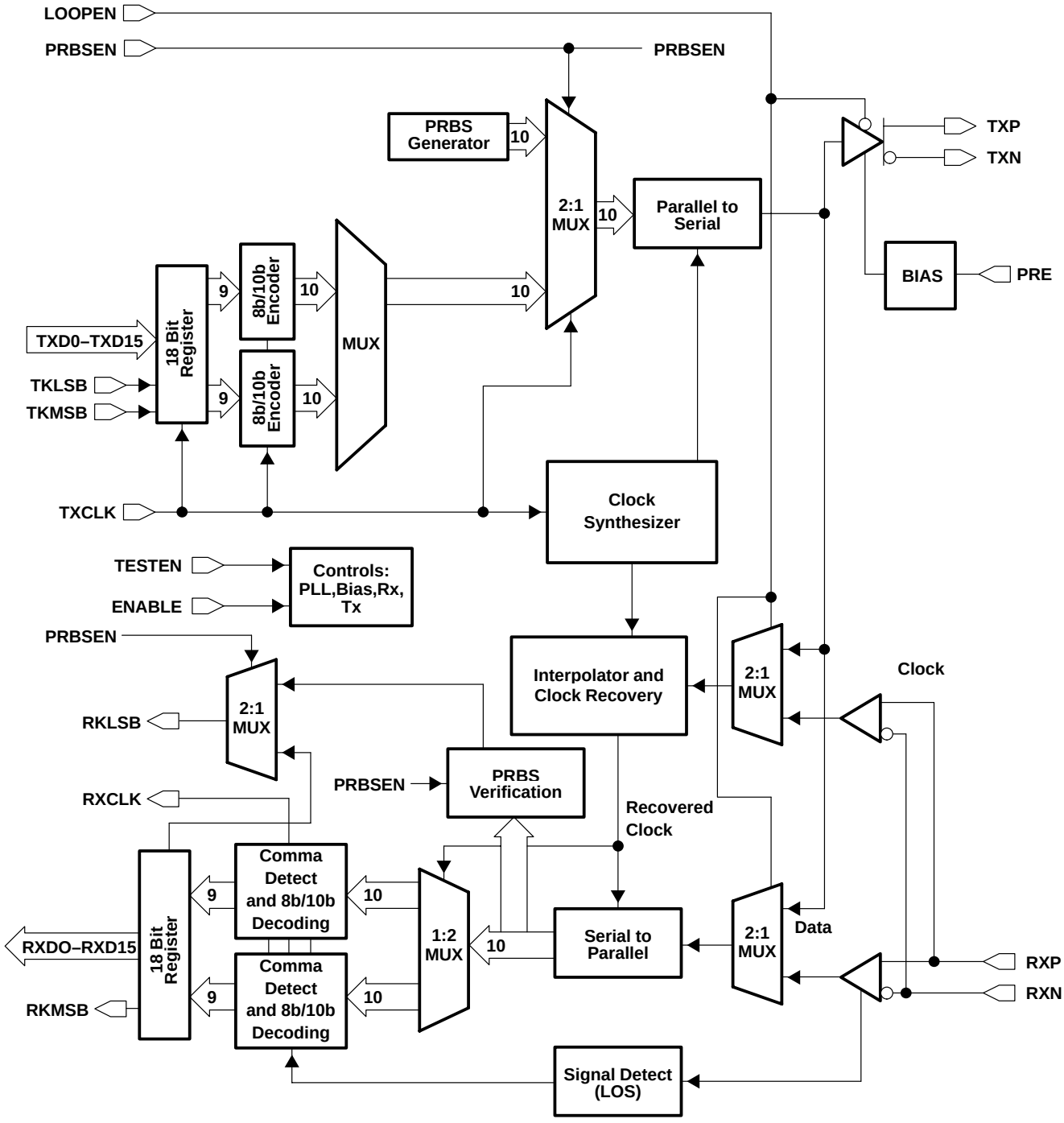


Figure 1. TLK2711 Block Diagram

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	GQE	RCP		
ENABLE	A5	24	I†	Device enable. When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high while the device is in power-down mode, the transceiver goes into power-on reset before beginning normal operation.
GND	A1, J1, D3, E3, F3, G3, C4, D4, E4, F4, G4, A9, J9	5, 13, 18, 28, 33, 43		Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDA	H4, H6	52, 58, 61		Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
LCKREFN	B5	25	I†	Lock to reference. When LCKREFN is low, the receiver clock is frequency locked to TXCLK. This places the device in a transmit only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals, RXD[0:15], RXCLK and RKLSB, RKMSB are in a high-impedance state. When LCKREFN is deasserted high, the receiver is locked to the received data stream.
LOOPEN	B6	21	I‡	Loop enable. When LOOPEN is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRE	J5	56	I‡	Preemphasis control. Selects the amount of preemphasis to be added to the high speed serial output drivers. Left low or unconnected, 5% preemphasis is added. Pulled high, 20% preemphasis is added.
PRBSEN	A4	26	I‡	PRBS test enable. When asserted high results of pseudo random bit stream (PRBS) tests can be monitored on the RKLSB terminal. A high on RKLSB indicates that valid PRBS is being received.
RKLSB	A3	29	O	K-Code indicator/PRBS test results. When RKLSB is asserted high, an 8-bit/10-bit K code was received and is indicated by data bits RXD0–RXD7. When RKLSB is asserted low an 8-bit/10-bit D code is received and is presented on data bits RXD0–RXD7. When PRBSEN is asserted high this pin is used to indicate status of the PRBS test results (high = pass).
RKMSB	B3	30	O	K-code indicator. When RKMSB is asserted high an 8-bit/10-bit K code was received and is indicated by data bits RXD8 –RXD15. When RKMSB is asserted low an 8-bit/10-bit D code was received and is presented on data bits RXD8 – RXD15. If the differential signal on RXN and RXP drops below 200 mV, then RXD [0:15], RKLSB, and RKMSB are all asserted high.
RXCLK RX_CLK	E2	 41	O	Recovered clock. Output clock that is synchronized to RXD [0..9], RKLSB, and RKMSB. RXCLK is the recovered serial data rate clock divided by 20. RXCLK is held low during power-on reset.

† Internal 10k pullup
‡ Internal 10k pulldown

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	GQE	RCP		
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15	H3 J2 H2 H1 G2 G1 F2 F1 E1 D1 C1 D2 C2 B1 B2 A2	51 50 49 47 46 45 44 42 40 39 37 36 35 34 32 31	O	Receive data bus. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RXCLK. The data is valid on the rising edge of RXCLK as shown in Figure 5. These terminals are in high-impedance state during power-on reset.
RXN RXP DINRXN DINRXP	J3 J4	 53 54	I	Serial receive inputs. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
TESTEN	B4	27	I‡	Test mode enable. This terminal should be left unconnected or tied low.
TKLSB	A6	22	I†	K-code generator (LSB). When TKLSB is high, an 8-bit/10-bit K code is transmitted as controlled by data bits TXD0 –TXD7. When TKLSB is low an 8-bit/10-bit D code is transmitted as controlled by data bits TXD0 – TXD7.
TKMSB	B7	20	I†	K-code generator (MSB). When TKMSB is high an 8-bit/10-bit K code is transmitted as controlled by data bits TXD8 –TXD15. When TKMSB is low an 8-bit/10-bit D code is transmitted as controlled by data bits TXD8 – TXD15.
TXCLK GTX_CLK	E9	 8	I	Reference clock. TXCLK is a continuous external input clock that synchronizes the transmitter interface signals TKMSB, TKLSB and TXD [0..15]. The frequency range of TXCLK is 80 MHz to 135 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data TXD [0..15] for serialization.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15	H7 J8 H8 H9 G8 G9 F9 F8 D9 D8 C9 C8 B9 B8 A8 A7	62 63 64 2 3 4 6 7 10 11 12 14 15 16 17 19	I	Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of TXCLK as shown in Figure 2.
TXN TXP DOUTTXN DOUTTXP	J6 J7	 59 60	O	Serial transmit outputs. TXP and TXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the TXCLK value. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset these terminals are high impedance.

† Internal 10k pullup
‡ Internal 10k pulldown

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	GQE	RCP	I/O	
VDD	C5, D5, E5, F5, G5, C6, D6, E6, F6, G6, C7, D7, E7, F7, G7, E8	1, 9, 23, 38, 48		Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	H5	55, 57		Analog power. V_{DDA} provides a supply reference for the high-speed analog circuits, receiver and transmitter

detailed description

transmit interface

The transmitter portion registers valid incoming 16-bit wide data (TXD[0:15]) on the rising edge of the TXCLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (TXCLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (TXD0) first.

transmit data bus

The transmit bus interface accepts 16-bit single-ended TTL parallel data at the TXD[0:15] terminals. Data and K-code control is valid on the rising edge of the TXCLK. The TXCLK is used as the word clock. The data, K-code, and clock signals must be properly aligned as shown in Figure 2. Detailed timing information can be found in the electrical characteristics table**.**

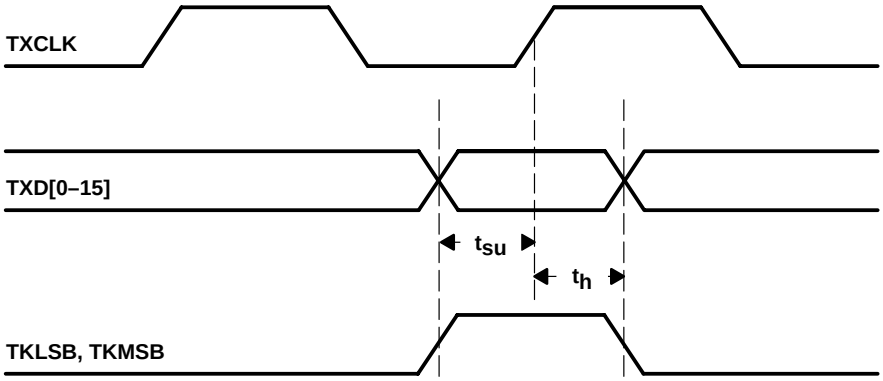


Figure 2. Transmit Timing Waveform

transmission latency

The data transmission latency of the TLK2711 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency $t_{d(Tx\ latency)}$ is 34 bit times; the maximum is 38 bit times. Figure 3 illustrates the timing relationship between the transmit data bus, the TXCLK, and the serial transmit terminals.

detailed description (continued)

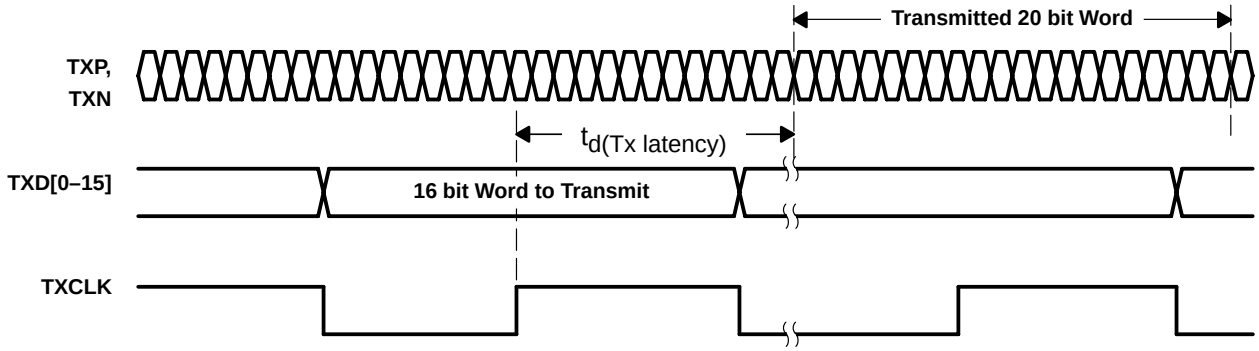


Figure 3. Transmitter Latency

8-bit/10-bit encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK2711 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and gigabit ethernet. This is transparent to the user, as the TLK2711 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the TLK2711 is a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals, the TKMSB and TKLSB.

Table 1. Transmit Data Controls

TKLSB	TKMSB	16 BIT PARALLEL INPUT
0	0	Valid data on TXD(0–7), Valid data TXD(8–15)
0	1	Valid data on TXD(0–7), K code on TXD(8–15)
1	0	K code on TXD(0–7), Valid data on TXD(8–15)
1	1	K code on TXD(0–7), K code on TXD(8–15)

PRBS generator

The TLK2711 has a built-in 2^7-1 PRBS (pseudorandom bit stream) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK2711, or looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the TXCLK input frequency. The LSB (TXD0) is transmitted first.

detailed description (continued)

high-speed data output

The high-speed data output driver consists of a voltage mode logic (VML) differential pair optimized for a 50-Ω impedance environment. The magnitude of the differential pair signal swing is compatible with pseudo emitter coupled logic (PECL) levels when ac-coupled. The line can be directly-coupled or ac-coupled. Refer to Figure 11 and Figure 12 for termination details. The outputs also provide preemphasis to compensate for ac loss when driving a cable or PCB backplane trace over a long distance (see Figure 4). The level of preemphasis is controlled by PRE as shown in Table 2 .

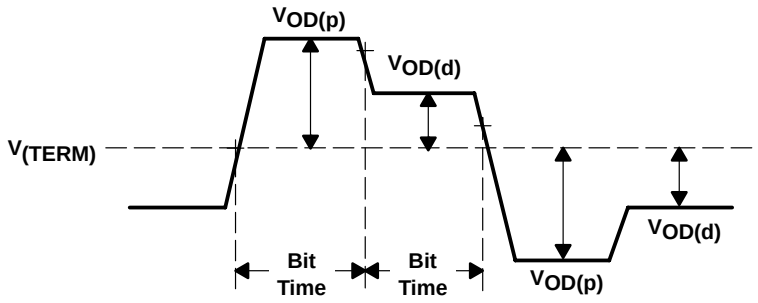


Figure 4. Output Voltage Under Preemphasis (|VTXP–VTXN|)

Table 2. Programmable Preemphasis

PRE	PREEMPHASIS LEVEL(%) $V_{OD(P)}$, $V_{OD(D)}$†
0	5%
1	20%

† $V_{OD(p)}$: Voltage swing when there is a transition in the data stream
$V_{OD(d)}$: Voltage swing when there is no transition in the data stream.

receive interface

The receiver portion of the TLK2711 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded and output on a 16-bit wide parallel bus synchronized to the extracted receive clock. The data is received LSB (RXD0) first.

receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RXD[0:15] terminals. Data is valid on the rising edge of the RXCLK. The RXCLK is used as the recovered word clock. The data, RKLSB, RKMSB, and clock signals are aligned as shown in Figure 5. Detailed timing information can be found in the switching characteristics table**.**

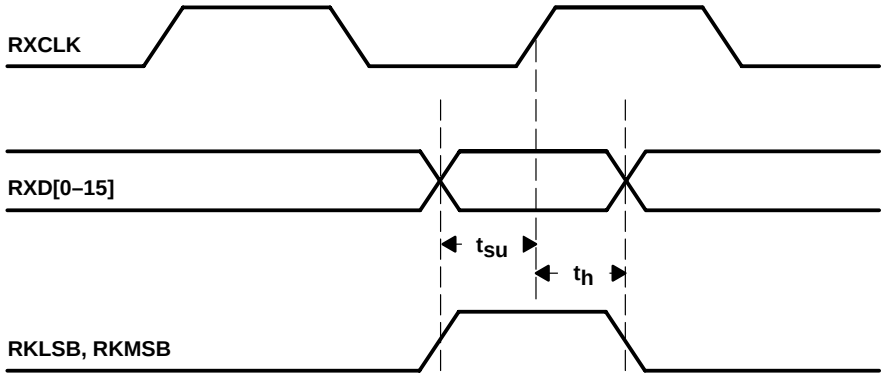


Figure 5. Receive Timing Waveform

detailed description (continued)

data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency $t_{d(Rx\ latency)}$ is 76 bit times; the maximum is 107 bit times. Figure 6 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RXCLK), and the receive data bus.

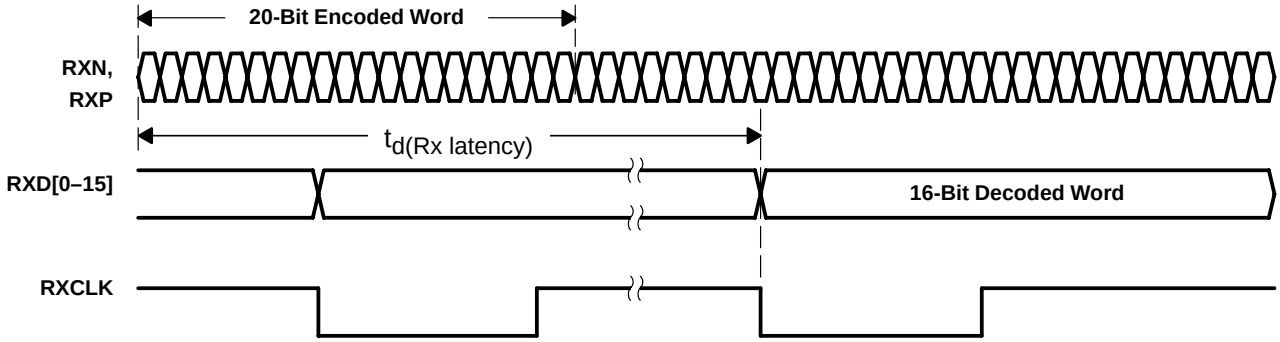


Figure 6. Receiver Latency

serial-to-parallel

Serial data is received on the RXP and RXN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders where the data is then synchronized to the incoming data stream word boundary by detection of the comma 8-bit/10-bit synchronization pattern.

comma detect and 8-bit/10-bit decoding

The TLK2711 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10 bit encoded data (half of the 20-bit received word) back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. Generally this is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1's and 0's that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. The 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma detect circuit on the TLK2711 to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RXCLK) and output valid on the rising edge of the RXCLK.

NOTE:
The TLK2711 only achieves byte alignment on the 0011111 comma.

comma detect and 8-bit/10-bit decoding (continued)

Decoding provides two additional status signals, RKLSB and RKMSB. When RKLSB is asserted , an 8-bit/10-bit K code was received and the specific K code is presented on the data bits RXD0–RXD7; otherwise, an 8-bit/10-bit D code was received. When RKMSB is asserted, an 8-bit/10-bit K code was received and the specific K-code is presented on data bits RXD8–RXD15; otherwise, an 8-bit/10-bit D code was received (see Table 3). The valid K codes the TLK2711 decodes are provided in Table 4. An error detected on either byte, including K codes not in Table 4, causes that byte only to indicate a K0.0 code on the RK×SB and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code. A loss of input signal causes a K31.7 code to be presented on both bytes, where K31.7 is also known to be an invalid 8-bit/10-bit code.

Table 3. Receive Status Signals

RKLSB	RKMSB	DECODED 20 BIT OUTPUT
0	0	Valid data on RXD(0–7), Valid data RXD(8–15)
0	1	Valid data on RXD(0–7), K code on RXD(8–15)
1	0	K code on RXD(0–7), Valid data on RXD(8–15)
1	1	K code on RXD(0–7), K code on RXD(8–15)

Table 4. Valid K Characters

K CHARACTER	RECEIVE DATA BUS (RXD[7–0]) OR (RXD[15–8])
K28.0	000 11100
K28.1†	001 11100
K28.2	010 11100
K28.3	011 11100
K28.4	100 11100
K28.5†	101 11100
K28.6	110 11100
K28.7†	111 11100
K23.7	111 10111
K27.7	111 11011
K29.7	111 11101
K30.7	111 11110

† Should only be present on RXD[7–0] when in running disparity < 0.

power down mode

When the ENABLE pin is pulled low, the TLK2711 goes into power-down mode. In the power-down mode, the serial transmit pins (TXN), the receive data bus pins (RXD[0:15]), and RKLSB goes into a high-impedance state. In the power-down condition, the signal detection circuit draws less than 15 mW. When the TLK2711 is in the power-down mode, the clock signal on the TXCLK terminal must be provided.

loss of signal detection

The TLK2711 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK2711 reports this condition by asserting RKLSB, RKMSB and RXD[0:15] terminals to a high state. As long as the differential signal is above 200 mV in differential magnitude, the LOS circuit does not signal an error condition.

PRBS verification

The TLK2711 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RKLSB terminal low.

detailed description (continued)

reference clock input

The reference clock (TXCLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

operating frequency range

The TLK2711 can operate at a serial data rate from 1.6 Gbps to 2.7 Gbps. To achieve these serial rates, TXCLK must be within 80 MHz to 135 MHz. The TXCLK must be within ±100 PPM of the desired parallel data rate clock.

testability

The TLK2711 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for BIST (built-in self-test).

loopback testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loop-back path. Enabling this terminal causes serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

built-in self-test (BIST)

The TLK2711 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RKLSB terminal.

power-on reset

Upon application of minimum valid power, the TLK2711 generates a power-on reset. During the power-on reset the RXD[0..15], RKLSB, and RKMSB signal terminals go to a high-impedance state. The RXCLK is held low. The length of the power-on reset cycle is dependent upon the TXCLK frequency, but is less than 1 ms.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 V to 3 V
Voltage range at TXD[0..15], ENABLE, TXCLK, TKMSB, TKLSB, LOOPEN, PRBSEN, LCKREFN, PRE . . . . . –0.3 V to 4 V
Voltage range at any other terminal except above . . . . . –0.3 V to V_{DD}+0.3 V
Package power dissipation, P_D . . . . . See Dissipation Rating Table
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Electrostatic discharge . . . . . HBM: 4 kV, CDM:1.5 kV
Characterized free-air operating temperature range, T_A: RCP . . . . . –40°C to 85°C
GQE . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are stated with respect to network ground.

DISSIPATION RATING TABLE‡

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
GQE	37.8	4.56	3.3 W

‡ This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4 layer 3 in × 3 in PCB.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le$25°C POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING
RCP64§	5.25 W	46.58 mW/°C	2.89 W
RCP64¶	3.17 W	23.70 mW/°C	1.74 W
RCP64#	2.01 W	13.19 mW/°C	1.11 W

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
§ 2 oz. Trace and copper pad with solder.
¶ 2 oz. Trace and copper pad without solder.
# Standard JEDEC High-K board.

For more information, refer to TI application note *PowerPAD™ Thermally Enhanced package*, TI literature number SLMA002.

electrical characteristics over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5	2.7	V
Supply current, I_{CC}	Frequency = 1.6 Gbps, PRBS pattern		105		mA
	Frequency = 2.7 Gbps, PRBS pattern		156		
Power dissipation, P_D	Frequency = 1.6 Gbps, PRBS pattern		262		mW
	Frequency = 2.7 Gbps, PRBS pattern		390		mW
	Frequency = 2.7 Gbps, worst case pattern‖			550	mW
Shutdown current	Enable = 0, V_{DDA}, V_{DD} terminals, V_{DD} = MAX		3		mA
PLL startup lock time	V_{DD}, V_{DDC} = 2.3 V		0.1	0.4	ms
Data acquisition time			1024		Bits
Operating free-air temperature, T_A		–40		85	°C

‖ Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

reference clock (TXCLK) timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	Typ–0.01%	80	Typ+0.01%	MHz
Frequency	Maximum data rate	Typ–0.01%	135	Typ+0.01%	MHz
Frequency tolerance		–100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak-to-peak			40	ps

TTL input electrical characteristics over recommended operating conditions (unless otherwise noted), TTL signals: TXDO–TXD15, TXCLK, LOOPEN, LCKREFN, ENABLE, PRBS_EN, TKLSB, TKMSB, PRE

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 7	1.7		3.6	V
V_{IL}	Low-level input voltage	See Figure 7			0.80	V
I_{IH}	Input high current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = MAX, V_{IN} = 0.4 V	–40			µA
C_I	Receiver input capacitance				4	pF
t_r	Rise time, TXCLK, TKMSB, TKLSB, TXD[0..15]	0.7 V to 1.9 V, C = 5 pF, SeeFigure 7		1		ns
t_f	Fall time, TXCLK, TKMSB, TKLSB, TXD[0..15]	1.9 V to 0.7 V, C = 5 pF, See Figure 7		1		ns
t_{su}	TXD[0..15], TKMSB, TKLSB setup to ↑ TXCLK	See Figure 7	1.5			ns
t_h	TXD, TKMSB, TKLSB hold to ↑ TXCLK	See Figure 7	0.4			ns

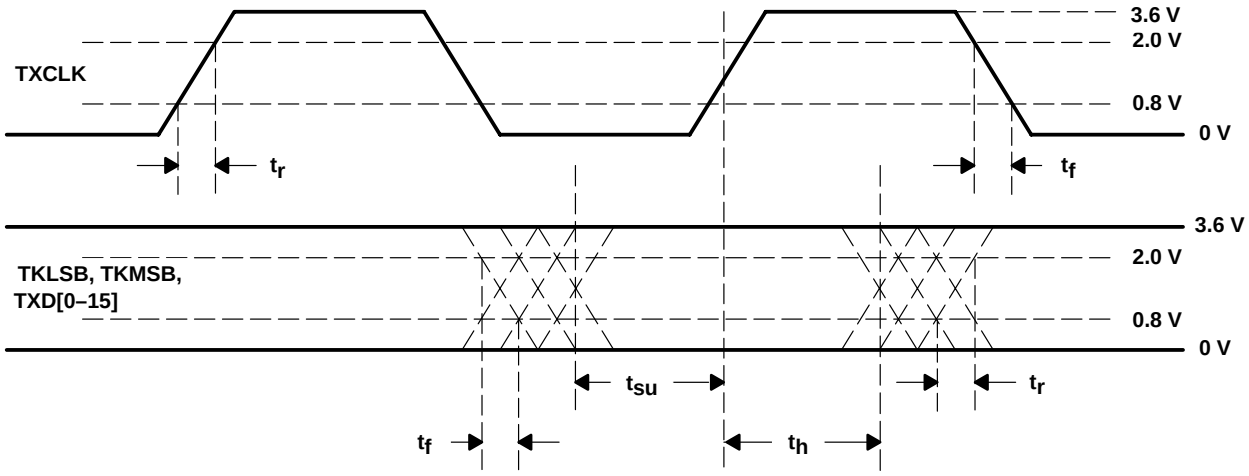


Figure 7. TTL Data Input Valid Levels for AC Measurements

TTL output switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, V_{DD} = MIN	2.10	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	GND	0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15]	0.8 V to 2 V, C = 5 pF, See Figure 8	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of RXCLK, RKLSB, RKMSB, RXD[0..15]	0.8 V to 2 V, C = 5 pF, See Figure 8	0.5			V/ns
t_{su}	RXD[0..15], RKMSB, RKLSB setup to ↑ RXCLK	50% voltage swing, TXCLK = 80 MHz, Figure 8	3			ns
		50% voltage swing, TXCLK = 135 MHz, See Figure 8	2.5			ns
t_h	RXD[0..15], RKMSB, RKLSB hold to ↑ RXCLK	50% voltage swing, TXCLK = 80 MHz, See Figure 8	3			ns
		50% voltage swing, TXCLK = 135 MHz, See Figure 8	2.5			ns

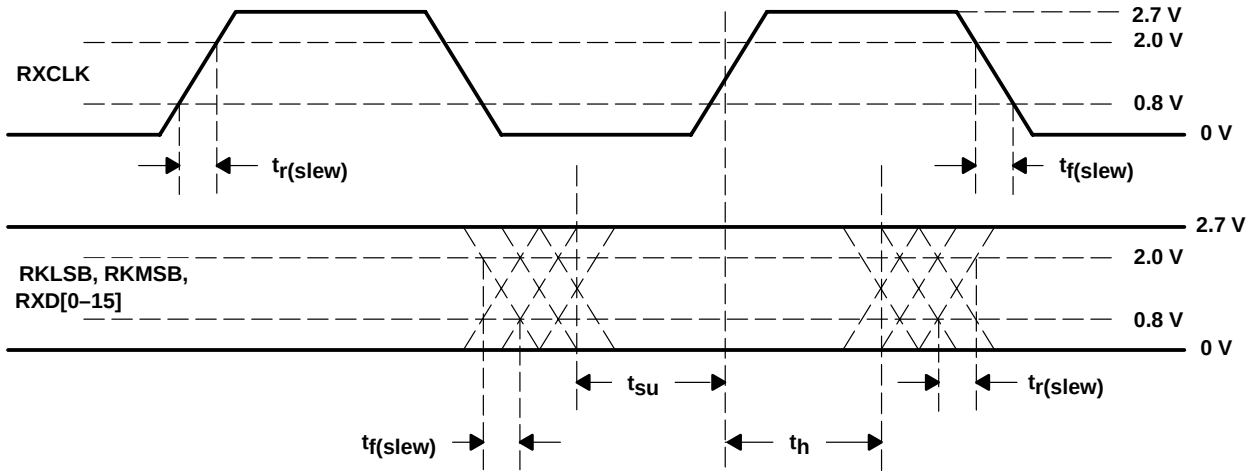


Figure 8. TTL Data Output Valid Levels for AC Measurements

transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p)}$	Preemphasis V_{OD}, direct, $V_{OD(p)}$ = |VTXP – VTXN|	Rt = 50 Ω, PREM = high, dc-coupled, See Figure 9	655	725	795	mV
		Rt = 50 Ω, PREM = low, dc-coupled, See Figure 9	590	650	710	
$V_{OD(pp\_p)}$	Differential, peak-to-peak output voltage with preemphasis	Rt = 50 Ω, PREM = high, dc-coupled, See Figure 9	1310	1450	1590	mV_{p-p}
		Rt = 50 Ω, PREM = low, dc-coupled, See Figure 9	1180	1300	1420	
$V_{OD(d)}$	Deemphais output voltage, |VTXP – VTXN|	Rt = 50 Ω, DC-coupled, See Figure 9	540	600	660	mV
$V_{OD(pp\_d)}$	Differential, peak-to-peak output voltage with deemphasis	Rt = 50 Ω, dc-coupled, See Figure 9	1080	1200	1320	mV_{p-p}
$V_{(cmt)}$	Transmit common mode voltage range, (VTXP + VTXN)/2	Rt = 50 Ω, See Figure 9	1000	1250	1400	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|		200		1600	mV
$V_{(cmr)}$	Receiver common mode voltage range, (VRXP + VRXN)/2		1000	1250	2250	mV
I_{lkg}	Receiver input leakage current		–10		10	µA
C_i	Receiver input capacitance				2	pF
	Serial data total jitter (peak-to-peak)	Differential output jitter at 2.7 Gbps, Random + deterministic, PRBS pattern		0.20		UI†
		Differential output jitter at 1.5 Gbps, Random + deterministic, PRBS pattern		0.16		UI†
t_t, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		150		ps
	Jitter tolerance	Differential input jitter, random + determinisitc, PRBS pattern at zero crossing	0.60			UI
$t_{d(Tx\ latency)}$	Tx latency	See Figure 3	34		38	bits
$t_{d(Rx\ latency)}$	Rx latency	See Figure 6	76		107	bits

† UI is the time interval of one serialized bit.

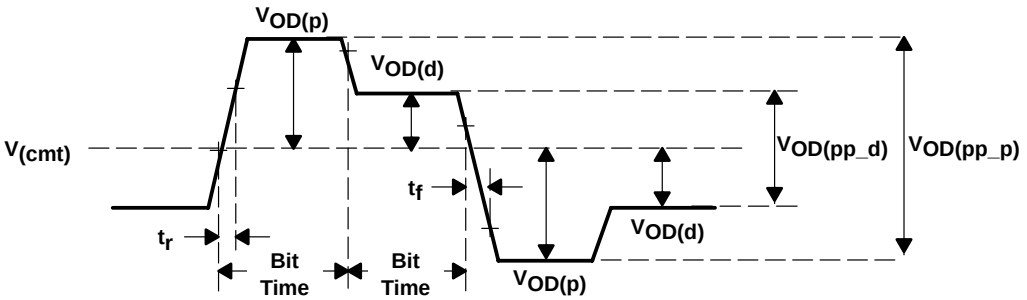


Figure 9. Differential and Common-Mode Output Voltage Definitions

THERMAL INFORMATION

thermal characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		21.47		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.20		
		Board-mounted, no air flow, JEDEC test board		75.88		
$R_{\theta JC}$	Junction-to-case thermal resistance	Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land		0.38		°C/W
		Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land		0.38		
		Board-mounted, no air flow, JEDEC test board		7.8		

APPLICATION INFORMATION

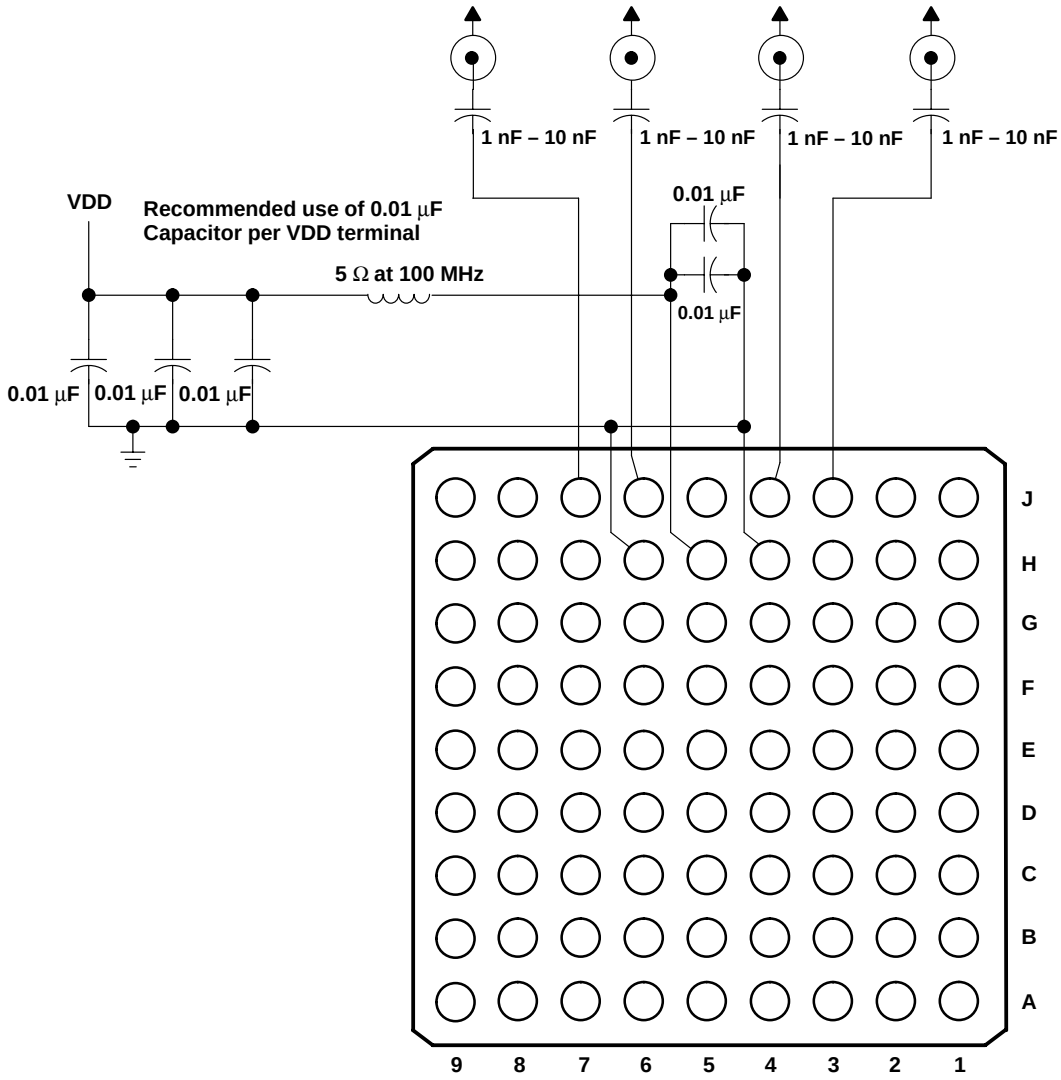


Figure 10. External Component Interconnection

APPLICATION INFORMATION

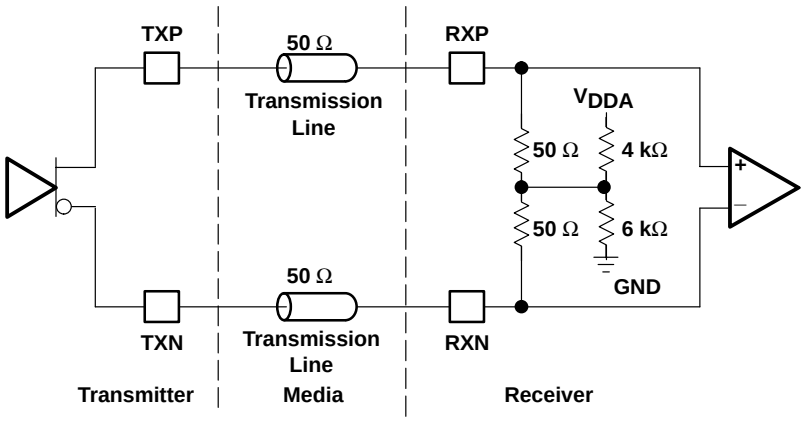


Figure 11. High-Speed I/O Directly-Coupled Mode

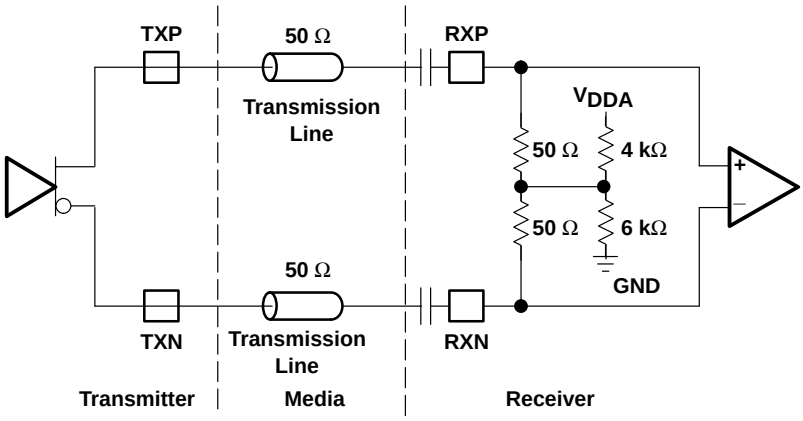
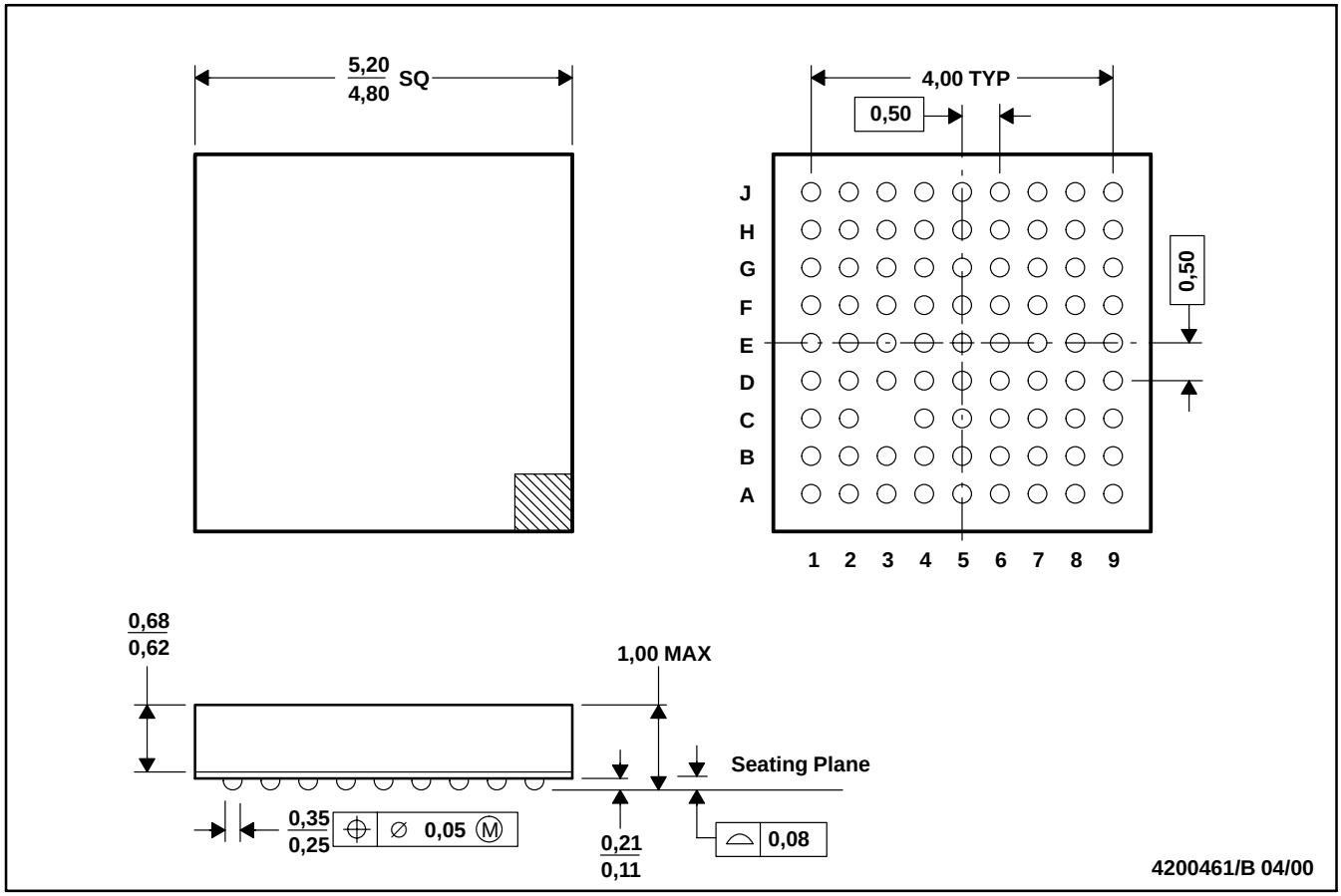


Figure 12. High-Speed I/O AC-Coupled Mode

MECHANICAL DATA

GQE (S-PBGA-N80) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration

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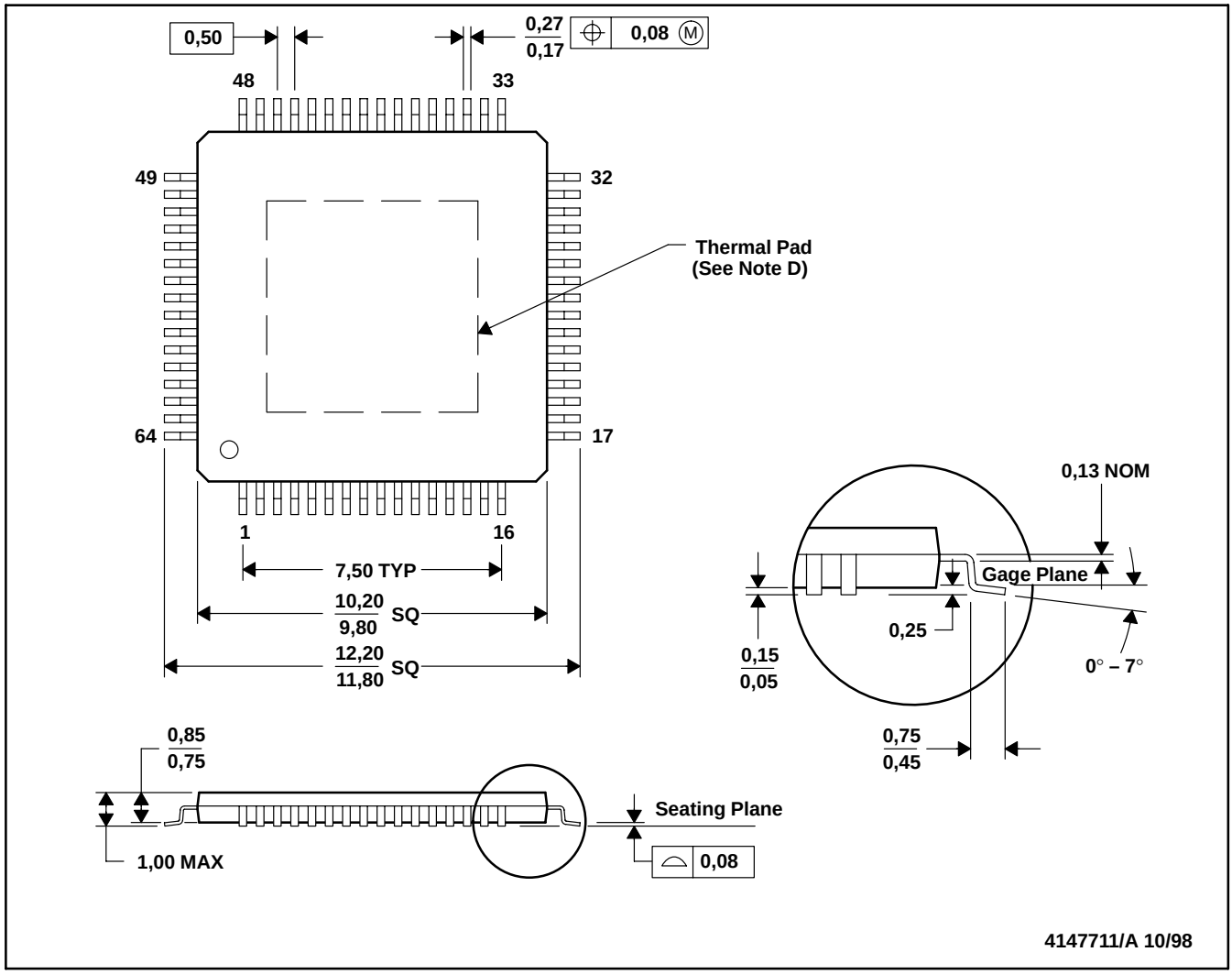
MECHANICAL DATA

RCP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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