DATA SHEET

TDA8792
3.3 V, 25 MHz 8-bit analog-to-digital converter (ADC)

Product specification
Supersedes data of 1995 Apr 26
File under Integrated Circuits, IC02

1996 Feb 21

Philips Semiconductors

PHILIPS

3.3 V, 25 MHz 8-bit analog-to-digital converter (ADC)

TDA8792

FEATURES

- 8-bit resolution
- Sampling rate up to 25 MHz
- 30 MHz input signal bandwidth (full scale)
- High signal-to-noise ratio over a large analog input frequency range (7.3 effective bits at 4.43 MHz full-scale input at f_{clk} = 25 MHz)
- CMOS compatible digital inputs
- External reference voltage regulator
- Power dissipation only 53 mW (typical)
- Standby mode (only 1.2 mW typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

Analog-to-digital conversion for:

- General purpose
- Hand-held equipment
- Mobile telecommunication
- Instrumentation
- Video.

GENERAL DESCRIPTION

The TDA8792 is a 8-bit analog-to-digital converter (ADC) for low-voltage, portable applications. It operates at 3.3 V and converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 25 MHz. The output data is valid after a delay of 6 clock cycles.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.85	3.3	3.6	V
V_{DDD}	digital supply voltage		2.70	3.3	3.6	V
V_{DDO}	output stages supply voltage		2.5	3.3	3.6	V
I_{DDA}	analog supply current		–	12	20	mA
I_{DDD}	digital supply current		–	3	6	mA
I_{DDO}	output stages supply current	f_{clk} = 25 MHz; C_L = 15 pF; ramp input	–	1	2	mA
INL	integral non-linearity	f_{clk} = 25 MHz; ramp input	–	±0.4	±0.8	LSB
DNL	differential non-linearity	f_{clk} = 25 MHz; ramp input	–	±0.3	±0.75	LSB
$f_{clk(max)}$	maximum clock frequency		25	–	–	MHz
P_{tot}	total power dissipation	f_{clk} = 25 MHz; C_L = 15 pF; ramp input	–	53	100	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8792M	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

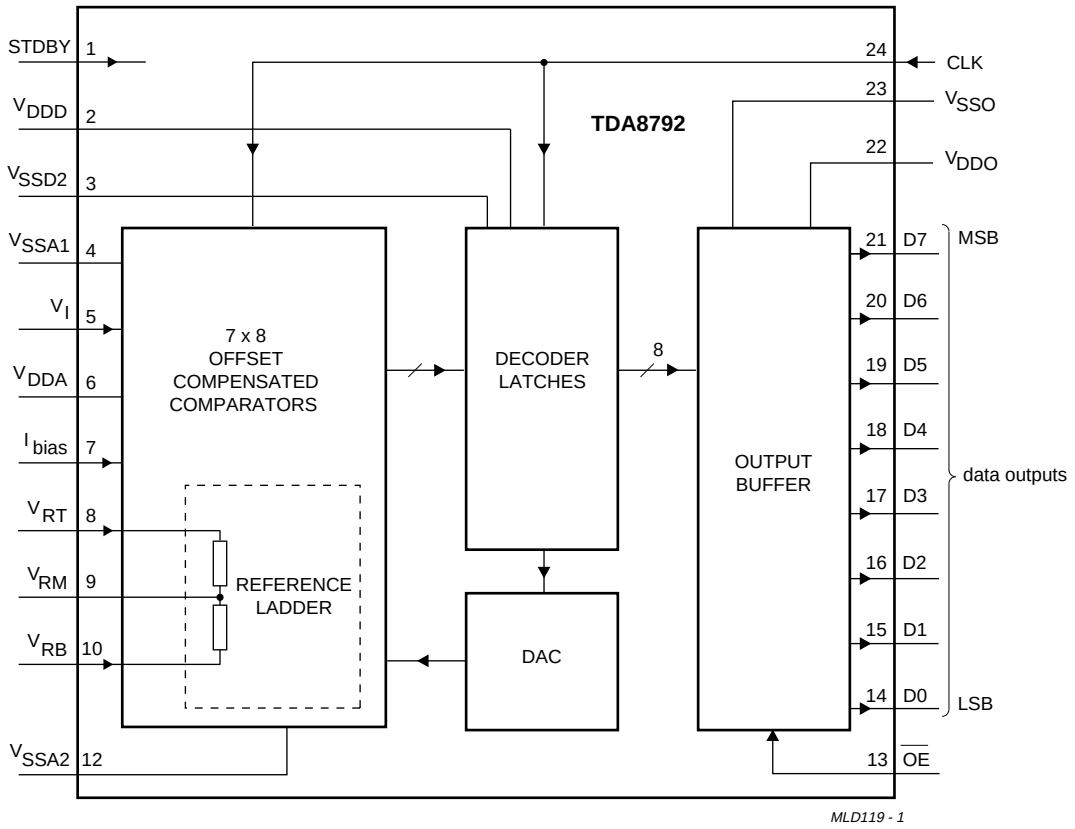


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
STDBY	1	standby input
V_{DDD}	2	digital supply voltage (+3.3 V)
V_{SSD2}	3	digital ground 2
V_{SSA1}	4	analog ground 1
V_I	5	analog input voltage
V_{DDA}	6	analog supply voltage (+3.3 V)
I_{bias}	7	bias current input
V_{RT}	8	reference voltage TOP input
V_{RM}	9	reference voltage MIDDLE
V_{RB}	10	reference voltage BOTTOM input
n.c.	11	not connected
V_{SSA2}	12	analog ground 2
$\overline{OE}$	13	output enable input (CMOS level input, active LOW)
D0	14	data output; bit 0 (LSB)
D1	15	data output; bit 1
D2	16	data output; bit 2
D3	17	data output; bit 3
D4	18	data output; bit 4
D5	19	data output; bit 5
D6	20	data output; bit 6
D7	21	data output; bit 7 (MSB)
V_{DDO}	22	positive supply voltage for output stage (+3.3 V)
V_{SSO}	23	output ground
CLK	24	clock input

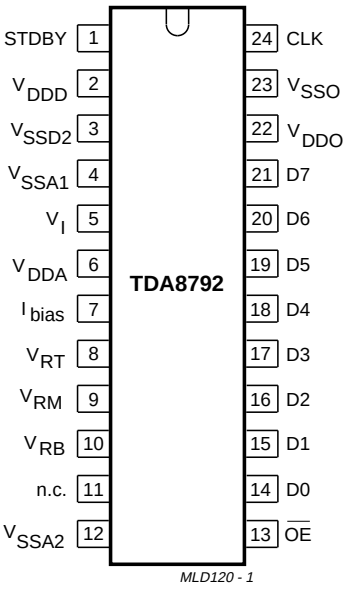


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	–0.5	+5.0	V
V_{DDD}	digital supply voltage	note 1	–0.5	+5.0	V
V_{DDO}	output stages supply voltage	note 1	–0.5	+5.0	V
ΔV_{DD1}	supply voltage differences between $\Delta V_{DD1} = V_{DDA} - V_{DDD}$		–0.3	+0.3	V
ΔV_{DD2}	supply voltage differences between $\Delta V_{DD2} = V_{DDD} - V_{DDO}$		–1.0	+1.0	V
ΔV_{DD3}	supply voltage differences between $\Delta V_{DD3} = V_{DDA} - V_{DDO}$		–1.0	+1.0	V
V_I	input voltage	referenced to V_{SSA}	–0.5	+5.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to V_{SSD}	–	V_{DDD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
T_j	junction temperature		–	+125	°C

Note

1. The supply voltages V_{DDA}, V_{DDD} and V_{DDO} may have any value between –0.5 V and +5.0 V provided that the differences ΔV_{DD1}, ΔV_{DD2} and ΔV_{DD3} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	119	K/W

CHARACTERISTICS

V_{DDA} = V_6 to $V_{4,12}$ = 2.85 to 3.6 V; V_{DDD} = V_2 to V_3 and V_1 = 2.7 to 3.6 V; V_{DDO} = V_{22} to V_{23} = 2.5 to 3.6 V; V_{SSA}, V_{SSD} and V_{SSO} shorted together; V_{DDA} to V_{DDD} = –0.15 to +0.15 V; f_{clk} = 25 MHz; 50% duty factor; V_{IL} = 0 V; V_{IH} = V_{DDD}; C_L = 15 pF; T_{amb} = 0 to +70 °C; typical values measured at V_{DDA} = V_{DDD} = V_{DDO} = 3.3 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		2.85	3.3	3.6	V
V_{DDD}	digital supply voltage		2.7	3.3	3.6	V
V_{DDO}	output stages supply voltage		2.5	3.3	3.6	V
I_{DDA}	analog supply current		–	12	20	mA
I_{DDD}	digital supply current		–	3	6	mA
I_{DDO}	output stages supply current	C_L = 15 pF; ramp input	–	1	2	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO V_{SSD}); note 1						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–10	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	10	µA
C_I	input capacitance		–	10	–	pF
INPUTS $\overline{OE}$ AND STDBY (REFERENCED TO V_{SSD}); see Tables 2 and 3						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
I_{IL}	LOW level input current	V_{IL} = 0.4 V	–10	–	–	µA
I_{IH}	HIGH level input current	V_{IH} = 2.7 V	–	–	+10	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO V_{SSA})						
I_{IL}	LOW level input current	V_I = 0 V	–20	–	–	µA
I_{IH}	HIGH level input current	V_I = 1.5 V	–	–	+20	µA
Z_I	input impedance	f_i = 4.43 MHz	–	35	–	kΩ
C_I	input capacitance	f_i = 4.43 MHz	–	5	–	pF
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		0	–	0.15	V
V_{RT}	reference voltage TOP		1.4	–	1.6	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.25	1.5	1.6	V
I_{ref}	reference current		–	1.3	–	mA
R_{LAD}	resistor ladder		–	1250	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1	–	Ω/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO V_{SSO})						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –1 mA	V_{DDO} – 0.4	–	V_{DDO}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{DDO}	–10	–	+10	μA
Switching characteristics						
CLOCK INPUT CLK (V_{DDA} = 3.15 TO 3.45 V; V_{DDD} = 3.15 TO 3.45 V); see Fig.3 and note 1						
$f_{clk(max)}$	maximum clock frequency		25	–	–	MHz
$f_{clk(min)}$	minimum clock frequency		0.5	–	–	MHz
t_{CPH}	clock pulse width HIGH		16	–	–	ns
t_{CPL}	clock pulse width LOW		16	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	ramp input	–	±0.4	±0.8	LSB
DNL	differential non-linearity	ramp input	–	±0.3	±0.75	LSB
BANDWIDTH (V_{DDA} = 3.15 TO 3.45 V; V_{DDD} = 3.15 TO 3.45 V); T_{AMB} = 25 °C						
B	analog bandwidth	full-scale sine wave; note 2	20	30	–	MHz
		small signal at mid-scale; V_i = ±10 LSB at code 128; note 2	–	35	–	MHz
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.5; note 3	–	8	12	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.5; note 3	–	8	12	ns
HARMONICS						
h_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
h_{all}	harmonics (full scale); all components	f_i = 4.43 MHz				
	second harmonics		–	–61	–	dB
	third harmonics		–	–61	–	dB
THD	total harmonic distortion	f_i = 4.43 MHz	–	–58	–	dB
SIGNAL-TO-NOISE RATIO; see Figs 6 and 11; note 4						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 25 MHz; f_i = 4.43 MHz	–	46	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS; see Figs 6 and 11; note 4						
EB	effective bits	f_{clk} = 25 MHz				
		f_i = 2.0 MHz	–	7.4	–	bits
		f_i = 4.43 MHz	–	7.3	–	bits
		f_i = 7.5 MHz	–	7.2	–	bits
		f_i = 10 MHz	–	7.0	–	bits
DIFFERENTIAL GAIN; see note 5						
G_{diff}	differential gain	f_{clk} = 25 MHz; PAL modulated ramp	–	1.5	–	%
DIFFERENTIAL PHASE; see note 5						
φ_{diff}	differential phase	f_{clk} = 25 MHz; PAL modulated ramp	–	0.5	–	deg
Timing (f_{clk} = 25 MHz); see Fig.3 and note 6						
t_{ds}	sampling delay time		–	–	2	ns
t_h	output hold time		6	–	–	ns
t_d	output delay time		8	13	25	ns
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	17	28	ns
t_{dZL}	enable LOW		–	22	30	ns
t_{dHZ}	disable HIGH		–	20	28	ns
t_{dLZ}	disable LOW		–	22	30	ns
Standby mode output delay times						
t_{dSTBLH}	standby (LOW-to-HIGH transition)		–	–	200	ns
t_{dSTBHL}	start-up (HIGH-to-LOW transition)		–	–	note 7	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. The analog bandwidth is defined as the maximum full-scale input sine wave frequency which can be applied to the device. No glitches greater than 8 LSBs are observed in the reconstructed signal neither is there any significant attenuation.
3. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB $\times$ 6.02 + 1.76 dB.
5. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
6. Output data acquisition: the output data is available after the maximum delay time of t_d. In the event of 25 MHz clock operation, the hardware design must be taken into account the t_d and t_h limits with respect to the input characteristics of the acquisition circuit.
7. Maximum value standby mode start-up output delay time (HIGH-to-LOW transition): $100 + \frac{7000}{f_{clk}(MHz)}$.

Table 1 Output coding and input voltage (typical values; referenced to V_{SSA})

STEP	$V_{I(p-p)}$ (V)	BINARY OUTPUT BITS							
		D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	.	1	1	1	1	1	1	1	0
255	1.5	1	1	1	1	1	1	1	1
Overflow	>1.5	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{OE}$	D7 TO D0
1	high impedance
0	active; binary

Table 3 Standby selection

STDBY	D7 TO D0	$I_{DDA} + I_{DDD}$ (typ.)
1	LOW	0.4 mA
0	active	15 mA

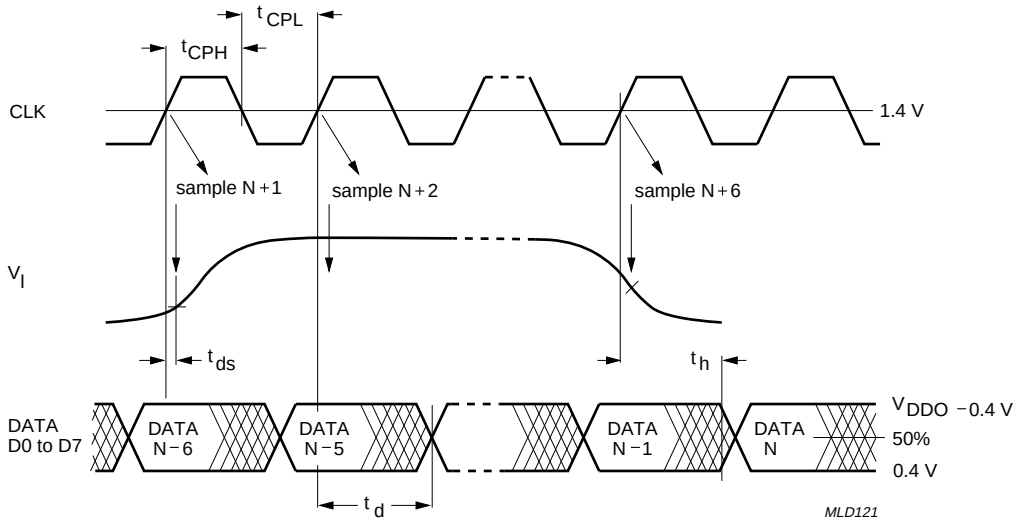
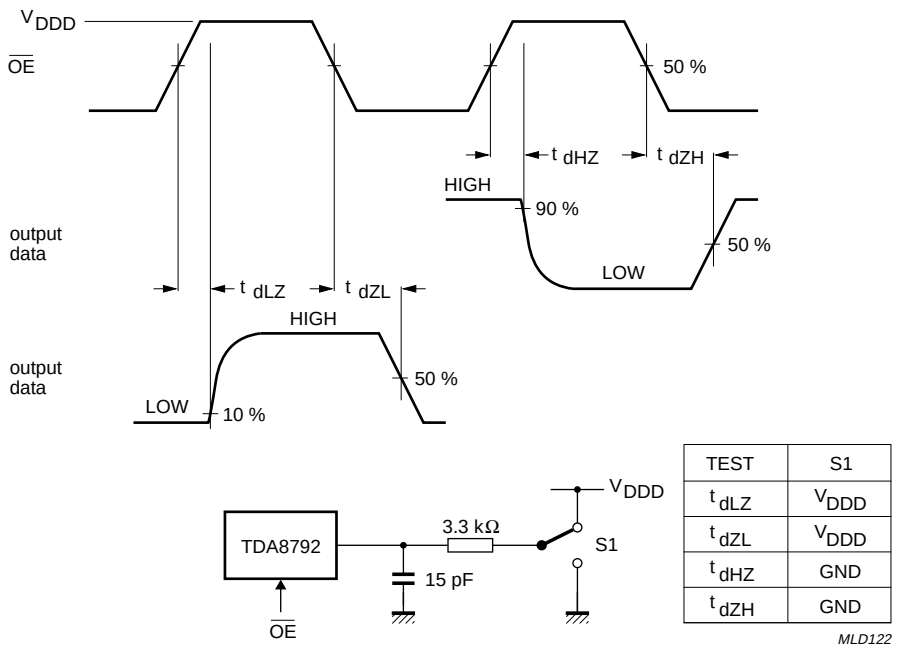


Fig.3 Timing diagram.



TEST	S1
t_{dLZ}	V_{DDD}
t_{dZL}	V_{DDD}
t_{dHZ}	GND
t_{dZH}	GND

f_{OE} = 100 kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

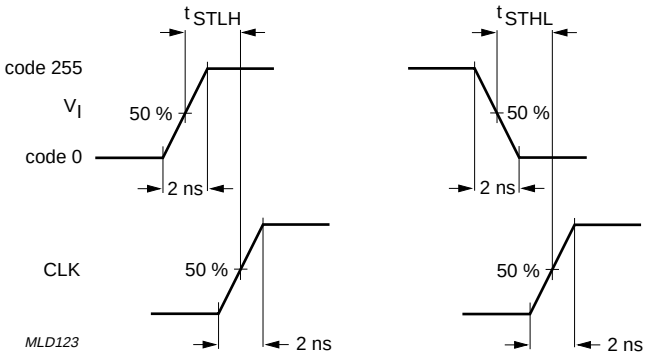
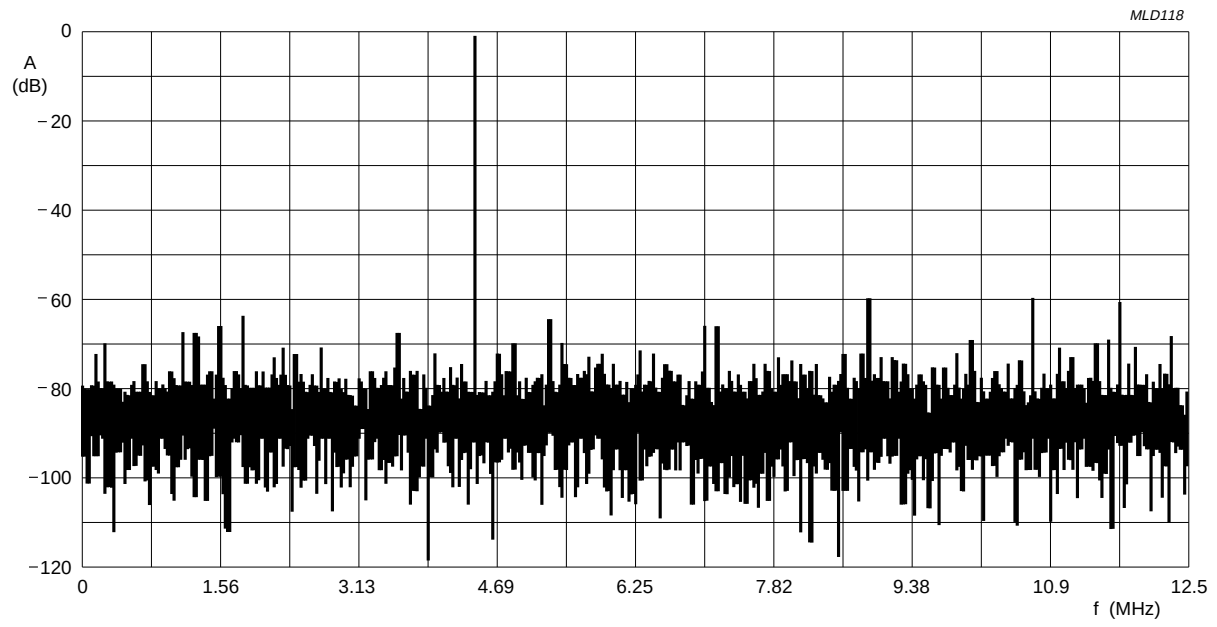


Fig.5 Analog input settling-time diagram.



Effective bits: 7.42; THD = –57.27 dB;
Harmonic levels (dB): 2nd = –60.76; 3rd = –60.96; 4th = –76.17; 5th = –80.63; 6th = –66.96.

Fig.6 Typical Fast Fourier Transform (f_{clk} = 25 MHz; f_i = 4.43 MHz).

INTERNAL PIN CONFIGURATIONS

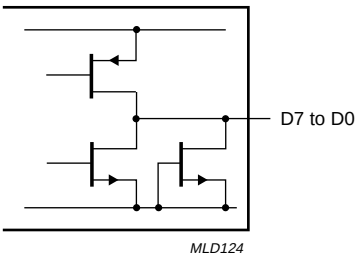


Fig.7 Digital data outputs.

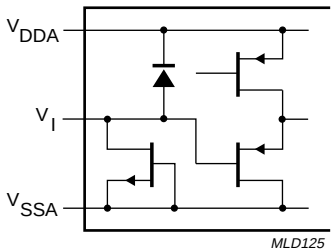


Fig.8 Analog inputs.

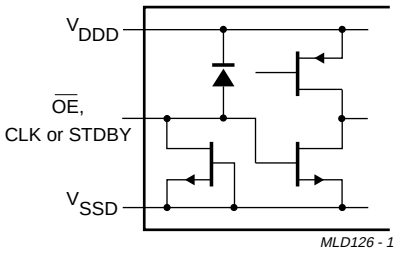


Fig.9 Digital inputs.

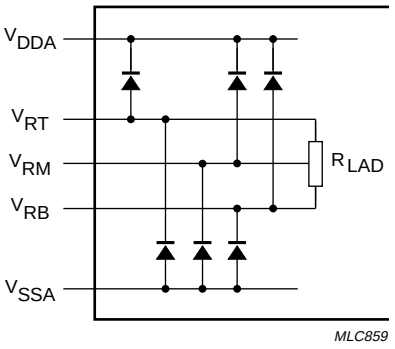


Fig.10 V_{RB}, V_{RM} and V_{RT}.

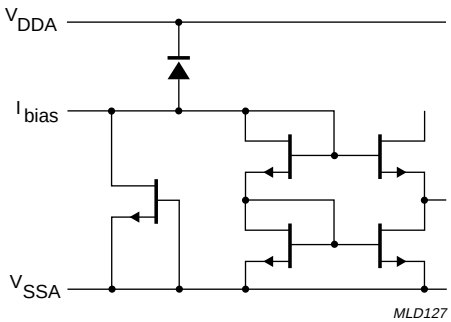
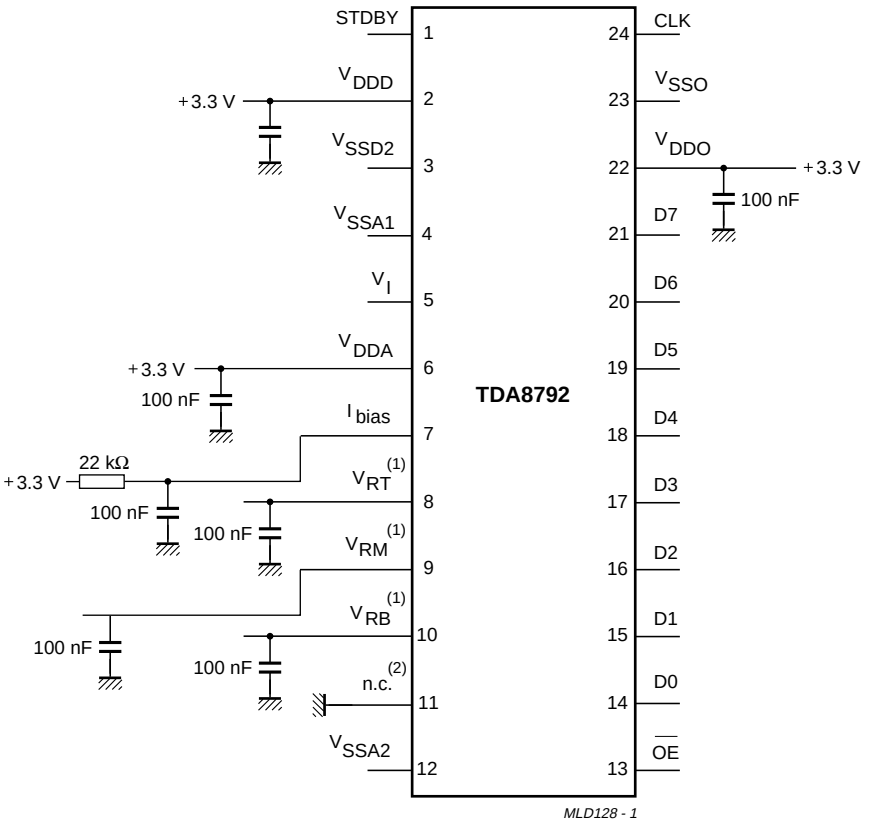


Fig.11 Bias current input.

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. The reference ladder voltages can also be derived from a well regulated V_{DDA} supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale, V_{RM} must be decoupled and connected to analog input signal (pin 5) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g. R = 5 kΩ and C = 100 nF).

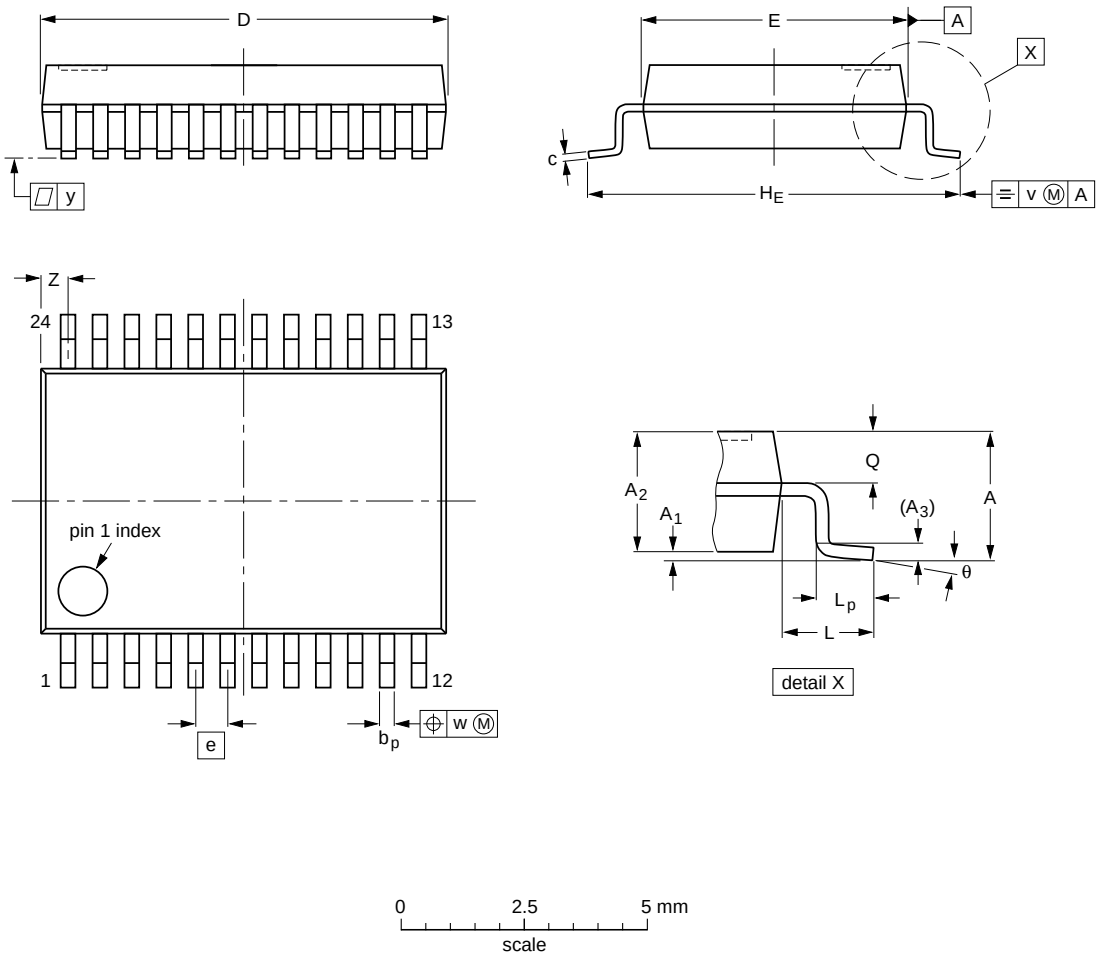
(1) V_{RB}, V_{RM} and V_{RT} are decoupled to V_{SSA}.

(2) Pin 11 should be connected to V_{SSA} in order to prevent noise influence.

Fig.12 Application diagram.

PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SOLDERING SSOP

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40-2783749, Fax. (31)40-2788399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil,
P.O. Box 7383 (01064-970),
Tel. (011)821-2333, Fax. (011)829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO,
Tel. (02)773 816, Fax. (02)777 6730

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. (852)2319 7888, Fax. (852)2319 7700

Colombia: IPRELENSO LTDA, Carrera 21 No. 56-17,
77621 BOGOTA, Tel. (571)249 7624/(571)217 4609,
Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300
COPENHAGEN S, Tel. (45)32 88 26 36, Fax. (45)31 57 19 49

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (358)0-615 800, Fax. (358)0-61580 920

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 51 40, 20035 HAMBURG,
Tel. (040)23 53 60, Fax. (040)23 53 63 00

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01)4894 339/4894 911, Fax. (01)4814 240

India: Philips INDIA Ltd, Shivsagar Estate, A Block,
Dr. Annie Besant Rd. Worli, Bombay 400 018
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950,
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)7640 000, Fax. (01)7640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l.,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5130, Fax. (03)3740 5077

Korea: Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)709-1412, Fax. (02)709-1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905,
Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. (040)2783749, Fax. (040)2788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49,
Fax. (021)577035/5874546

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (63) 2 816 6380, Fax. (63) 2 817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)4163160/4163333, Fax. (01)4163174/4163366

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430, Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (0)8-632 2000, Fax. (0)8-632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West
Road, Sec. 1. Taipeh, Taiwan ROC, P.O. Box 22978,
TAIPEI 100, Tel. (886) 2 382 4443, Fax. (886) 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
Bangkok 10260, THAILAND,
Tel. (66) 2 745-4090, Fax. (66) 2 398-0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 27 70, Fax. (0212)282 67 07

Ukraine: Philips UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. 380-44-4760297, Fax. 380-44-4766991

United Kingdom: Philips Semiconductors LTD.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX,
Tel. (0181)730-5000, Fax. (0181)754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

Internet: http://www.semiconductors.philips.com/ps/

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-p,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-2724825

Printed in The Netherlands

537021/1100/02/pp20 Date of release: 1996 Feb 21

Document order number: 9397 750 00675

Let's make things better.

Philips Semiconductors

PHILIPS