

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2141 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 1.1 \, \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 3.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 1150 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolated TO-220 (MP-45F) Package

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

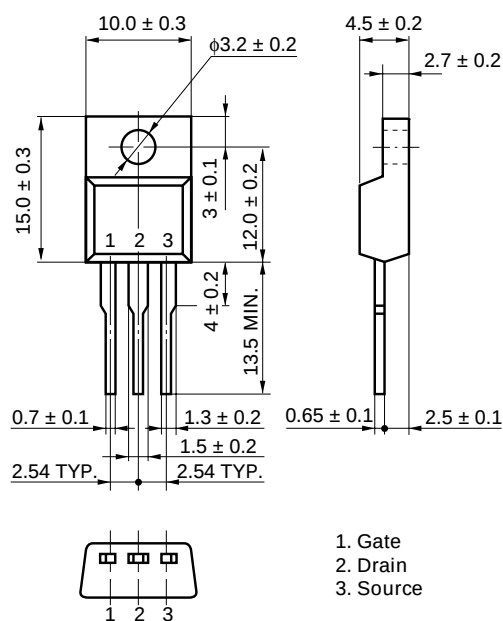
Drain to Source Voltage	V_{DSS}	600	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	I_D (DC)	± 6.0	A
Drain Current (pulse)	I_D (pulse)*	± 24	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	2.0	W
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Single Avalanche Current	I_{AS}^{**}	6.0	A
Single Avalanche Energy	E_{AS}^{**}	12	mJ

*PW $\leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

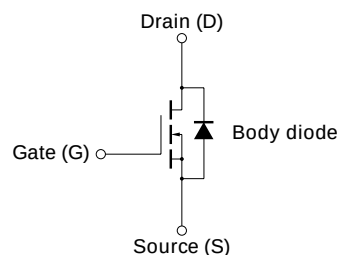
****Starting $T_{ch} = 25\text{ }^{\circ}\text{C}$, $R_G = 25\text{ }\Omega$, $V_{GS} = 20\text{ V} \rightarrow 0$**

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DIMENSIONS



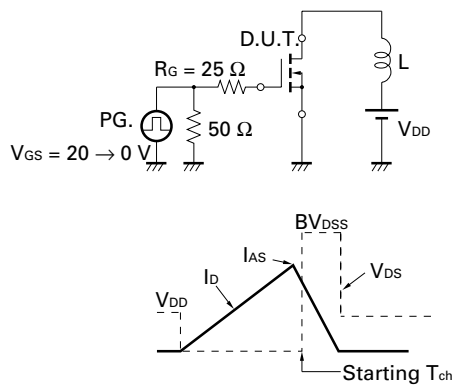
ISOLATED TO-220 (MP-45F)



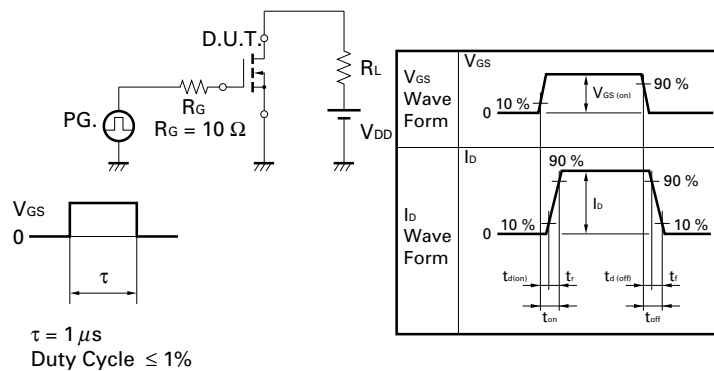
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.8	1.1	Ω	V _{GS} = 10 V, I _D = 3.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	2.0			S	V _{DS} = 10 V, I _D = 3.0 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 600V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		1150		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		260		pF	
Reverse Transfer Capacitance	C _{rss}		60		pF	
Turn-On Delay Time	t _{d(on)}		15		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 3.0 A, R _G = 10 Ω R _L = 37.5 Ω
Rise Time	t _r		15		ns	
Turn-Off Delay Time	t _{d(off)}		75		ns	
Fall Time	t _f		13		ns	
Total Gate Charge	Q _G		40		nC	V _{GS} = 10 V I _D = 6.0 A V _{DD} = 480 V
Gate to Source Charge	Q _{GS}		6.0		nC	
Gate to Drain Charge	Q _{GD}		20		nC	
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 6.0 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		370		ns	I _F = 6.0 A di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		1.5		μC	

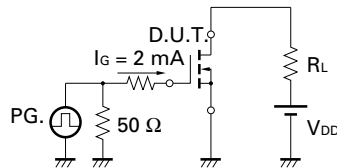
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time

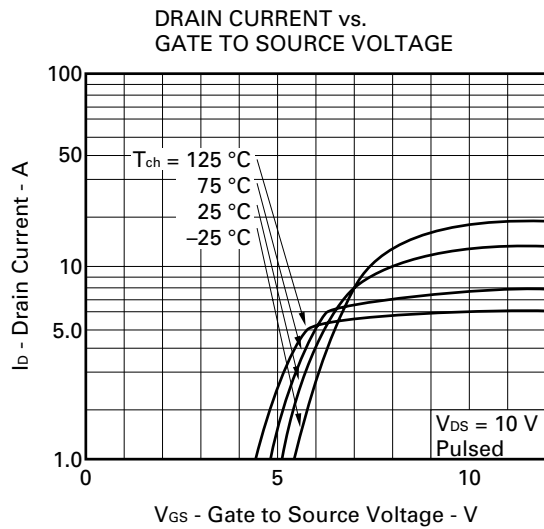
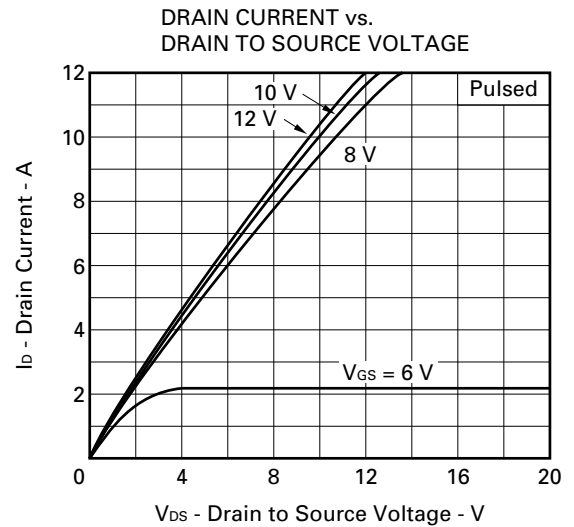
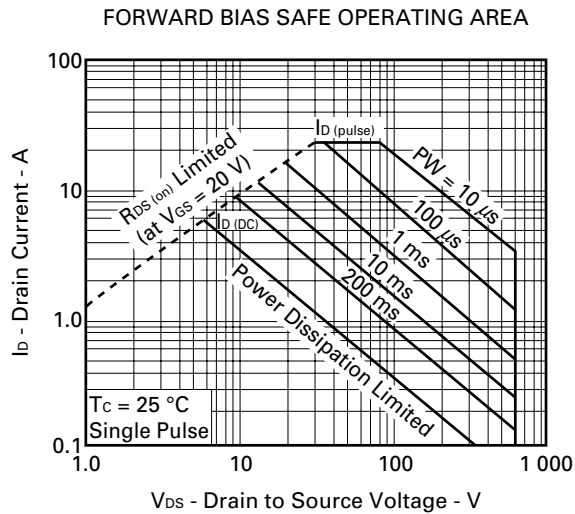
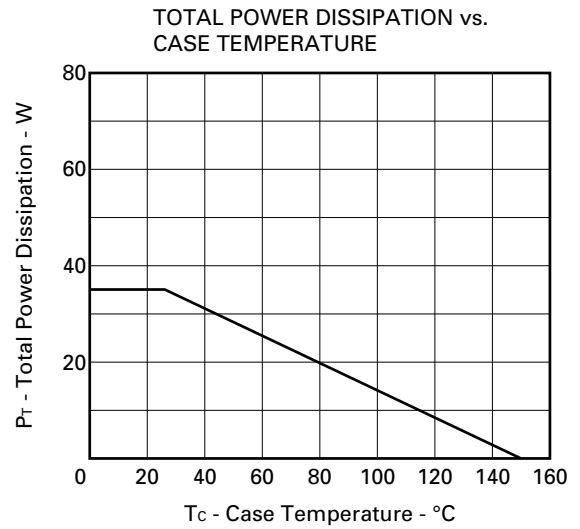
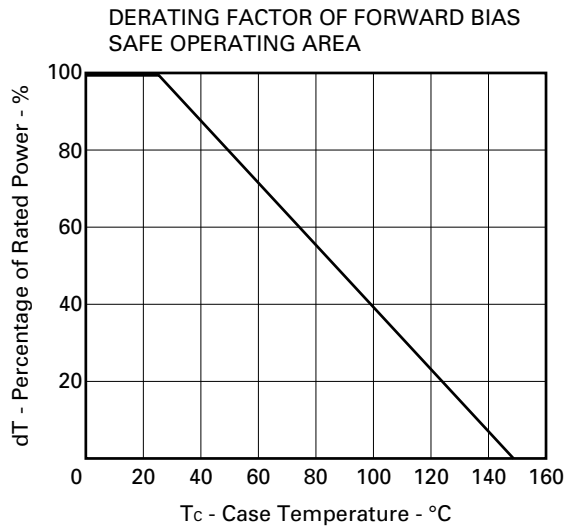


Test Circuit 3: Gate Charge

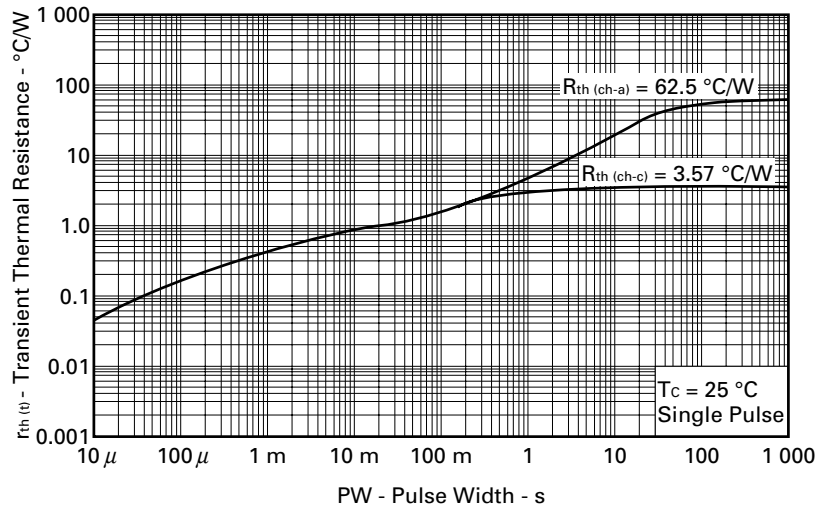


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

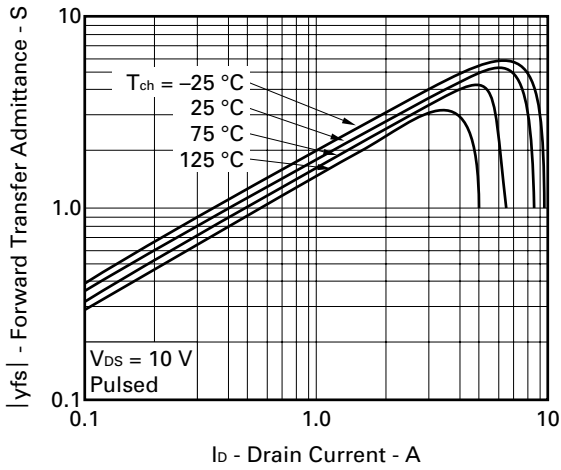
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



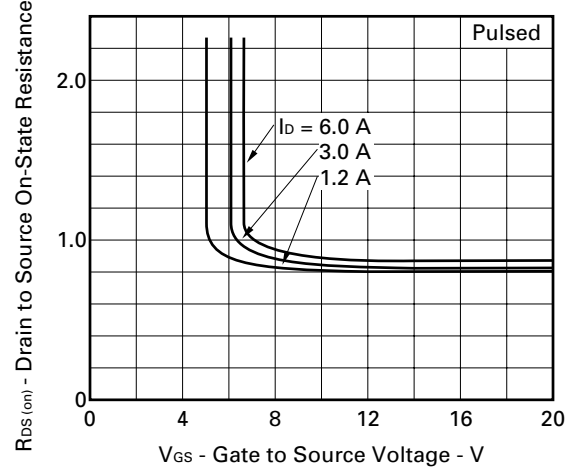
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



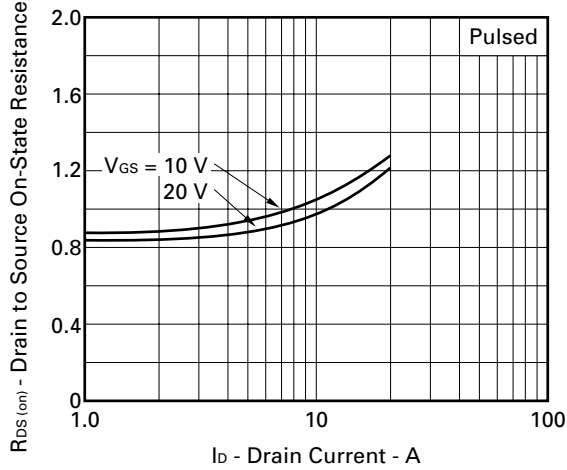
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



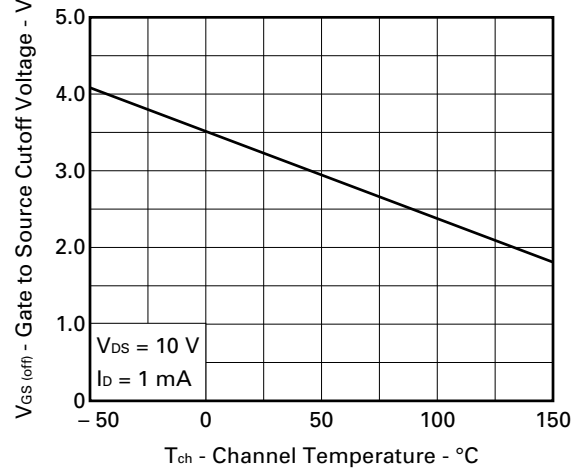
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

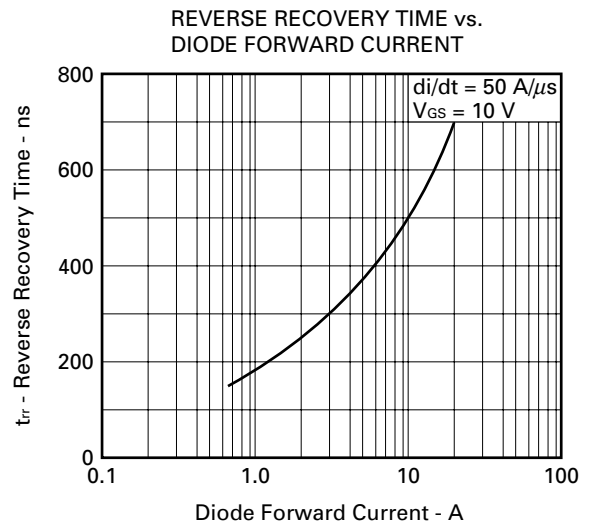
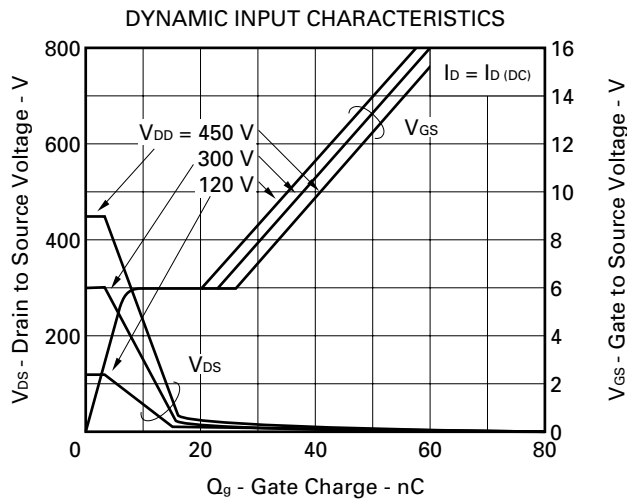
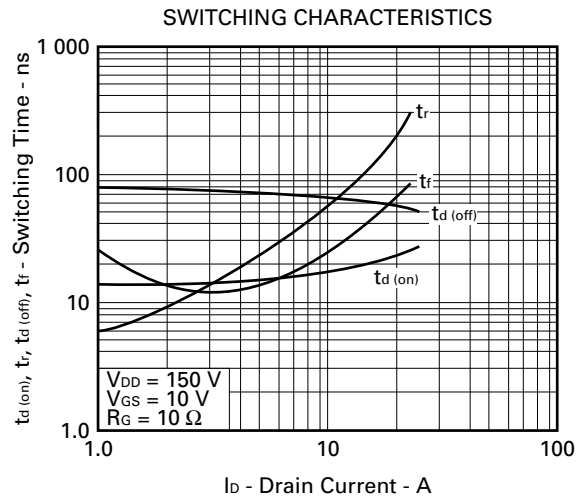
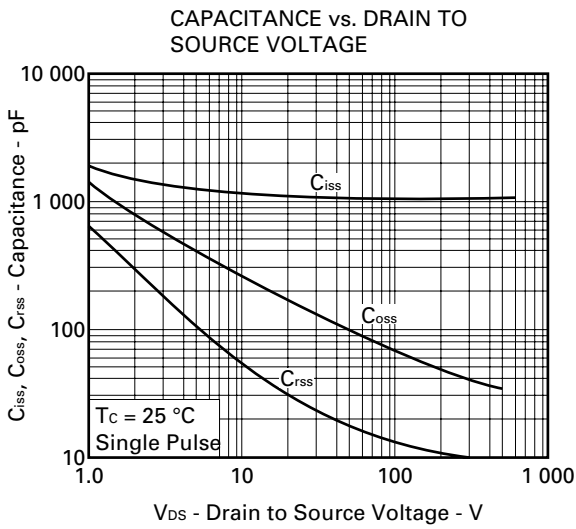
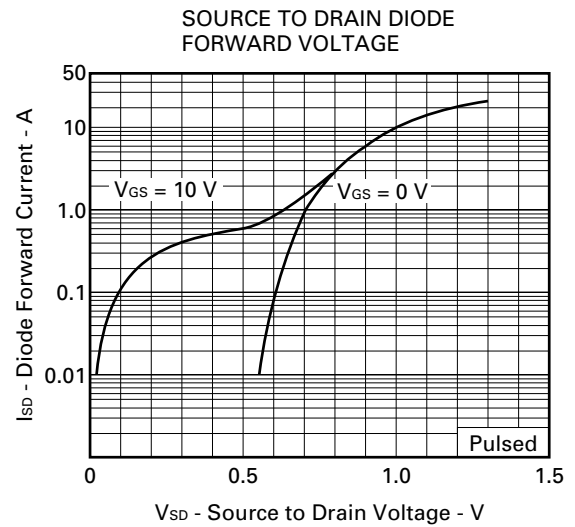
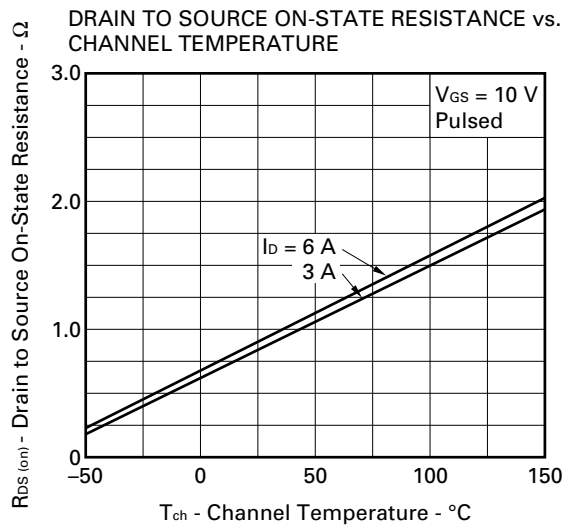


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

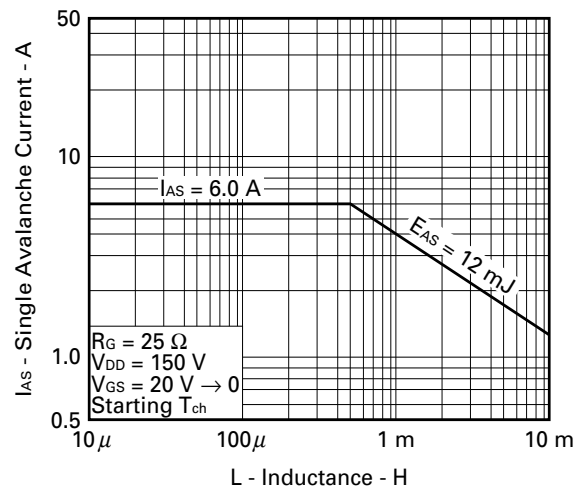


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

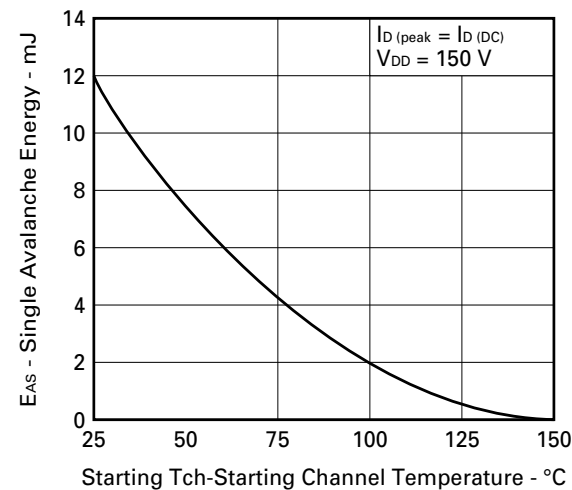




SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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