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P1 98.2

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SJ329

SWITCHING

P-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SJ329 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 47 \text{ m}\Omega \text{ TYP. (} V_{GS} = -10 \text{ V, } I_D = -8 \text{ A)}$
 $R_{DS(on)} = 80 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4 \text{ V, } I_D = -6 \text{ A)}$
- Low C_{iss} $C_{iss} = 2150 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

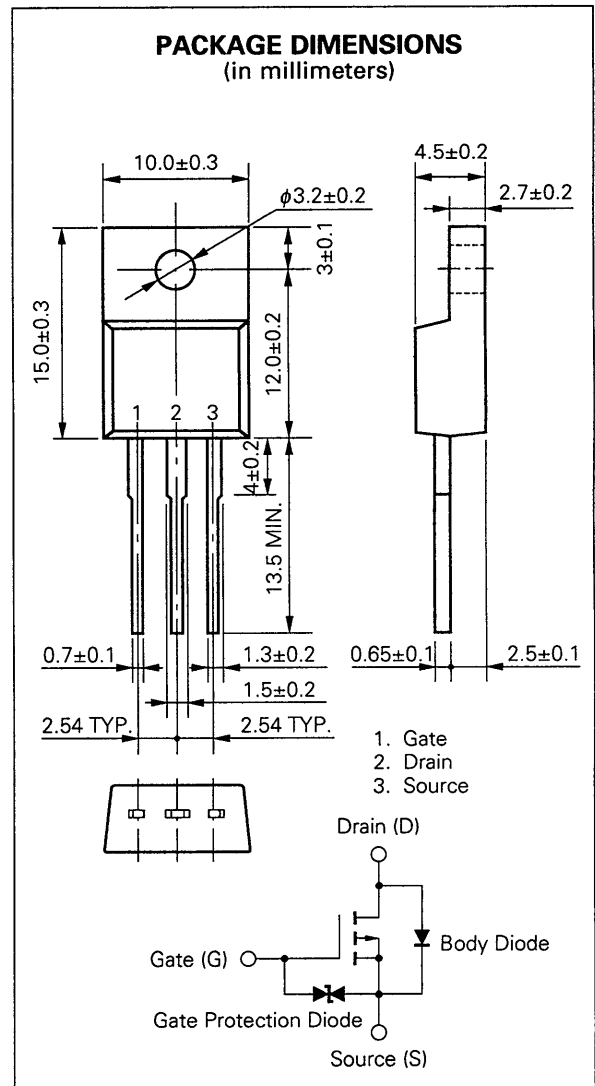
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage	$V_{GSS(DC)}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	± 15	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 60	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$) P_{T1}		35	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$) P_{T2}		2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C MAX.}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

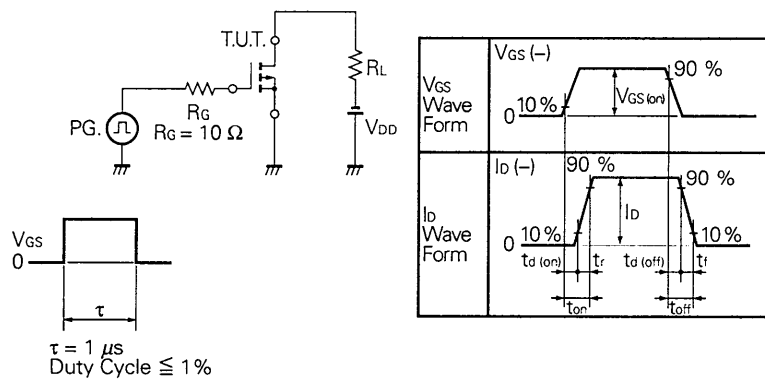
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$



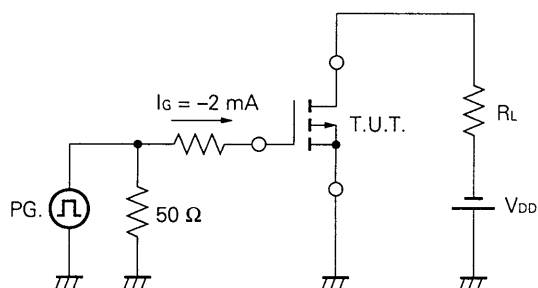
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		47	60	mΩ	V _{GS} = -10 V, I _D = -8 A
Drain to Source On-state Resistance	R _{DS(on)}		80	110	mΩ	V _{GS} = -4 V, I _D = -6 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	8.0	12		S	V _{DS} = -10 V, I _D = -8 A
Drain Leakage Current	I _{DSS}			-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 150		pF	V _{DS} = -10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		1 100		pF	
Reverse Transfer Capacitance	C _{rss}		530		pF	
Turn-On Delay Time	t _{d(on)}		35		ns	V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -8 A, R _G = 10 Ω R _L = 3.8 Ω
Rise Time	t _r		150		ns	
Turn-Off Delay Time	t _{d(off)}		260		ns	
Fall Time	t _f		230		ns	
Total Gate Charge	Q _G		80		nC	V _{GS} = -10 V I _D = -15 A V _{DD} = -48 V
Gate to Source Charge	Q _{GS}		6		nC	
Gate to Drain Charge	Q _{GD}		35		nC	
Diode Forward Voltage	V _{SD}		1.0		V	I _F = 15 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		120		ns	I _F = 15 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		260		nC	

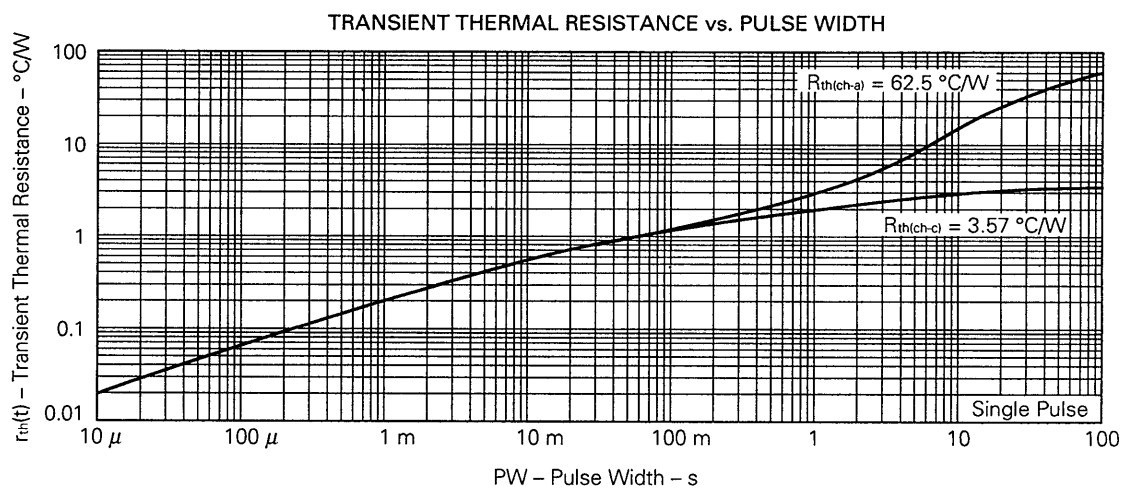
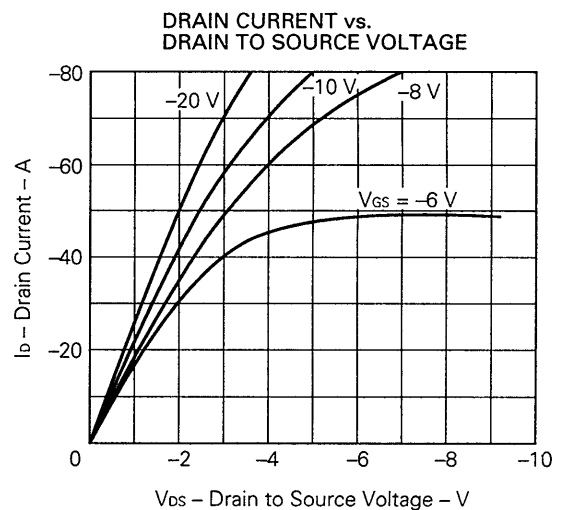
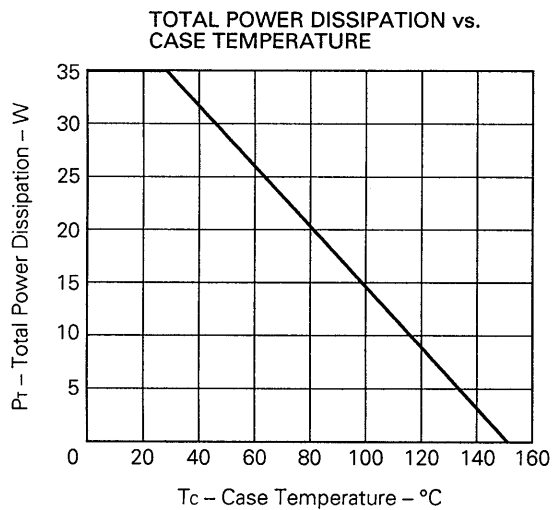
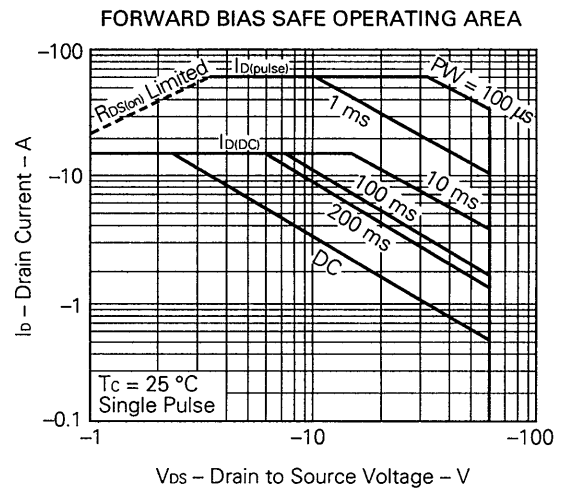
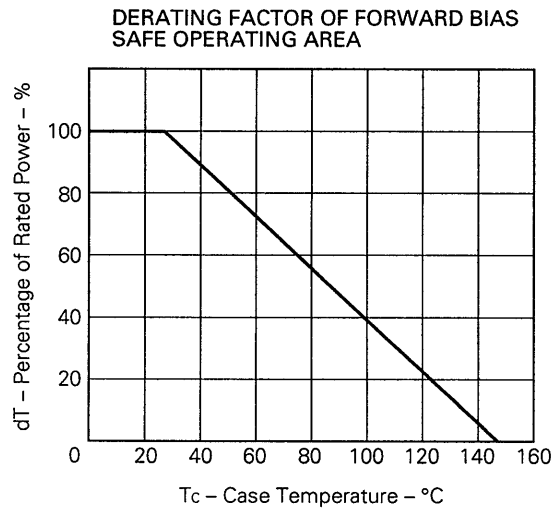
Test Circuit 1: Switching Time



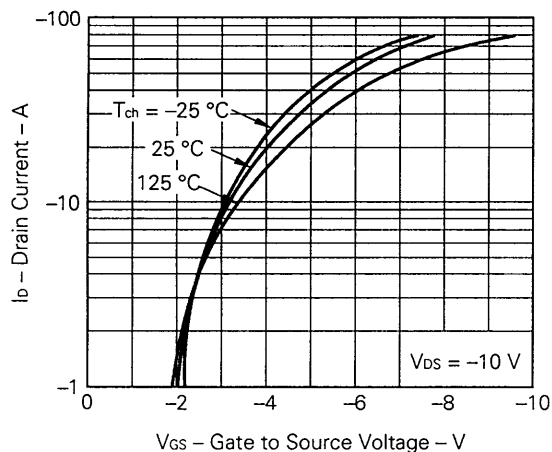
Test Circuit 2: Gate Charge



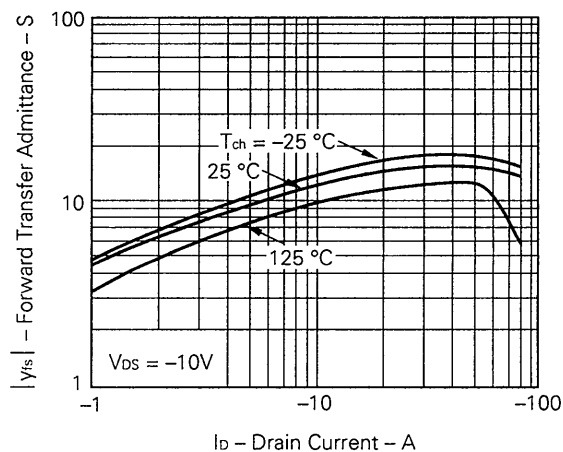
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



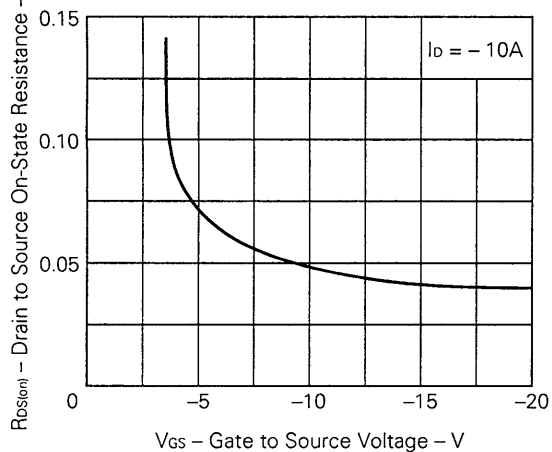
TRANSFER CHARACTERISTICS



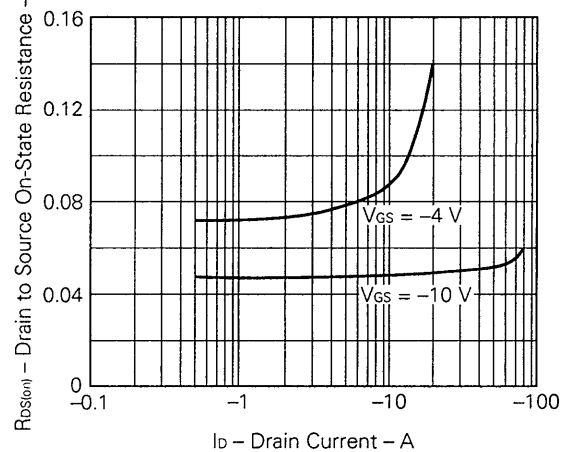
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



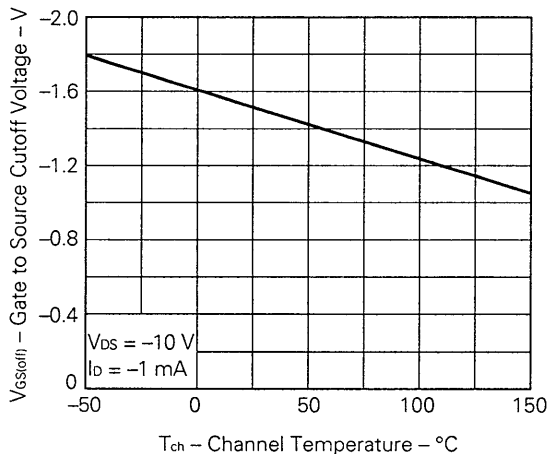
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



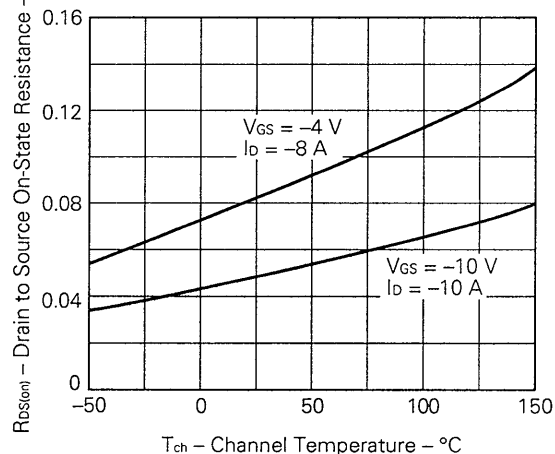
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

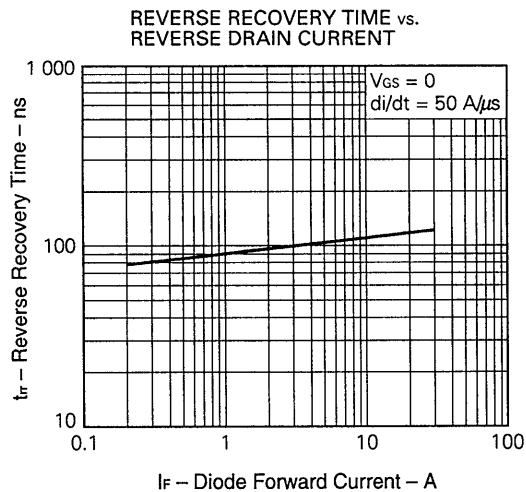
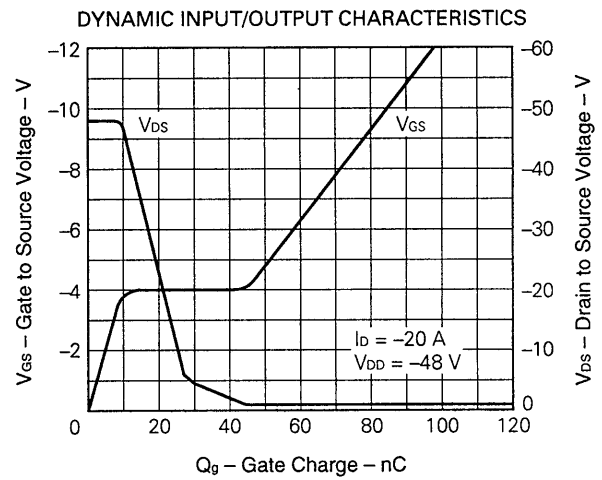
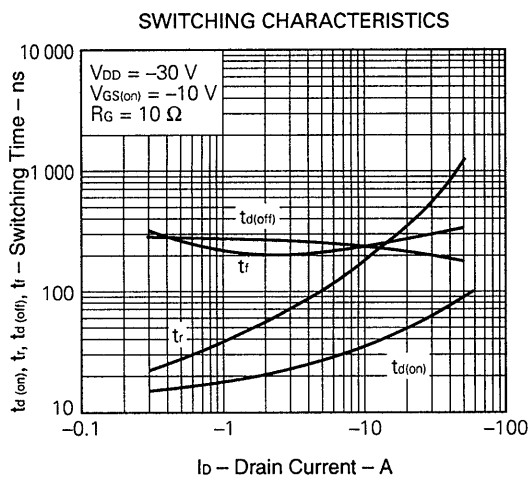
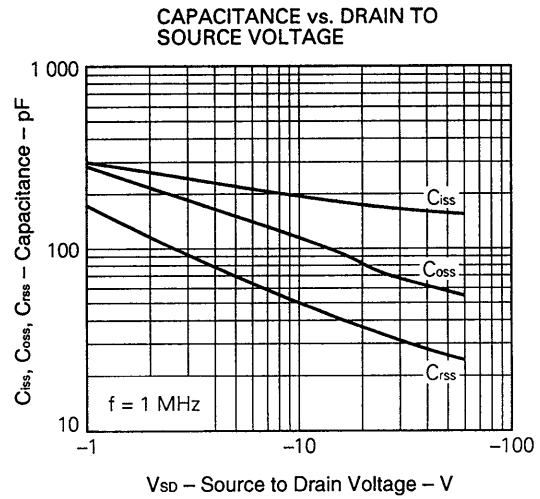
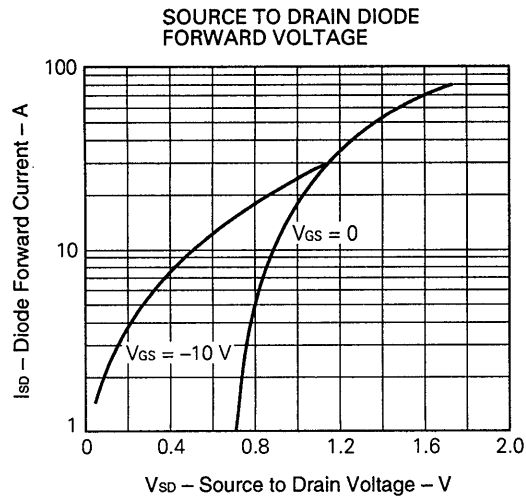


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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