DIGITAL AMPLIFIER POWER STAGE

FEATURES

- **70-W RMS Power (BTL) Into 4 Ω With Less Than 0.2% THD+N**
- **85-W RMS Power (BTL) Into 4 Ω With Less Than 10% THD+N (DKD)**
- **95-dB Dynamic Range (TDAA System With TAS5026)**
- **Power Efficiency Greater Than 90% Into 4-Ω and 8-Ω Loads**
  - **Smaller Power Supplies**
- **Self-Protecting Design**
- **32-Pin TSSOP (DAD) PowerPAD™ Package**
- **36-Pin PSOP3 (DKD) PowerPAD Package**
- **3.3-V Digital Interface**
  - **Built-in Converter From 3.3V to PVDD**
- **EMI Compliant When Used With Recommended System Design**
  - **Proven Design**

APPLICATIONS

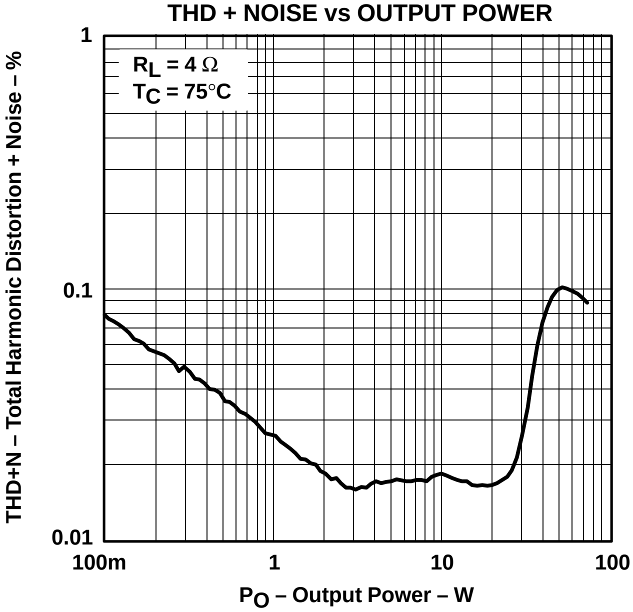
- **DVD Receiver**
- **Home Theatre**
- **Mini/Micro Component Systems**
- **Internet Music Appliance**

DESCRIPTION

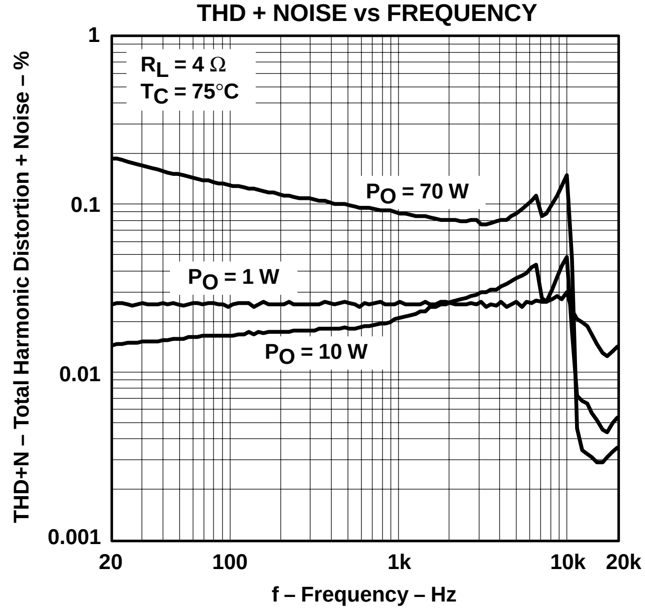
The TAS5111 is a high-performance digital amplifier power stage designed to drive a 4-Ω speaker up to 70 W with 0.2% distortion plus noise. The device incorporates TI's Equibit™ technology and is used in conjunction with a digital audio PWM processor (TAS50XX) and a simple passive demodulation filter to deliver high-quality, high-efficiency digital audio amplification.

The efficiency of this digital amplifier can be greater than 90%, depending on the system design. Overcurrent protection, overtemperature protection, and undervoltage protection are built into the TAS5111, safeguarding the device and speakers against fault conditions that could damage the system.

THD + NOISE vs OUTPUT POWER



THD + NOISE vs FREQUENCY



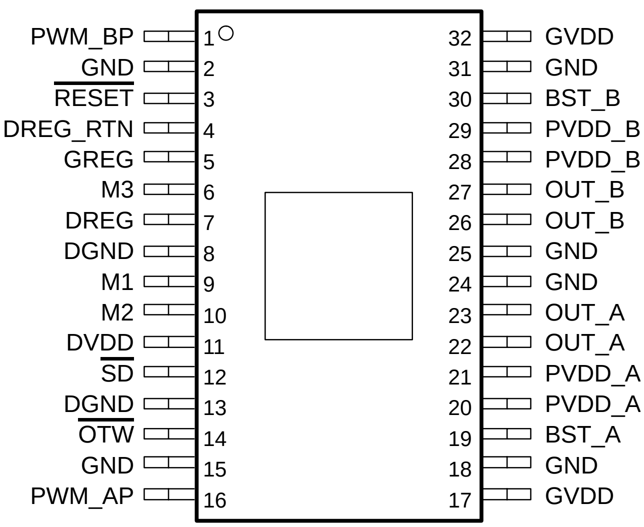
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

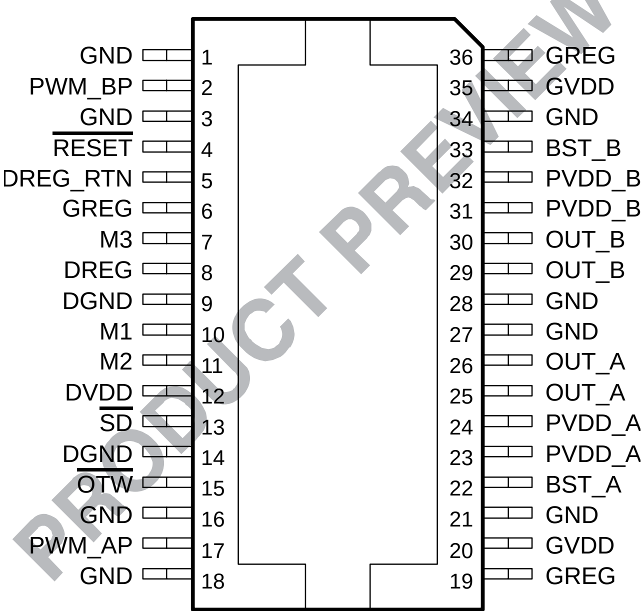
Terminal Assignment

The TAS5111 is offered in a thermally enhanced 32-pin TSSOP surface-mount package (DAD) and 36-pin PSOP3 (DKD). The DAD and DKD packages have the thermal pad on top.

DAD PACKAGE
(TOP VIEW)



DKD PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

TAS5111	UNITS
DVDD TO DGND	–0.3 V to 4.2 V
GVDD TO GND	33.5 V
PVDD_X TO GND (dc voltage)	33.5 V
PVDD_X TO GND (spike voltage(2))	48 V
OUT_X TO GND (dc voltage)	33.5 V
OUT_X TO GND (spike voltage(2))	48 V
BST_X TO GND (dc voltage)	48 V
BST_X TO GND (spike voltage(2))	53 V
GREG TO GND (3)	14.2 V
PWM_XP, RESET, M1, M2, M3, SD, OTW	–0.3 V to DVDD + 0.3 V
Maximum operating junction temperature, T_J	–40°C to 150°C
Storage temperature	–40°C to 125°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The duration of voltage spike should be less than 100 ns.
(3) GREG is treated as an input when the GREG pin is overdriven by GVDD of 12 V.

ORDERING INFORMATION

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5111DAD	32-pin small TSSOP
	TAS5111DKD	36-pin large PSOP3

(1) For the most current specification and package information, refer to our web site at www.ti.com.

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)
36-Pin DKD PSOP3	0.85	See Note 1
32-Pin DAD TSSOP	1.69	See Note 1

(1) Both versions of the TAS5111 package are thermally enhanced for conductive cooling using an exposed metal pad area. It is impractical to use the devices with the pad exposed to ambient air as the only heat sinking of the device.

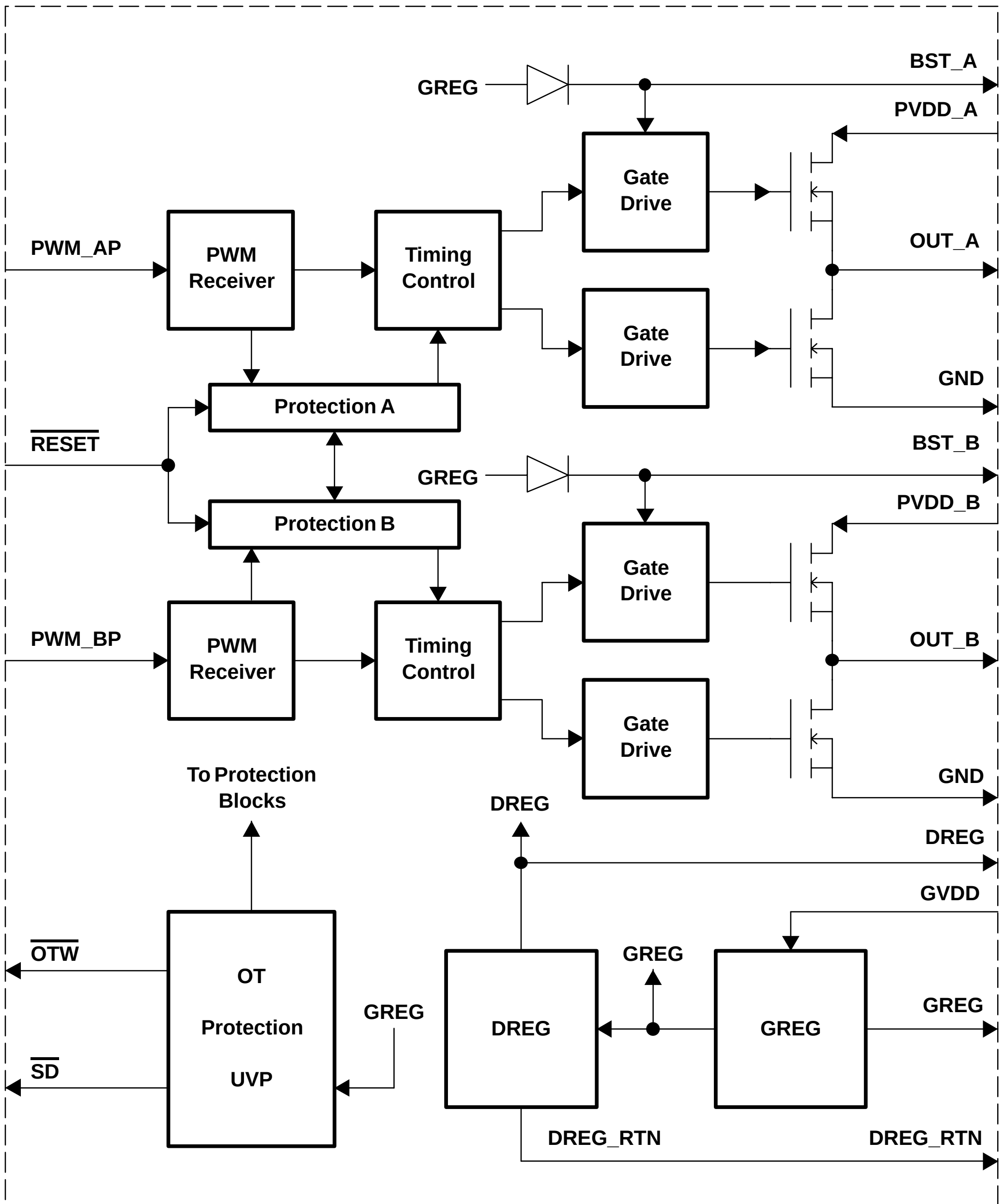
For this reason, $R_{\theta JA}$ a system parameter that characterizes the thermal treatment provided in the application. An example and discussion of typical system $R_{\theta JA}$ values are provided in the *Thermal Information* section. This example provides additional information regarding the power dissipation ratings. This example should be used as a reference to calculate the heat dissipation ratings for a specific application. TI application engineering provides technical support to design heat sinks if needed. Also, for additional general information on PowerPad packages, see TI (SLMA002).

Terminal Functions

TERMINAL			FUNCTION(1)	DESCRIPTION
NAME	DKD	DAD		
BST_A	22	19	P	HS bootstrap supply (BST), external capacitor to OUT_A required
BST_B	33	30	P	HS bootstrap supply (BST), external capacitor to OUT_B required
DGND	9, 14	8, 13	P	I/O reference ground
DREG	8	7	P	Digital supply voltage regulator decoupling pin, capacitor connected to DREG_RTN
DREG_RTN	5	4	P	Decoupling return pin
DVDD	12	11	P	I/O reference supply input (3.3V): 100 Ω to DREG
GND	1, 3, 16, 18, 21, 27, 28, 34	2,15, 18, 24, 25, 31	P	Power ground
GREG	6, 19, 36	5	P	Gate drive voltage regulator decoupling pin, capacitor to GND
GVDD	20, 35	17, 32	P	Voltage supply to on-chip gate drive and digital supply voltage regulators
M1	10	9	I	Mode selection pin
M2	11	10	I	Mode selection pin
M3	7	6	I	Mode selection pin
$\overline{\text{OTW}}$	15	14	O	Overtemperature warning output, open drain with internal pullup
OUT_A	25, 26	22, 23	O	Output, half-bridge A
OUT_B	29, 30	26, 27	O	Output, half-bridge B
PVDD_A	23, 24	20, 21	P	Power supply input for half-bridge A
PVDD_B	31, 32	28, 29	P	Power supply input for half-bridge B
PWM_AP	17	16	I	Input signal, half-bridge A
PWM_BP	2	1	I	Input signal, half-bridge B
RESET	4	3	I	Reset signal, active low
$\overline{\text{SD}}$	13	12	O	Shutdown signal for half-bridges A and B

(1) I = input, O = Output, P = Power

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
DVDD	Digital supply (1)	Relative to DGND	3	3.3	3.6	V
GVDD	Supply for internal gate drive and logic regulators	Relative to GND	16	29.5	30.5	V
PVDD_x	Half-bridge supply	Relative to GND, R_L = 4 Ω to 8 Ω	0	29.5	30.5	V
T_J	Junction temperature		0		125	°C

(1) It is recommended for DVDD to be connected to DREG via a 100-Ω resistor.

ELECTRICAL CHARACTERISTICS

PVDD_X = 29.5 V, GVDD = 29.5 V, DVDD = 3.3 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 4 Ω, 8X f_S = 384 kHz, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE				
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	T_A=40°C TO 85°C	UNITS	MIN/TYP/ MAX
AC PERFORMANCE, BTL Mode, 1 kHz								
Po	Output power	R_L = 8 Ω, THD = 0.2%, AES17 filter			40		W	Typ
		R_L = 8 Ω, THD = 10%, AES17 filter			53		W	Typ
		R_L = 6 Ω, THD = 0.2%, AES17 filter			53		W	Typ
		R_L = 6 Ω, THD = 10%, AES17 filter			68		W	Typ
		R_L = 4 Ω, THD = 0.2%, AES17 filter			74		W	Typ
		R_L = 4 Ω, THD = 10%, AES17 filter			93		W	Typ
THD+N	Total harmonic distortion + noise	Po = 1 W/ channel, R_L = 4 Ω, AES17 filter			0.05%			Typ
		Po = 10 W/channel, R_L = 4 Ω, AES17 filter			0.03%			Typ
		Po = 70 W/channel, R_L = 4 Ω, AES17 filter			0.2%			Typ
Noise	Output integrated noise	A-weighted, mute, R_L = 4 Ω, 20 Hz to 20 kHz, AES17 filter			295		μV	Max
SNR	Signal-to-noise ratio	A-weighted			95		dB	Typ
DR	Dynamic range	f = 1 kHz, A-weighted			95		dB	Typ
INTERNAL VOLTAGE REGULATOR								
DREG	Voltage regulator	I_O = 1 mA, PVDD = 18 V–30.5 V	3.1				V	Min
							V	Max
GREG	Voltage regulator	I_O = 1.2 mA, PVDD = 18 V–30.5 V	13.4				V	Min
							V	Max
IVGDD	GVDD supply current, operating	f_S = 384 kHz, no load, 50% duty cycle		27			mA	Max
IDVDd	DVDD supply current, operating	f_S = 384 kHz, no load	1	5			mA	Max
OUTPUT STAGE MOSFETs								
$R_{on,LS}$	Forward on-resistance, LS	T_J = 25°C	110	132			mΩ	Max
$R_{on,HS}$	Forward on-resistance, HS	T_J = 25°C	110	132			mΩ	Max

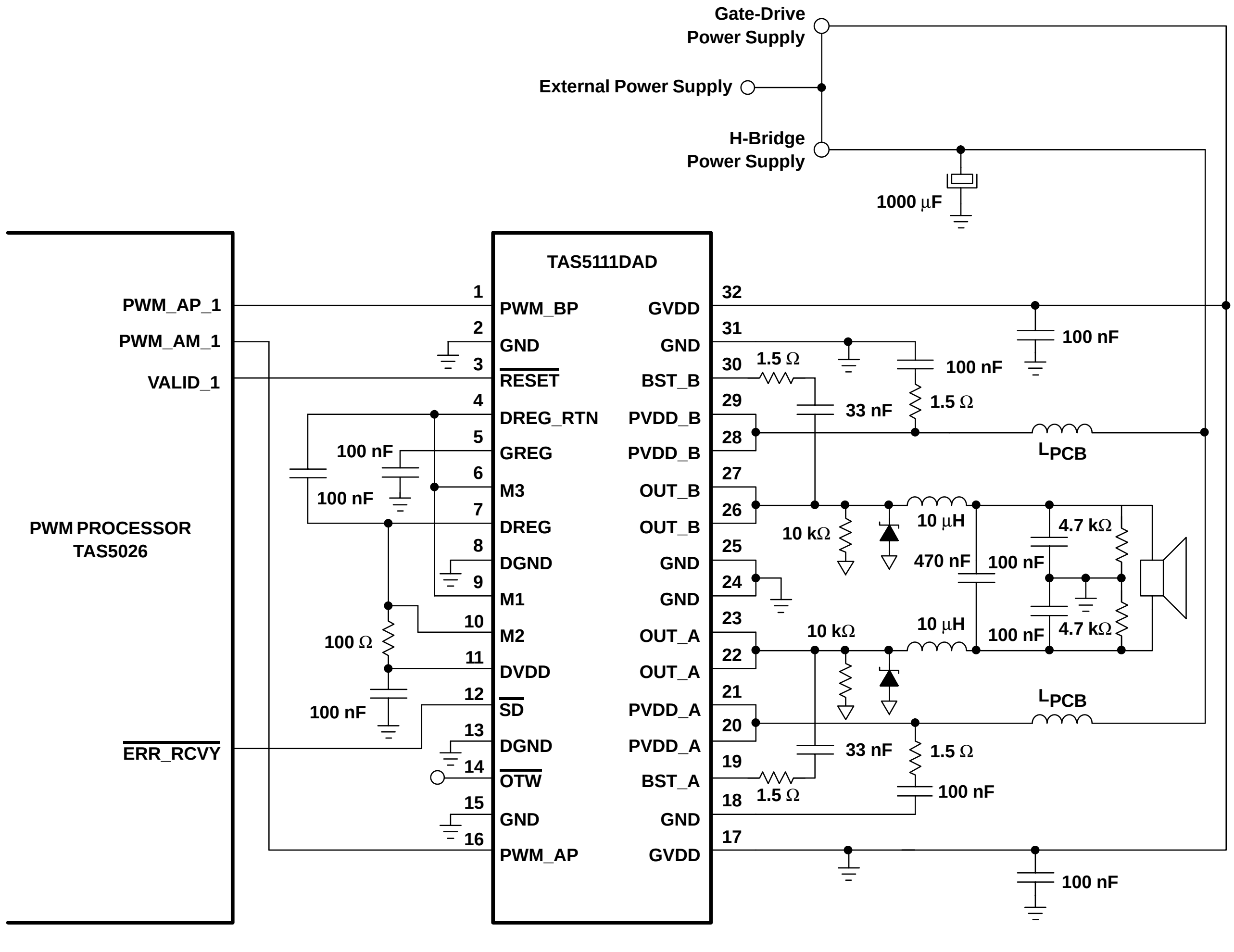
ELECTRICAL CHARACTERISTICS

PVDD_X = 29.5 V, GVDD = 29.5 V, DVDD = 3.3 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 4 Ω, 8X f_S = 384 kHz, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE				
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	T_A=40°C TO 85°C	UNITS	MIN/TYP/ MAX
INPUT/OUTPUT PROTECTION								
$V_{uvp,G}$	Undervoltage protection limit, GVDD	Set the DUT in normal operation mode with all the protections enabled. Sweep GVDD up and down. Monitor $\overline{SD}$ output. Record the GREG reading when $\overline{SD}$ is triggered.	7.4	6.9			V	Min
				7.9			V	Max
OTW	Overtemperature warning		125				°C	Typ
OTE	Overtemperature error		150				°C	Typ
OC	Overcurrent protection	See Note 1.	8				A	Typ
STATIC DIGITAL SPECIFICATION								
	PWM_AP, $\overline{PWM\_BP}$, M1, M2, M3, $\overline{SD}$, $\overline{OTW}$							
V_{IH}	High-level input voltage			2			V	Min
				DVDD			V	Max
V_{IL}	Low-level input voltage			0.8			V	Max
Leakage	Input leakage current			–10			μA	Min
				10			μA	Max
OTW/SHUTDOWN (SD)								
	Internally pull up R from $\overline{OTW}$/$\overline{SD}$ to DVDD		28	22			kΩ	Min
V_{OL}	Low level output voltage	I_O = 4 mA		0.4			V	Max

(1) To optimize device performance and prevent overcurrent (OC) protection tripping, the demodulation filter must be designed with special care. See *Demodulation Filter Design* in the *Application Information* section of the data sheet and consider the recommended inductors and capacitors for optimal performance. It is also important to consider PCB design and layout for optimum performance of the TAS5111. It is recommended to review the TAS5026-5111KEVM (S/N 001) design and layout documents as an example.

SYSTEM CONFIGURATION USED FOR CHARACTERIZATION



LPCB : TRACK IN THE PCB (1.0 mm wide and 50 mm long)

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

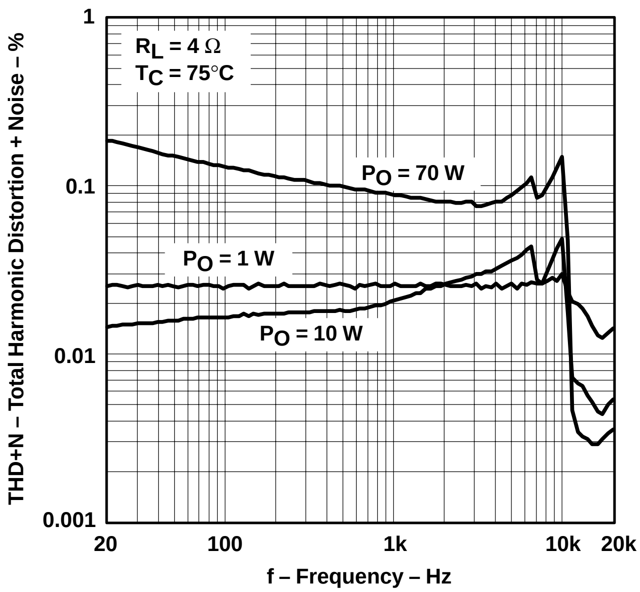


Figure 1

NOISE AMPLITUDE vs FREQUENCY

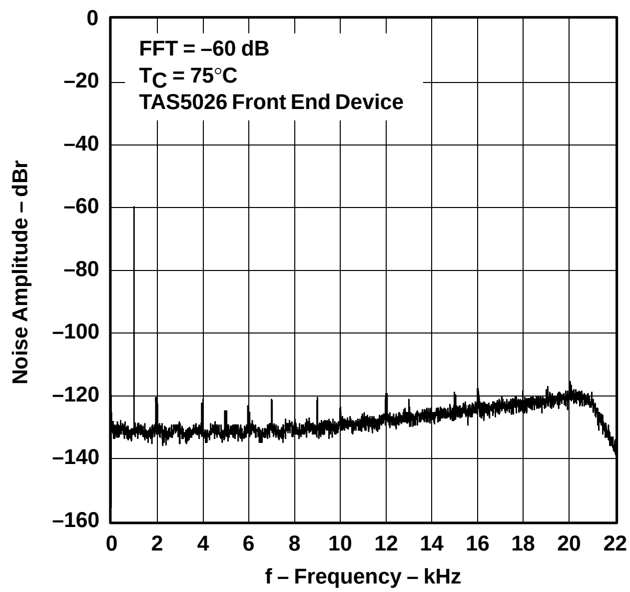


Figure 2

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

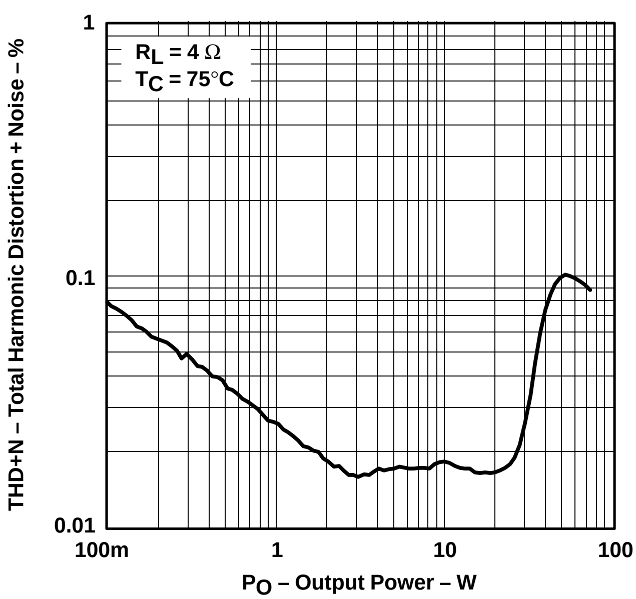


Figure 3

OUTPUT POWER vs H-BRIDGE VOLTAGE

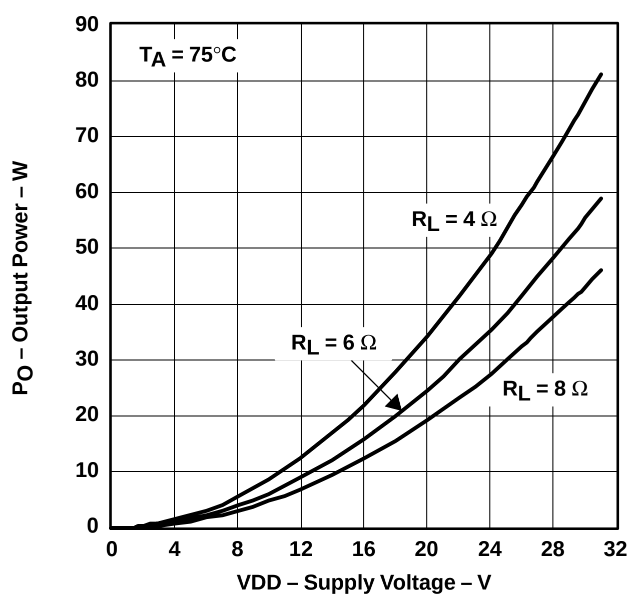


Figure 4

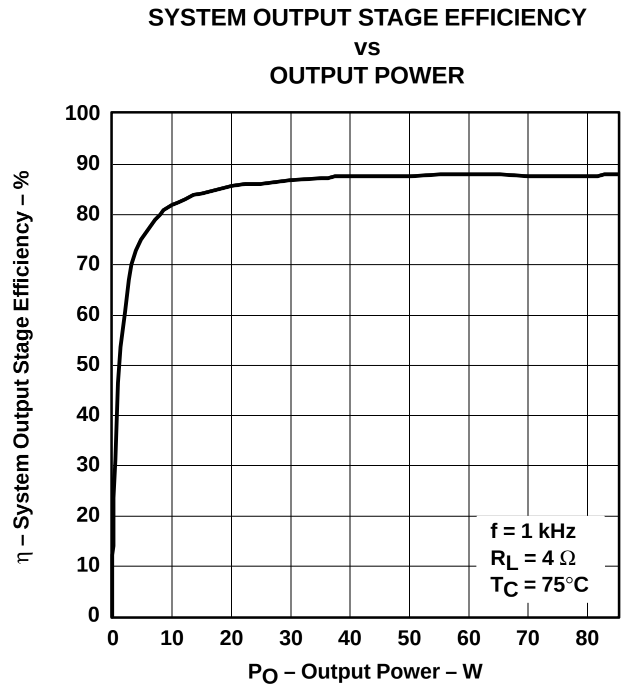


Figure 5

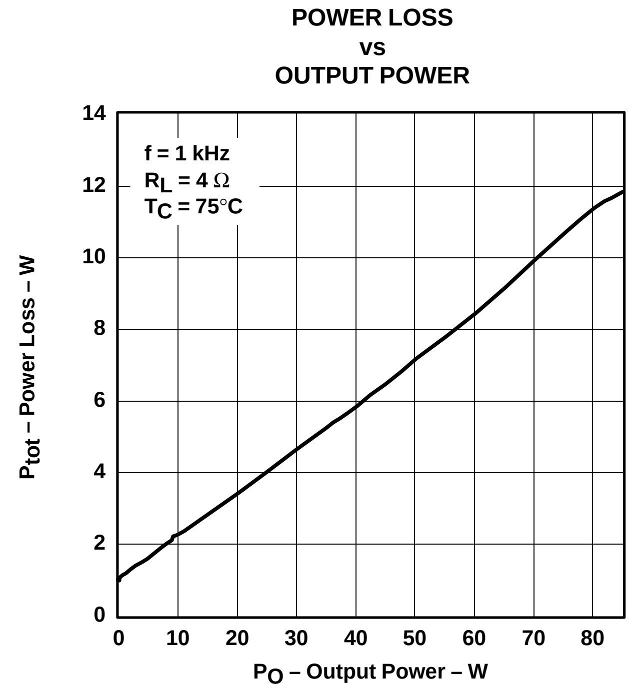


Figure 6

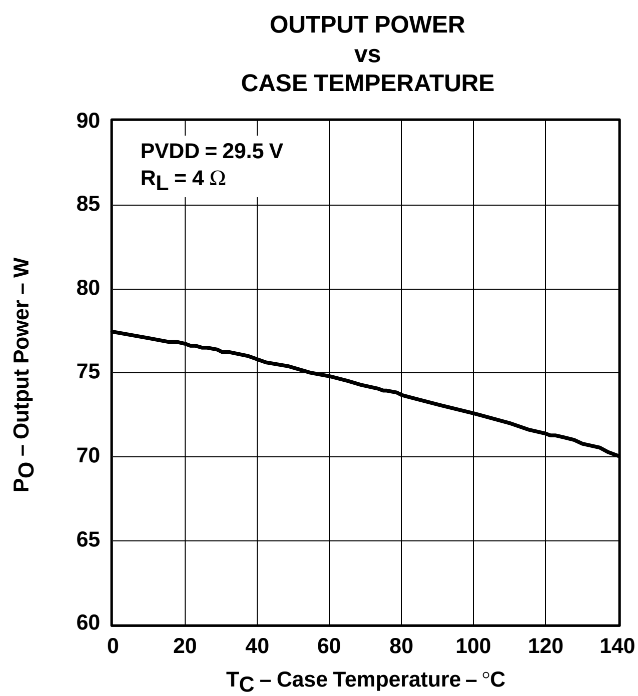


Figure 7

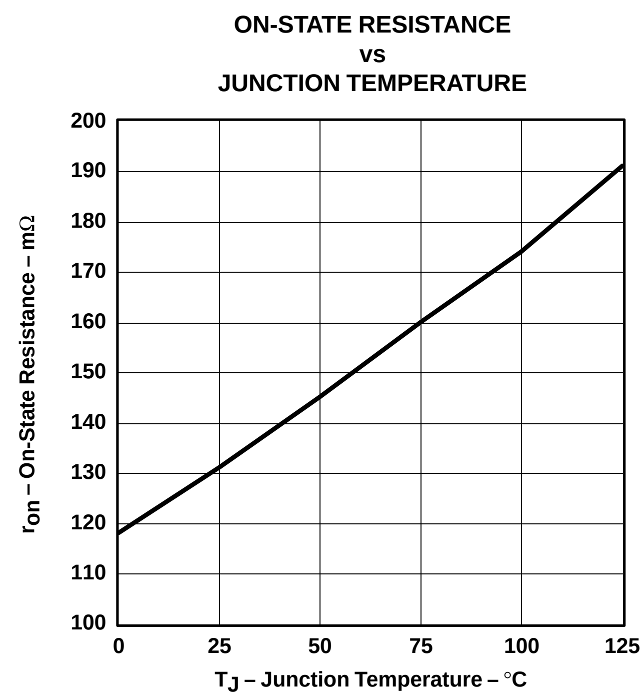


Figure 8

THEORY OF OPERATION

POWER SUPPLIES

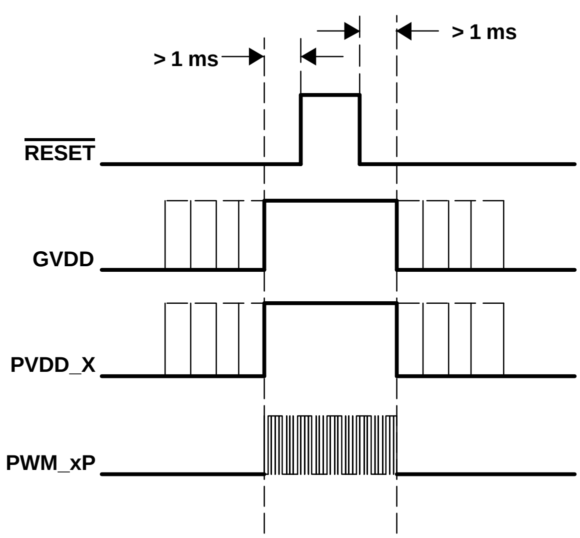
The power device only requires two supply voltages, GVDD and PVDD_X.

GVDD is the gate drive supply for the device, regulated internally down to approximately 12 V, and decoupled with regards to board GND on the GREG pins through an external capacitor. GREG powers both the low side and high side via a bootstrap step-up conversion. The bootstrap supply is charged after the first low-side turnon pulse. Internal digital core voltage DREG is also derived from GVDD and regulated down by internal LDRs to 3.3 V.

The gate-driver LDR can be bypassed for reducing idle loss in the device by shorting GREG to GVDD and directly feeding in 12.0 V. This can be useful in an application where thermal conduction of heat from the device is difficult. Bypassing the LDR reduces dissipation by approximately 1 W at 30 V GVDD input.

PVDD_X is the H-bridge power supply pin. Two power pins exists for each half-bridge to handle the current density. It is very important that the circuitry recommendations around the PVDD_X pins are followed very carefully both topology- and layout-wise. For topology recommendations, see the *Typical System Configuration* section. For layout recommendations, see the reference design layout for the TAS5111. Following these recommendations is important for parameters like EMI, reliability, and performance.

POWERING UP



During power up when RESET is asserted LOW, all MOSFETs are turned off and the two internal half-bridges are in the high-impedance state (Hi-Z). The bootstrap capacitors supplying high-side gate drive are at this point not charged. To comply with the click and pop scheme and use of non-TI TDAA modulators it is recommended to use a 4-kΩ pulldown resistor on each PWM output node to ground. This precharges the bootstrap supply capacitors and discharges the output filter capacitor (see the *Typical TAS5111 Application Configuration* section).

After GVDD has been applied, it takes approximately 800 µs to fully charge the BST capacitor. Within this time, RESET must be kept low. After approximately 1 ms, the back-end bootstrap capacitor is charged.

RESET can now be released if the modulator is powered up and streaming valid PWM signals to the back-end PWM_xP. Valid means a switching PWM signal which complies with the frequency and duty cycle ranges stated in the *Recommended Operating Conditions*.

A constant HIGH dc level on the PWM_xP is not permitted, because it would force the high-side MOSFET ON until it eventually ran out of BST capacitor energy and might damage the device.

An unknown state of the PWM output signals from the modulator is illegal and should be avoided, which in practice means that the PWM processor must be powered up and initialized before RESET is de-asserted HIGH to the back end.

POWERING DOWN

For power down of the back end, an opposite approach is necessary. The RESET must be asserted LOW before the valid PWM signal is removed.

When TI TDAA modulators are used in conjunction with TI TDAA back ends, the correct timing control of RESET and PWM_xP is performed by the modulator.

PRECAUTION

The TAS5111 must always start up in the high-impedance (Hi-Z) state. In this state, the bootstrap (BST) capacitor is precharged by a resistor on each PWM output node to ground. See the system configuration. This ensures that the back end is ready for receiving PWM pulses, indicating either HIGH- or LOW-side turnon after RESET is deasserted to the back end.

With the following pulldown and BST capacitor size the charge time is:

$C = 33\ nF,\ R = 4.7\ k\Omega$
$R \times C \times 5 = 775.5\ \mu s$

After GVDD has been applied, it takes approximately 800 µs to fully charge the BST capacitor. During this time, RESET must be kept low. After approximately 1 ms the back end BST is charged and are ready. RESET can now be released if the PWM modulator is ready and is streaming valid PWM signals to the back end. Valid PWM signals are switching PWM signals with a frequency between 350–400 kHz. A constant HIGH level on the PWM+ would force the high side MOSFET ON until it eventually ran out of BST capacitor energy. Putting the device in this condition should be avoided.

In practice this means that the DVDD-to-PWM processor (front-end) should be stable and initialization should be completed before RESET is deasserted to the back end.

An opposite approach is necessary when powering the system down. RESET must be asserted LOW before the valid PWM signal is removed.

CONTROL I/O

Shutdown Pin: SD

The SD pin functions as an output pin and is intended for protection-mode signaling to, for example, a controller or other front-end device. The pin is open-drain with an internal pullup to DVDD.

The logic output is, as shown in the following table, a combination of the device state and RESET input:

SD	RESET	DESCRIPTION
0	0	Not used
0	1	Device in protection mode, i.e., UVP and/or OC and/or OT error
1(1)	0	Device set high-impedance (Hi-Z), SD forced high
1	1	Normal operation

(1) SD is pulled high when RESET is asserted low independent of chip state (i.e., protection mode). This is desirable to maintain compatibility with some TI PWM front ends.

Temperature Warning Pin: OTW

The OTW pin gives a temperature warning signal when temperature exceeds the set limit. The pin is of the open-drain type with an internal pullup to DVDD.

OTW	DESCRIPTION
0	Junction temperature higher than 125°C
1	Junction temperature lower than 125°C

Overall Reporting

The SD pin, together with the OTW pin, gives chip state information as described in Table 1.

Table 1. Error Signal Decoding

OTW	SD	DESCRIPTION
0	0	Overtemperature error (OTE)
0	1	Overtemperature warning (OTW)
1	0	Overcurrent (OC) or undervoltage (UVP) error
1	1	Normal operation, no errors/warnings

Chip Protection

The TAS5111 protection function is implemented in a closed loop with, for example, a system controller or other TI PWM processor (front-end) device. The TAS5111 contains three individual systems protecting the device against misuse. All of the error events covered result in the output stage being set in a high-impedance state (Hi-Z) for maximum protection of the device and connected equipment.

The device can be recovered by toggling RESET low and then high, after all errors are cleared.

Overcurrent (OC) Protection

The device has individual forward current protection on both high-side and low-side power stage FETs. The OC protection works only with the demodulation filter present at the output. See *Filter Demodulation Design* in the *Application Information* section of the data sheet for design constraints.

Overtemperature (OT) Protection

A dual temperature protection system asserts a warning signal when the device junction temperature exceeds 125°C. The OT protection circuit is shared by all half-bridges.

Undervoltage (UV) Protection

Undervoltage lockout occurs when GVDD is insufficient for proper device operation. The UV protection system protects the device under power-up and power-down situations. The UV protection circuits are shared by all half-bridges.

Reset Function

The function of the reset input is twofold:

- Reset is used for re-enabling operation after a latching error event (PMODE1).
- Reset is used for disabling output stage switching (mute function) (all PMODEs).

In PMODEs where the reset input functions as the means to re-enable operation after an error event, the error latch is cleared on the falling edge of reset and normal operation is resumed when reset goes high.

PROTECTION MODE

Latching Shutdown on All Errors (PMODE1)

In latching shutdown mode, all error situations result in a permanent shutdown (output stage Hi-Z). Re-enabling can be done by toggling the RESET pin.

MODE Pins Selection

The protection mode is selected by shorting M1/M2 to DREG or DGND according to Table 2.

Table 2. Protection Mode Selection

M1	M2	PROTECTION MODE
0	0	Reserved
0	1	Latching shutdown on all errors (PMODE1)
1	0	Reserved
1	1	Reserved

The output configuration mode is selected by shorting the M3 pin to DREG or DGND according to Table 3.

Table 3. Output Mode Selection

M3	OUTPUT MODE
0	Bridge-tied load output stage (BTL)
1	Reserved

NOTE: When any of the RESET, MUTE, or ERROR_RECOVER pins is asserted, the speaker outputs are set to high impedance (Hi-Z).

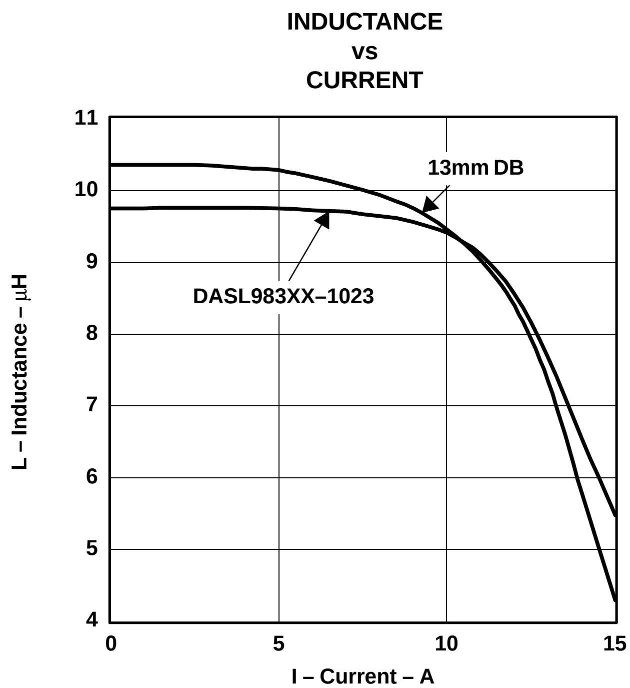


Figure 9. Inductance Saturation

APPLICATION INFORMATION

DEMODULATION FILTER DESIGN

Design of the demodulation filter affects the performance of the power amplifier significantly. As a result, to ensure proper operation of the overcurrent (OC) protection circuit and meet the device THD+N specifications, the selection of the inductors used in the output filter must be considered according to the following. The rule is that the inductance should remain stable within the range of peak current seen at maximum output power and deliver at least 5 µH of inductance at 15 A.

If this rule is observed, the TAS5111 will not have distortion issues due to the output inductors and overcurrent conditions will not occur due to inductor saturation in the output filter.

Another parameter to be considered is the idle current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05.

In general, 10-µH inductors suffice for most applications. The frequency response of the amplifier is slightly altered by the change in output load resistance; however, unless very tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 µH.

The graphs in Figure 9 and NO TAG display the inductance vs current characteristics of two inductors that are recommended for use with the TAS5111.

The selection of the capacitor that is placed across the output of each inductor (C_{load} in Figure 12) is very simple. To complete the output filter, use a 0.47-µF capacitor with a voltage rating at least twice the voltage applied to the output stage (PVDD).

This capacitor should be a good quality polyester dielectric such as a Wima MKS2-047ufd/100/10 or equivalent.

In order to minimize the EMI effect of unbalanced ripple loss in the inductors, 0.1-µF 50-V SMD capacitors (X7R or better) should be added from the output of each inductor to ground.

GENERAL PRINCIPLES OF DEMODULATION FILTER DESIGN

The TDAA amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either off or fully on, which reduces the DMOS transistor on-state resistance, R(DMOSon), and the power dissipated in the device, thereby increasing efficiency.

The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. For this application, EMI is considered important; therefore, the selected filter is the full-output type shown in Figure 10.

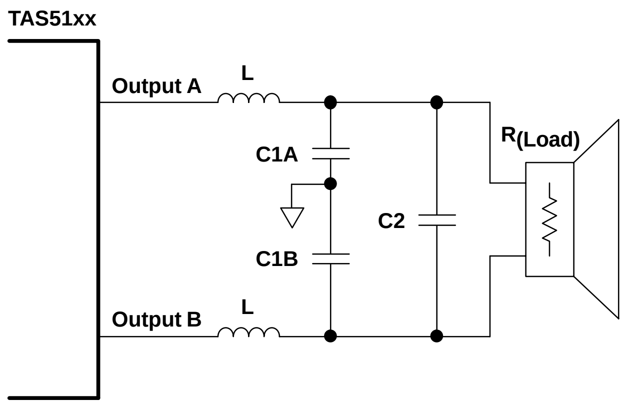


Figure 10. Demodulation Filter

The main purpose of the output filter is to attenuate the high-frequency switching component of the TDAA amplifier while preserving the signals in the audio band.

The first step in designing the filter is to construct the circuit and derive the transfer function, starting first with a half-circuit model and moving later to the full-bridge circuit. The half-circuit model of the Butterworth low-pass filter output is shown in Figure 11, with only one-half of the desired dc load resistance, $R_{(load)}$, of the speaker shown. The input signal, V(in), is the 352.8-kHz square-wave output of the TDAA amplifier, while the output, V_O, is the voltage developed across the speaker.

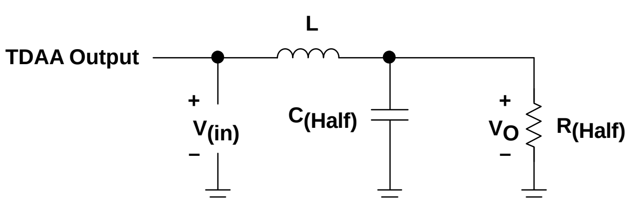


Figure 11. Butterworth Low-Pass Filter Half-Circuit Model

The transfer function for this half circuit is:

$$H(s) = \frac{\frac{1}{L_{(half)}C_{(half)}}}{s^2 + \frac{1}{R_{(half)}C_{(half)}}s + \frac{1}{L_{(half)}C_{(half)}}}$$

The component values are:

$$C_{(half)} = \frac{1}{2\sqrt{2}\pi f_{co} R_{(half)}}$$

and

$$L_{(half)} = \frac{R_{(half)}}{\sqrt{2}\pi f_{co}}$$

The two half-circuit models are now combined to yield the actual bridge-tied load (BTL) circuit shown in Figure 12 and the capacitors and resistors are combined to provide the final BTL equations.

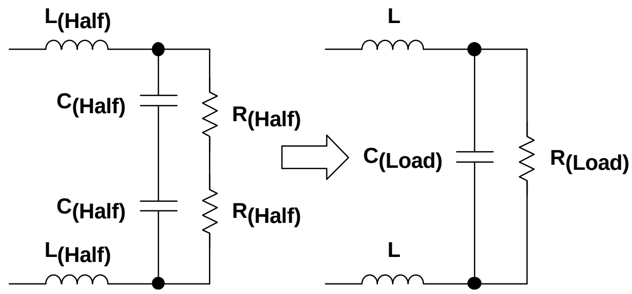


Figure 12. Combination of the Two Half-Circuit Models

$R_{(load)} = 2R_{(half)}$

$$C_{(load)} = \frac{1}{2\sqrt{2}\pi R_{(load)} f_{co}}$$

$$L = L_{(half)} = \frac{\sqrt{2}R_{(load)}}{4\pi f_{co}}$$

The inductance value is the same for the half- and full-bridge circuits because there are two inductances in the BTL circuit. Based on these BTL component values, the –3-dB cutoff frequency for the LC filter is:

$$f_{co} = \frac{1}{2\pi\sqrt{2 L C_{(load)}}}$$

where the $\sqrt{2}$ in the denominator is the result of transposing the inductance and capacitance values from the half-circuit to the BTL full-circuit model.

The capacitors labeled C1A and C1B in Figure 10 serve as high-frequency bypass capacitors acting as a common-mode filter and are empirically chosen to be approximately 10% of $2 \times C_L$.

THERMAL INFORMATION

The thermally augmented packages provided with the TAS5111 are designed to be interfaced directly to heat sinks using a thermal interface compound (for example, Wakefield Engineering type 126 thermal grease.) The heat sink then absorbs heat from the ICs and couples it to the local air. If the heatsink is carefully designed, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the TAS5111, heat sinks will be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with roughly the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the metal pad)
- Thermal grease thermal resistance
- Heat sink thermal resistance

$R_{\theta JC}$ has been provided in the *General Information* section.

The thermal grease thermal resistance can be calculated from the exposed pad area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W). The area thermal resistance of the example thermal grease with a 0.001 inch thick layer is about 0.054 °C-in^2/W. The approximate exposed pad sizes are as follows:

36-pin PSOP3	0.116 in^2
32-pin TSSOP	0.0164 in^2

Dividing the example thermal grease area resistance by the area of the pad gives the actual resistance through the thermal grease for both parts:

36-pin PSOP3	0.47 °C/W
32-pin TSSOP	3.3 °C/W

Note that both $R_{\theta JC}$ and the thermal grease resistance are better for the PSOP3 package. The PSOP3 package should be used when output power is high and/or when the heat sink must be restricted in size.

The thermal resistance of thermal pads is generally considerably higher than a thin thermal grease layer. Pads should only be used with the PSOP3 package. Thermal tape has an even higher thermal resistance and should not be used at all with either of these two packages.

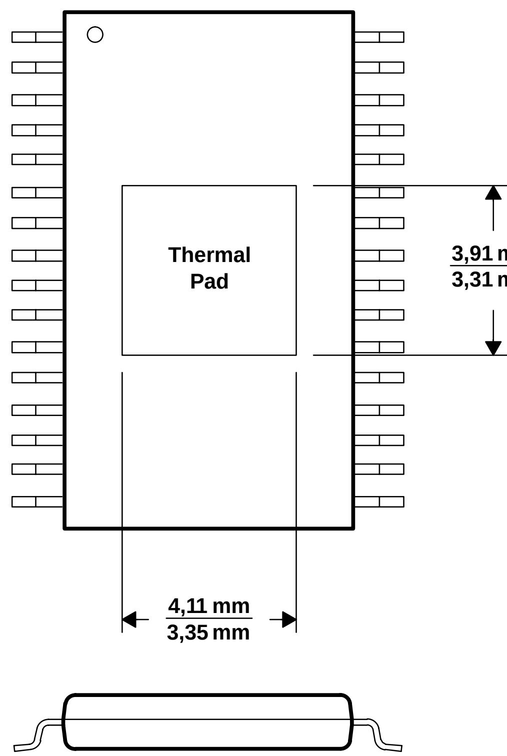
Heat sink thermal resistance is generally predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

The following table indicates modeled parameters for one TAS5111 IC on a heat sink. The junction temperature is set at 110°C in both cases while delivering 70 W RMS into 4-Ω loads with no clipping. It is assumed that the thermal grease is about 0.001 inch thick (this is critical).

	36-Pin PSOP3	32-Pin TSSOP
Ambienttemperature	25°C	25°C
Power to load	70 W	70 W
Delta T inside package	5.5°C	12.3°C
Delta T through thermal grease	3.2°C	21.1°C
Required heat sink thermal resistance	11.0°C/W	8.2°C/W
Junctiontemperature	110°C	110°C
System $R_{\theta JA}$	12.3°C/W	13.2°C/W
$R_{\theta JA}$ * power dissipation	85°C	85°C

As an indication of the importance of keeping the thermal grease layer thin, if the thermal grease layer increases to 0.002 inches thick, the required heat sink thermal resistance changes to 5.2°C/W for the PSOP3 package and to 2.4°C/W for the TSSOP package.



CLICK AND POP REDUCTION

Going from non-switching to switching operation causes a spectral energy burst to occur within the audio bandwidth, which is heard in the speaker as an audible click, for instance, after having asserted $\overline{\text{RESET}}$ LH during a system start-up.

To make this system work properly, the following design rules must be followed when using the TAS5111 back end:

- The relative timing between the PWM_AP/M_x signals and their corresponding VALID_x signal should not be skewed by inserting delays, because this increases the audible amplitude level of the click.

- The output stage must start switching from a fully discharged output filter capacitor. Because the output stage prior to operation is in the high-impedance state, this is done by having a passive pulldown resistor on each speaker output to GND (see *Typical System Configuration*).

Other things that can affect the audible click level:

- The spectrum of the click seems to follow the speaker impedance vs. frequency curve—the higher the impedance, the higher the click energy.
- Crossover filters used between woofer and tweeter in a speaker can have high impedance in the audio band, which should be avoided if possible.

Another way to look at it is that the speaker impulse response is a major contributor to how the click energy is shaped in the audio band and how audible the click will be.

The following mode transitions feature click and pop reduction.

STATE			CLICK AND POP REDUCED
Normal(1)	→	Mute	Yes
Mute	→	Normal(1)	Yes
Normal(1)	→	Error recovery (ERRCVY)	Yes
Error recovery	→	Normal(1)	Yes
Normal(1)	→	Hard Reset	No
Hard Reset	→	Normal(1)	Yes

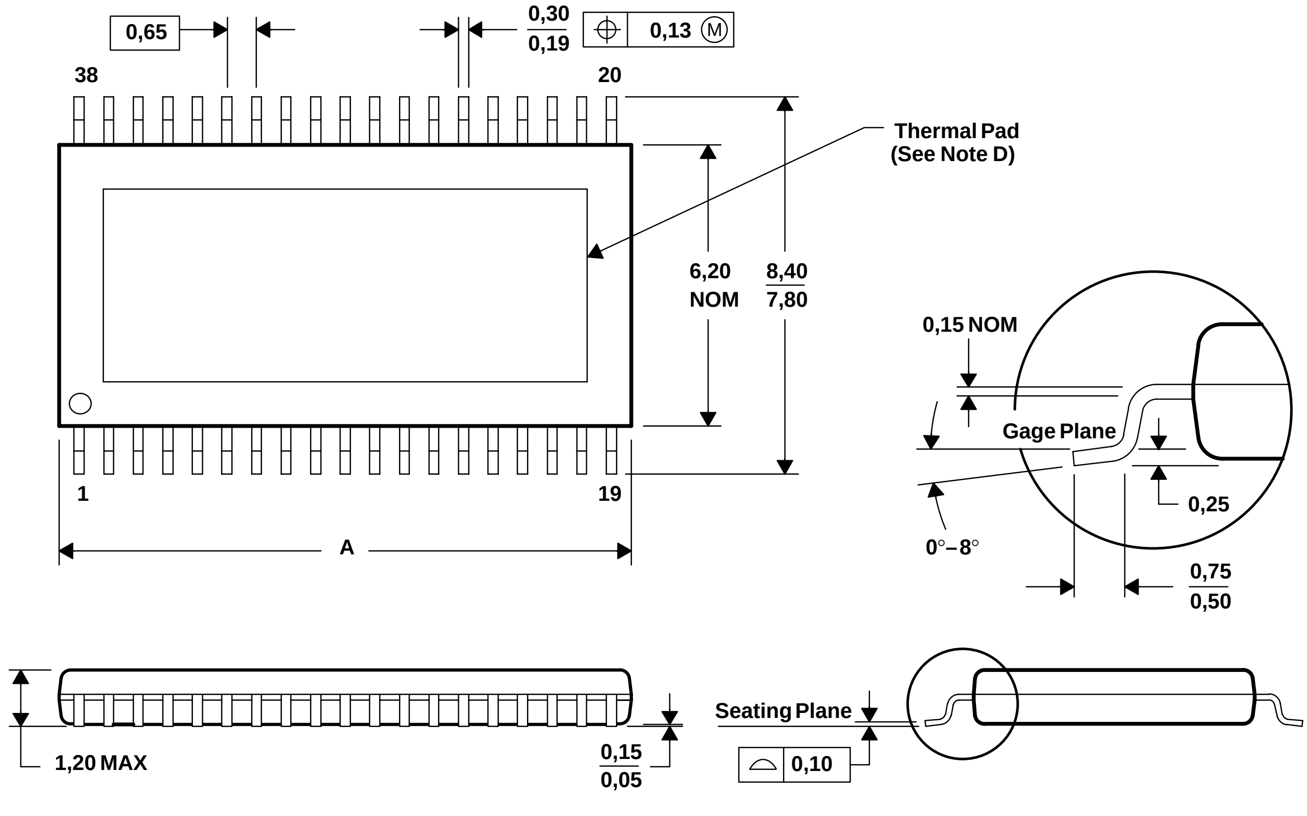
(1) Normal = switching

REFERENCES

1. *TAS5000 Digital Audio PWM Processor* data manual – TI (SLAS270)
2. *True Digital Audio Amplifier TAS5001 Digital Audio PWM Processor* data sheet – TI (SLES009)
3. *True Digital Audio Amplifier TAS5010 Digital Audio PWM Processor* data sheet – TI (SLAS328)
4. *True Digital Audio Amplifier TAS5012 Digital Audio PWM Processor* data sheet – TI (SLES006)
5. *TAS5026 Six-Channel Digital Audio PWM Processor* data manual – TI (SLES041)
6. *TAS5036A Six-Channel Digital Audio PWM Processor* data manual – TI (SLES061)
7. *TAS3103 Digital Audio Processor With 3D Effects* data manual – TI – TI (SLES038)
8. *Digital Audio Measurements* application report– TI (SLAA114)
9. *PowerPAD™ Thermally Enhanced Package* technical brief – TI (SLMA002)
10. *System Design Considerations for True Digital Audio Power Amplifiers* application report – TI (SLAA117)

DAD (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE (DIE DOWN)

38 PINS SHOWN



PINS ** / DIM	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

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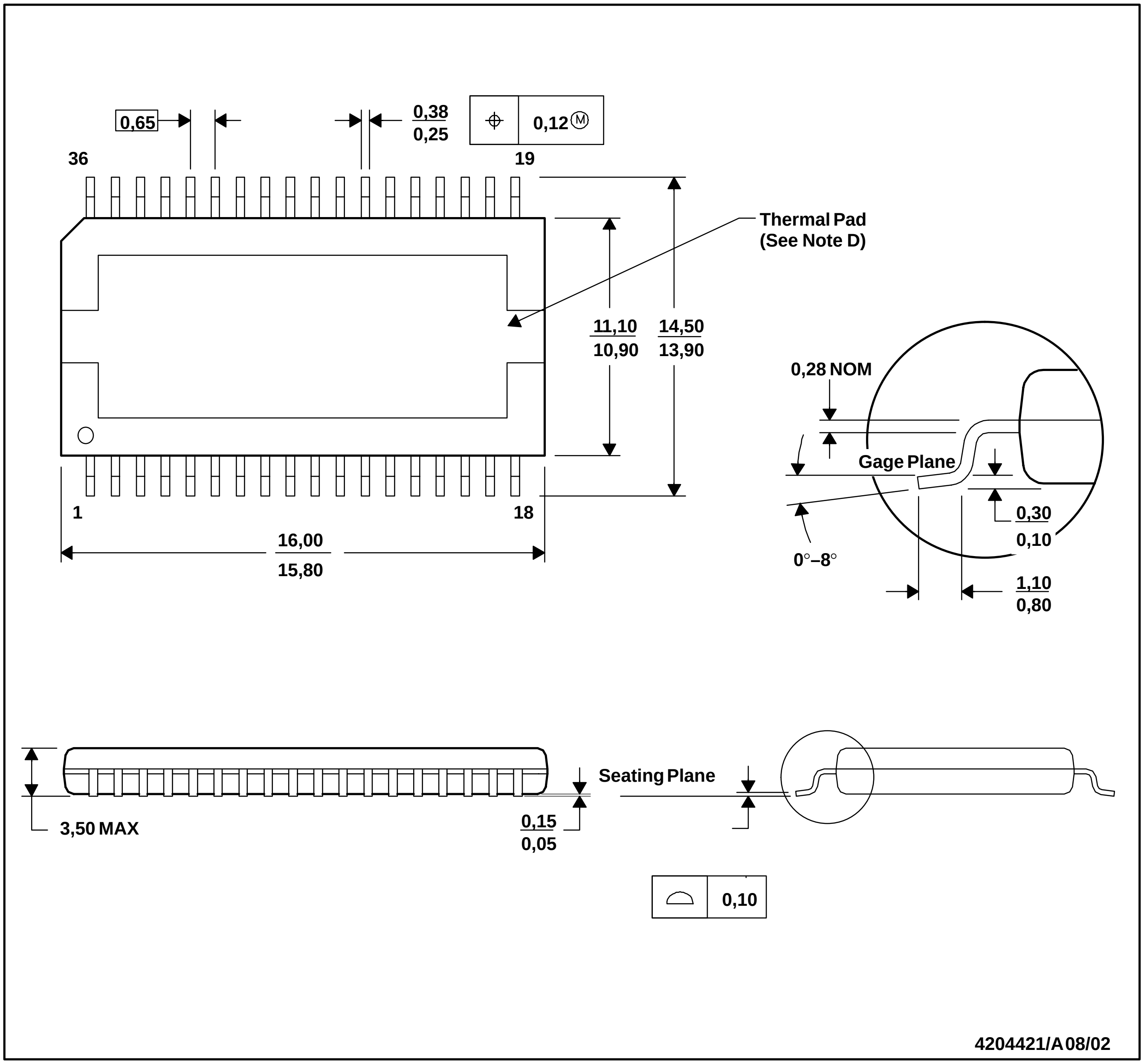
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

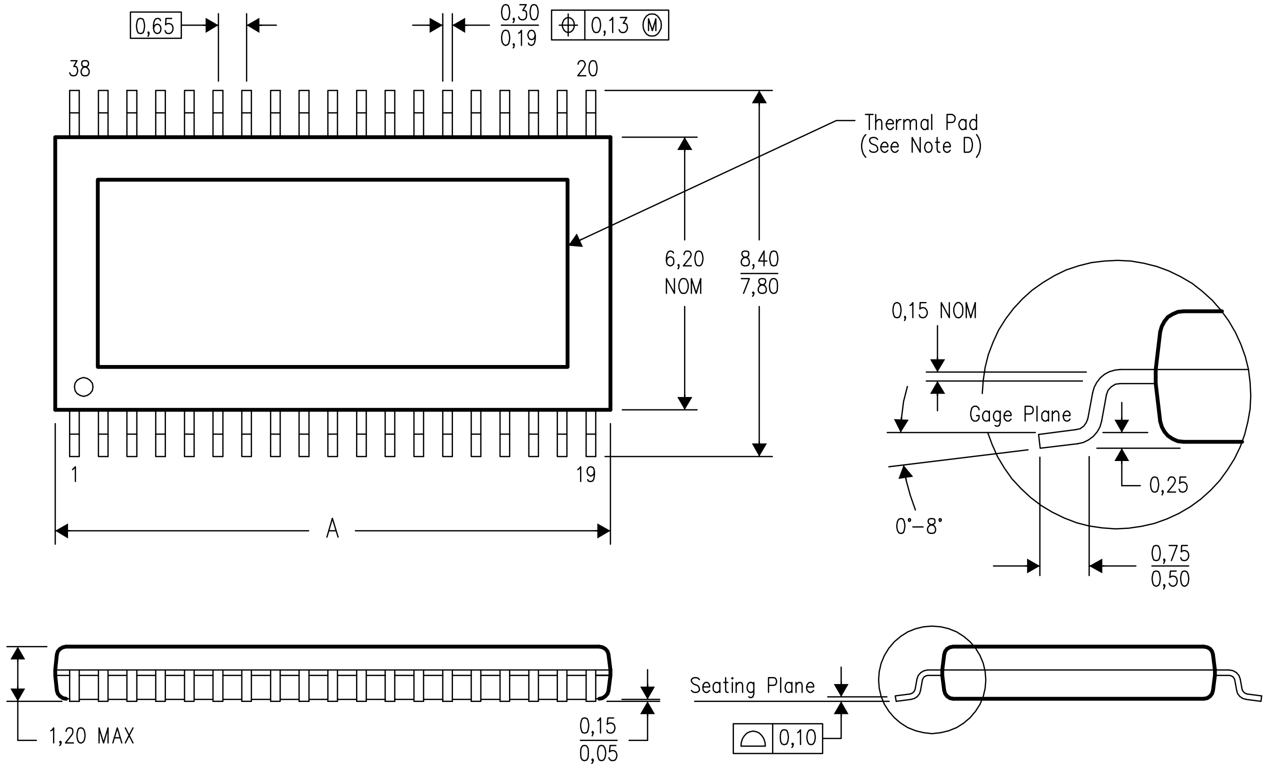
DKD (R-PDSO-G36) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-166
F. Falls within JEDEC MO-153

DAD (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE (DIE DOWN)

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

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