PLESSEY
Semiconductors

T-45-19-05

SP8743A 450MHz ÷ 8/9
SP8743B 500MHz ÷ 8/9

The SP8743 is an ECL counter with ECL 10K compatible outputs. It divides by 8 when either control input is in the high state and by 9 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

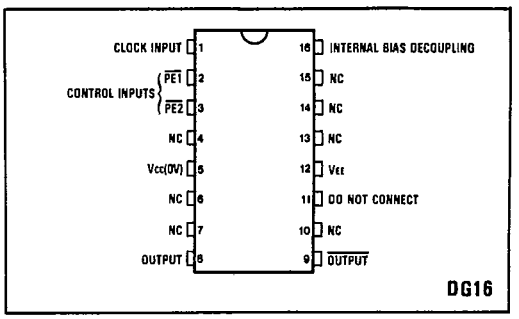

Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

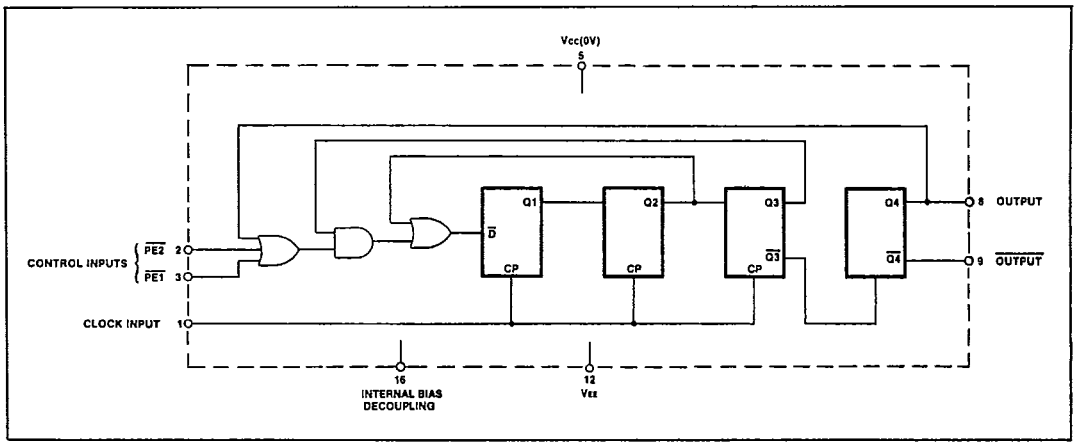

Fig.2 Function diagram

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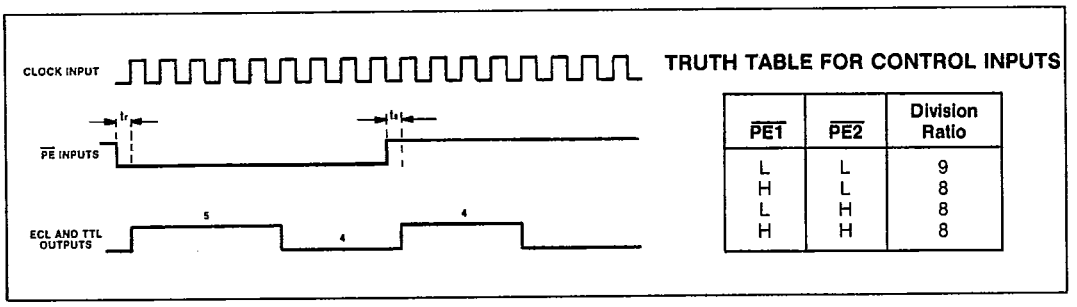
ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency	f_{max}	450		MHz	A	Input = 400 - 800mV p-p	Note 4
sinewave input		500		MHz	B	Input = 400 - 800mV p-p	Note 4
Minimum frequency	f_{min}		40	MHz	Both	Input = 400 - 800mV p-p	Note 5
sinewave input							
Power supply current	I_{EE}		60	mA	Both	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	Both	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	Both	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	Both	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	Both	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		6	ns	Both		Note 5
Set-up time	t_s	1		ns	Both		Note 5
Release time	t_r	2.5		ns	Both		Note 5

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at low and high temperature only (not at 25°C)
5. Guaranteed but not tested.
6. Tested at 25°C only.

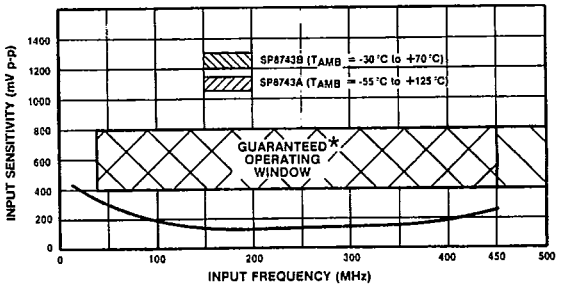


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.3 Timing diagram

NOTE
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷9 mode is obtained.



*Tested as specified in Table of Electrical Characteristics

Fig.4 Typical input characteristics of SP8743

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OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\bar{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8743 varies as a function of frequency. See Fig. 5.

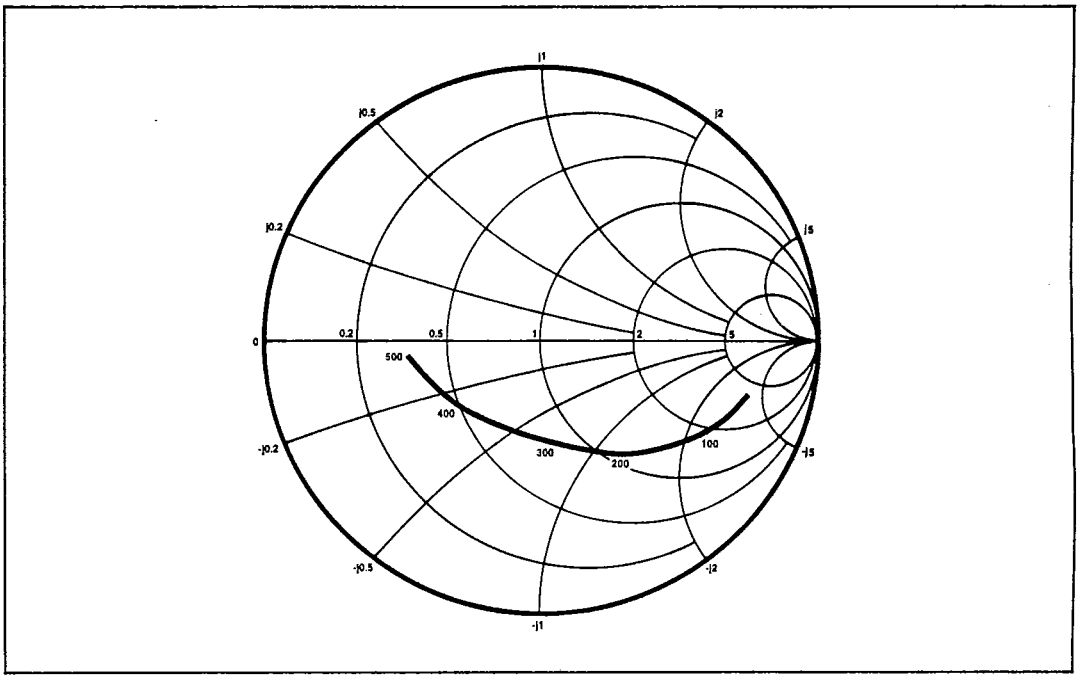

Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

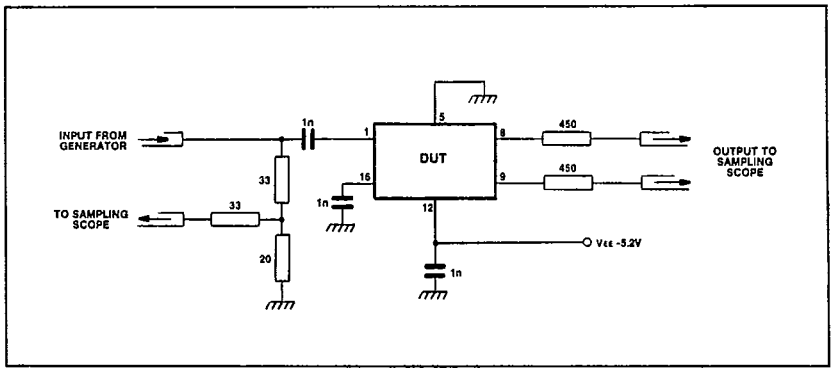

Fig.6 Test circuit

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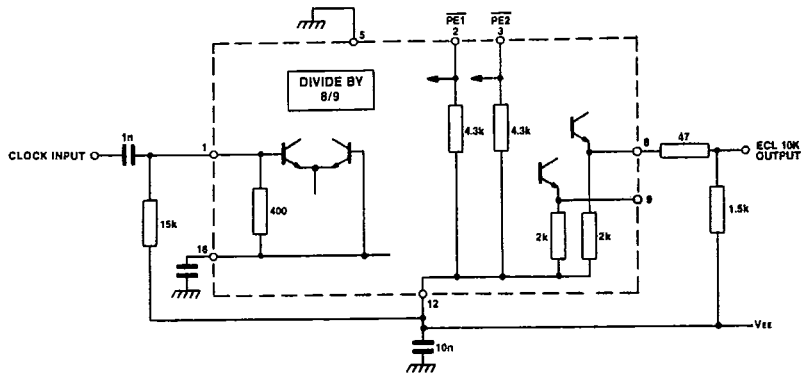

Fig.7 Typical applications circuit showing interfacing