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- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant

description/ordering information

This 20-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B-port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC20T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

	(TOP VI	EW)
1DIR [1 0	56	1 <u>0E</u>
1B1 [2	55	1A1
1B2 [3	54	1A2
GND [4	53	GND
1B3 [5	52	1A3
1B4 [6	51	1A4
V _{CCB} [7	50	VCCA
1B5 [8	49	1A5
1B6 [9	48	1A6
1B7 [10	47	1A7
GND [11	46	GND
1B8 [12	45	1A8
1B9 [13	44	1A9
1B10[14	43	1A10
2B1 [15	42	2A1
2B2 [16	41	2A2
2B3 [17	40	2A3
GND [18	39	GND
2B4 [19	38	2A4
2B5 [20	37	2A5
2B6 [21	36	2A6
V _{CCB} [22	35	V _{CCA}
2B7 [23	34	2A7
2B8 [24	33	2A8
GND [25	32	GND
2B9 [26	31	2A9
2B10[27	30	2 <u>A1</u> 0
2DIR [28	29	2OE

DGG OR DGV PACKAGE

The SN74AVC20T245 is designed so that the control (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) inputs are supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	TSSOP – DGG	Tape and reel	SN74AVC20T245DGGR	TBD
-40°C to 85°C	TVSOP – DGV	Tape and reel	SN74AVC20T245DGVR	TBD
	VFBGA – GQL	Tape and reel	SN74AVC20T245GQLR	TBD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



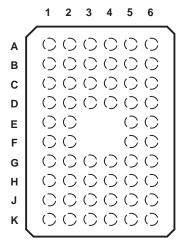
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL PACKAGE (TOP VIEW)



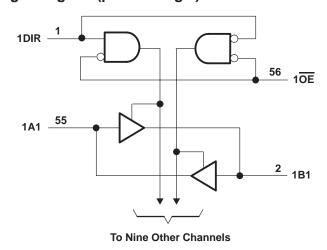
terminal assignments

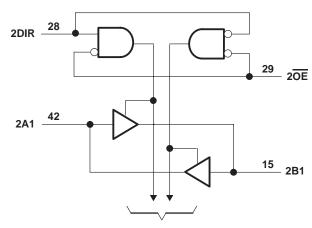
	1	2	3	4	5	6
Α	1B1	1B2	1DIR	1OE	1A2	1A1
В	1B3	1B4	GND	GND	1A4	1A3
С	1B5	1B6	VCCB	VCCA	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
Е	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
Н	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	2OE	2A10	2A9

FUNCTION TABLE (each 10-bit section)

INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

logic diagram (positive logic)





To Nine Other Channels

Pin numbers shown are for the DGG and DGV packages.



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CCA} and V _{CCB}	
Voltage range applied to any output in the high-impedance or power-off state, V _O	
(see Note 1): A port	–0.5 V to 4.6 V
B port	0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V _O	
(see Notes 1 and 2): A port	$-0.5 \text{ V to V}_{CCA} + 0.5 \text{ V}$
B port	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	
Continuous output current, I _O	
Continuous current through each V _{CCA} , V _{CCB} , and GND	
Package thermal impedance, θ _{JA} (see Note 3): DGG package	
DGV package	
GQL package	
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Notes 4 through 6)

			VCCI	Vcco	MIN	MAX	UNIT
VCCA	Supply voltage				1.4	3.6	V
VCCB	Supply voltage				1.4	3.6	V
			1.4 V to 1.95 V		V _{CCI} × 0.65		
ViH	High-level input voltage	Data inputs	1.95 V to 2.7 V		1.6		V
	voltage		2.7 V to 3.6 V		2		
			1.4 V to 1.95 V			V _{CCI} × 0.35	
٧ _{IL}	Low-level input voltage	Data inputs	1.95 V to 2.7 V			0.7	V
	Voltage		2.7 V to 3.6 V			0.8	
		_	1.4 V to 1.95 V		V _{CCA} × 0.65		
ViH	High-level input voltage	DIR and OE	1.95 V to 2.7 V		1.6		V
	voltage	(Referenced to V _{CCA})	2.7 V to 3.6 V		2		
		_	1.4 V to 1.95 V			V _{CCA} × 0.35	
٧ _{IL}	Low-level input voltage		1.95 V to 2.7 V			0.7	V
	vollage		2.7 V to 3.6 V			0.8	
.,	Outrotouthous	Active state			0	Vcco	V
VO	Output voltage	3-state			0	3.6	V
VI	Input voltage				0	3.6	V
				1.4 V to 1.6 V		-6	
				1.65 V to 1.95 V		-8	1.
ІОН	High-level output curre	ent		2.3 V to 2.7 V		-9	mA
				3 V to 3.6 V		-12	
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	1.
loL	Low-level output curre	nt		2.3 V to 2.7 V		9	mA
				3 V to 3.6 V		12	
Δt/Δν	Input transition rise or	fall rate				5	ns/V
TA	Operating free-air tem	perature			-40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.

- 5. V_{CCO} is the V_{CC} associated with the output port.
- All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 7 and 8)

PA	RAMETER	TEST CON	DITIONS	V _{CCA}	V _{ССВ}	MIN	TYP [†]	MAX	UNIT
		I _{OH} = -100 μA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	Vcco.	-0.2		
		I _{OH} = -6 mA	$V_I = V_{IH}$	1.4 V	1.4 V	TBD			
Vон		IOH = -8 mA	VI = VIH	1.65 V	1.65 V	1.2			V
		IOH = -9 mA	VI = VIH	2.3 V	2.3 V	1.75			
		I _{OH} = −12 mA	$V_I = V_{IH}$	3 V	3 V	2.3			
		I _{OL} = 100 μA	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	
		I _{OL} = 6 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	
VOL		$I_{OL} = 8 \text{ mA}$	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	V
		I _{OL} = 9 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.55	
		I _{OL} = 12 mA	$V_I = V_{IL}$	3 V	3 V			0.7	
Тį	Control inputs	$V_I = V_{CCA}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	μΑ
	A port	\\. 0 \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \		0 V	0 to 3.6 V			±10	^
loff	B port	V_I or $V_O = 0$ to 3.6 V		0 to 3.6 V	0 V			±10	μΑ
	A or B ports		OE = V _{IH}	3.6 V	3.6 V		±2.5	±5	
loz‡	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	OE = don't care	0 V	3.6 V		±2.5	±5	μА
	A port	11 1001 11 111		3.6 V	0 V		±2.5	±5	
				1.6 V	1.6 V			8	
				1.95 V	1.95 V			9	
١.		LV V - OND		2.7 V	2.7 V			13	
ICCA		$V_I = V_{CCI}$ or GND,	IO = 0	0 V	3.6 V			-1	μΑ
				3.6 V	0 V			12	
				3.6 V	3.6 V			20	
				1.6 V	1.6 V			8	
				1.95 V	1.95 V			9	
		W. Waaran CND	1- 0	2.7 V	2.7 V			13	
ІССВ		$V_I = V_{CCI}$ or GND,	IO = 0	0 V	3.6 V			12	μΑ
				3.6 V	0 V			-1	
				3.6 V	3.6 V			20	
I _{CCA} + (see Ta		$V_I = V_{CCI}$ or GND,	IO = 0	1.4 V to 3.6 V	1.4 V to 3.6 V			TBD	μΑ
C _i	Control inputs	$V_I = 3.3 \text{ V or GND}$		3.3 V	3.3 V				pF
C _{io}	A or B ports	$V_O = 3.3 \text{ V or GND}$		3.3 V	3.3 V				pF

 $[\]uparrow$ All typical values are at $T_A = 25^{\circ}$ C.



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

NOTES: 7. V_{CCO} is the V_{CC} associated with the output port.

8. V_{CCI} is the V_{CC} associated with the input port.

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switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.5 V \pm 0.1 V (see Figure 1)

PARAMETER	FROM	TO	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
^t PLH	^	В									20	
^t PHL	Α	Ь									ns	
^t PLH	В	۸									20	
^t PHL	Ь	А									ns	
^t PZH	ŌĒ	۸									20	
^t PZL	OE	Α									ns	
^t PZH	ŌĒ	В										
^t PZL	OE	В									ns	
^t PHZ	ŌĒ	٨									20	
tPLZ	OE	Α									ns	
^t PHZ	ŌĒ	В								·	ne	
t _{PLZ}	OE .	В									ns	

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V \pm 0.15 V (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CCB} = ± 0.7	: 1.5 V I V	V _{CCB} = ± 0.1	= 1.8 V 5 V	VCCB ± 0.	= 2.5 V 2 V	V _{CCB} = ± 0.5	= 3.3 V 3 V	UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	^	В									20
^t PHL	А	В									ns
t _{PLH}	В	^									
^t PHL	В	Α									ns
^t PZH	<u>OE</u>	^									
t _{PZL}	ÜE	А									ns
^t PZH	<u>OE</u>	В									20
t _{PZL}	ÜE	Ь									ns
^t PHZ	<u>OE</u>	٨									20
t _{PLZ}	OE	Α									ns
^t PHZ	ŌĒ	В									ns
t _{PLZ}	OE .	В									115



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switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V \pm 0.2 V (see Figure 1)

PARAMETER	AMETER FROM TO (INPUT) (OUTPUT)		V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = ± 0.		V _{CCB} = ± 0.5		UNIT		
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	^	В									
t _{PHL}	Α	Ь									ns
t _{PLH}	В	٨									
t _{PHL}	В	Α									ns
^t PZH	ŌĒ	^									
t _{PZL}	OE	А									ns
^t PZH	<u>OE</u>	В									
tPZL	OE	В									ns
^t PHZ	ŌĒ	^									
tPLZ	OE	Α									ns
^t PHZ	ŌĒ	В									ns
t _{PLZ}	OE .	В									115

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V \pm 0.3 V (see Figure 1)

PARAMETER	PARAMETER FROM		V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} =		V _{CCB} = ± 0.5		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	^	В									20
^t PHL	Α	Ь									ns
t _{PLH}	В	^									
^t PHL	В	Α									ns
^t PZH	<u>OE</u>	٨									
t _{PZL}	OE	Α									ns
^t PZH	<u>OE</u>	В									20
t _{PZL}	OE	Ь									ns
^t PHZ	<u>OE</u>	٨									20
t _{PLZ}	OE	Α									ns
^t PHZ	ŌĒ	В									ns
t _{PLZ}	OE .	В								·	115

operating characteristics, V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Power dissipation capacitance per transceiver,	Outputs enabled			
	A port input, B port output	Outputs disabled	0. 0. 4.0 MHz		
C _{pdA}	Power dissipation capacitance per transceiver,	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$		pF
	B port input, A port output	Outputs disabled]		
	Power dissipation capacitance per transceiver,	Outputs enabled			
	A port input, B port output	Outputs disabled	$C_1 = 0$, $f = 10 \text{ MHz}$		
C _{pdB}	Power dissipation capacitance per transceiver,	Outputs enabled	$C_L = 0$, $f = 10 \text{ MHz}$		pF
	B port input, A port output	Outputs disabled]		



typical total static power consumption (I_{CCA} and I_{CCB})

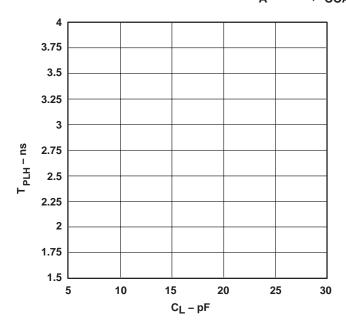
V		UNIT			
VCCB	1.5 V	1.8 V	2.5 V	3.3 V	UNII
1.5 V	TBD	TBD	TBD	TBD	nA
1.8 V	TBD	TBD	TBD	TBD	
2.5 V	TBD	TBD	TBD	TBD	
3.3 V	TBD	TBD	TBD	TBD	

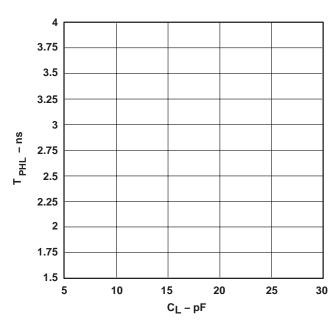
TABLE 1



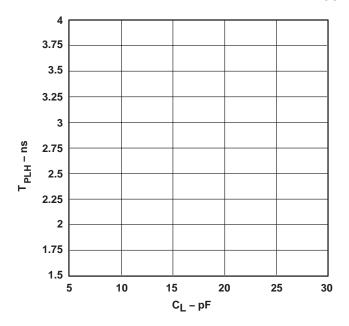
TYPICAL CHARACTERISTICS

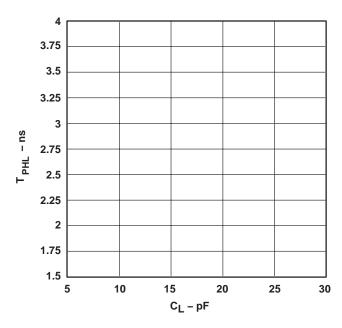
TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, $T_A = 25^{\circ}C, V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$



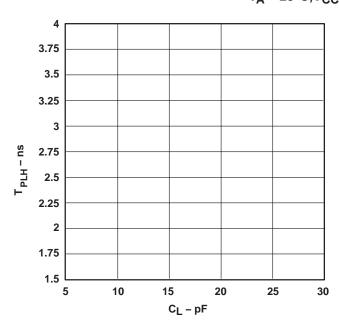


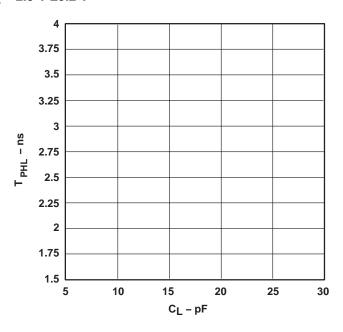
TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, $T_A = 25^{\circ}\text{C}, V_{CCA} = 1.8~\text{V} \pm 0.15~\text{V}$



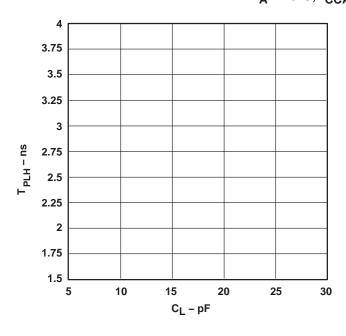


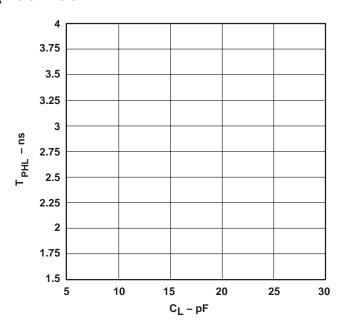
TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, $T_A = 25^{\circ}C, V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$





TYPICAL PROPAGATION DELAY vs LOAD CAPACITANCE, $T_A = 25^{\circ}C, V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

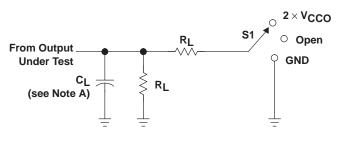




SN74AVC20T245

VCCA

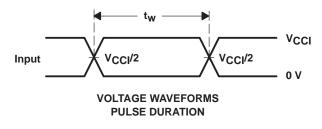
PARAMETER MEASUREMENT INFORMATION

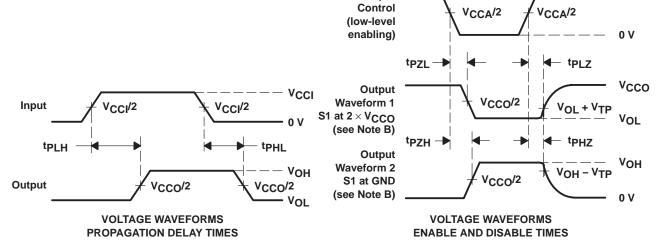


TEST	S1	
tpd	Open	
t _{PLZ} /t _{PZL}	2×V _{CCO}	
tPHZ/tPZH	GND	

LOAD CIRCUIT

VCCO	CL	RL	V _{TP}
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V





Output

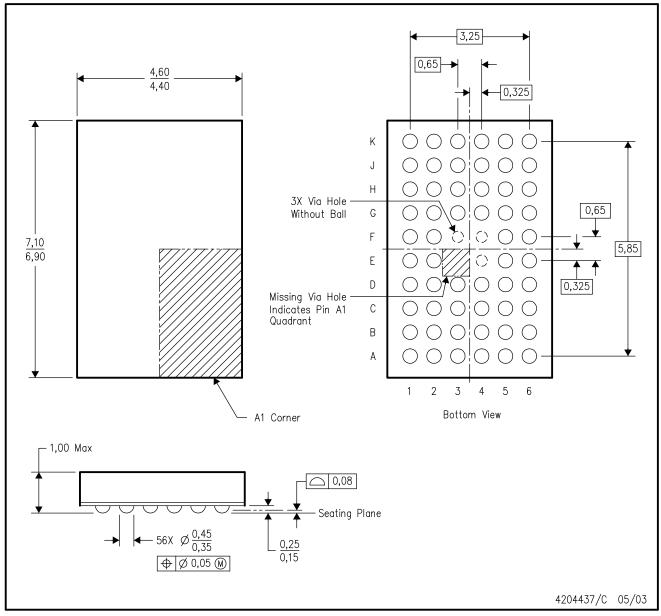
- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq$ 1 V/ns, $dv/dt \geq$ 1 V/ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. tpLH and tpHL are the same as tpd.
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. VCCO is the VCC associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms



ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ BGA configuration.
- D. Falls within JEDEC MO-225 variation BA.
- E. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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