- **Organization: 16 777 216 x 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz Systems**
- **JEDEC 144-Pin Small Outline Dual-In-Line Memory Module (SODIMM) Without Buffer for Use With Socket**
- **Uses Sixteen 64M-Bit Synchronous Dynamic RAMs (SDRAMs) (8M × 8-Bit) Memory Chips Assembled in Board-On-Chip/Ball-Grid-Array (BOC/BGA™) Packages.**
- **Byte-Read/Write Capability**
- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Performance Ranges:**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Four Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence Detect (SPD) Using EEPROM**

| | SYNCHRONOUS CLOCK CYCLE TIME | | ACCESS TIME CLOCK TO OUTPUT | | REFRESH INTERVAL |
|---|---|---|---|---|---|
| | $t_{CK3}$ | $t_{CK2}$ | $t_{AC3}$ | $t_{AC2}$ | $t_{REF}$ |
| TM16SM64JBN–10 | 10 ns | 15 ns | 7.5 ns | 7.5 ns | 64 ms |

PRODUCT PREVIEW

## description

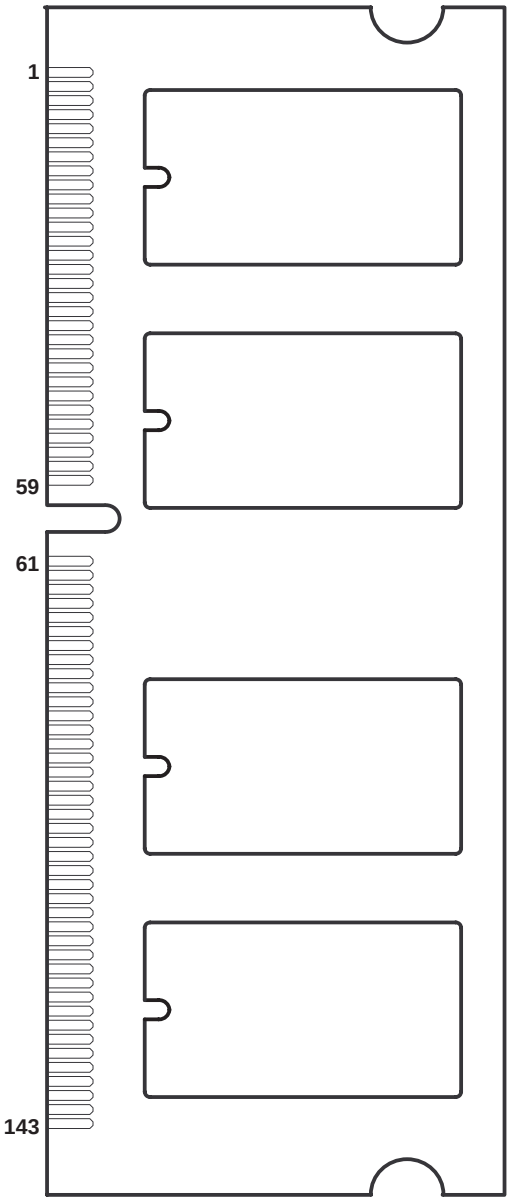
The TM16SM64JBN is a 64M-byte, 144-pin SODIMM. The SODIMM is composed of sixteen TMS664814DGE, 8 388 608 x 8-bit SDRAMs, two per board-on-chip/ball-grid-array (BOC/BGA) package mounted on a substrate with decoupling capacitors. See the TMS664814 data sheet (literature number SMOS695).

## operation

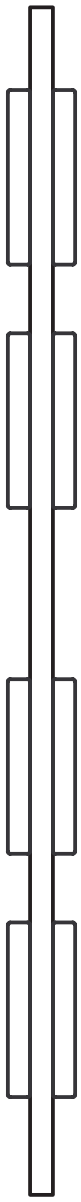
The TM16SM64JBN operates as sixteen TMS664814DGE devices that are connected as shown in the TM16SM64JBN functional block diagram.

PRODUCT PREVIEW

**DUAL-IN-LINE MEMORY MODULE (TOP VIEW)**




**TM16SM64JBN (SIDE VIEW)**



**PIN NOMENCLATURE**

| | |
|---|---|
| A[0:11] | Row-Address Inputs |
| A[0:8] | Column-Address Inputs |
| A13/BA0 | Bank-Select Zero |
| A12/BA1 | Bank-Select One |
| $\overline{CAS}$ | Column-Address Strobe |
| CKE[0:1] | Clock Enable |
| CK[0:3] | System Clock |
| DQ[0:63] | Data-In / Data Out |
| DQMB[0:7] | Data-In/Data-Out Mask Enable |
| $\overline{NC}$ | No Connect |
| $\overline{RAS}$ | Row-Address Strobe |
| $\overline{S}$[0:1] | Chip-Select |
| SCL | SPD Clock |
| SDA | SPD Address / Data |
| $V_{DD}$ | 3.3-V Supply |
| $V_{SS}$ | Ground |
| $\overline{WE}$ | Write Enable |

## Pin Assignments

| PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 37 | DQ8 | 73 | NC | 109 | A9 |
| 2 | $V_{SS}$ | 38 | DQ40 | 74 | CK1 | 110 | A12/BA1 |
| 3 | DQ0 | 39 | DQ9 | 75 | $V_{SS}$ | 111 | A10 |
| 4 | DQ32 | 40 | DQ41 | 76 | $V_{SS}$ | 112 | A11 |
| 5 | DQ1 | 41 | DQ10 | 77 | NC | 113 | $V_{DD}$ |
| 6 | DQ33 | 42 | DQ42 | 78 | NC | 114 | $V_{DD}$ |
| 7 | DQ2 | 43 | DQ11 | 79 | NC | 115 | DQMB2 |
| 8 | DQ34 | 44 | DQ43 | 80 | NC | 116 | DQMB6 |
| 9 | DQ3 | 45 | $V_{DD}$ | 81 | $V_{DD}$ | 117 | DQMB3 |
| 10 | DQ35 | 46 | $V_{DD}$ | 82 | $V_{DD}$ | 118 | DQMB7 |
| 11 | $V_{DD}$ | 47 | DQ12 | 83 | DQ16 | 119 | $V_{SS}$ |
| 12 | $V_{DD}$ | 48 | DQ44 | 84 | DQ48 | 120 | $V_{SS}$ |
| 13 | DQ4 | 49 | DQ13 | 85 | DQ17 | 121 | DQ24 |
| 14 | DQ36 | 50 | DQ45 | 86 | DQ49 | 122 | DQ56 |
| 15 | DQ5 | 51 | DQ14 | 87 | DQ18 | 123 | DQ25 |
| 16 | DQ37 | 52 | DQ46 | 88 | DQ50 | 124 | DQ57 |
| 17 | DQ6 | 53 | DQ15 | 89 | DQ19 | 125 | DQ26 |
| 18 | DQ38 | 54 | DQ47 | 90 | DQ51 | 126 | DQ58 |
| 19 | DQ7 | 55 | $V_{SS}$ | 91 | $V_{SS}$ | 127 | DQ27 |
| 20 | DQ39 | 56 | $V_{SS}$ | 92 | $V_{SS}$ | 128 | DQ59 |
| 21 | $V_{SS}$ | 57 | NC | 93 | DQ20 | 129 | $V_{DD}$ |
| 22 | $V_{SS}$ | 58 | NC | 94 | DQ52 | 130 | $V_{DD}$ |
| 23 | DQMB0 | 59 | NC | 95 | DQ21 | 131 | DQ28 |
| 24 | DQMB4 | 60 | NC | 96 | DQ53 | 132 | DQ60 |
| 25 | DQMB1 | 61 | CK0 | 97 | DQ22 | 133 | DQ29 |
| 26 | DQMB5 | 62 | CKE0 | 98 | DQ54 | 134 | DQ61 |
| 27 | $V_{DD}$ | 63 | $V_{DD}$ | 99 | DQ23 | 135 | DQ30 |
| 28 | $V_{DD}$ | 64 | $V_{DD}$ | 100 | DQ55 | 136 | DQ62 |
| 29 | A0 | 65 | $\overline{RAS}$ | 101 | $V_{DD}$ | 137 | DQ31 |
| 30 | A3 | 66 | $\overline{CAS}$ | 102 | $V_{DD}$ | 138 | DQ63 |
| 31 | A1 | 67 | $\overline{WE}$ | 103 | A6 | 139 | $V_{SS}$ |
| 32 | A4 | 68 | CEK1 | 104 | A7 | 140 | $V_{SS}$ |
| 33 | A2 | 69 | $\overline{S0}$ | 105 | A8 | 141 | SDA |
| 34 | A5 | 70 | NC | 106 | A13/BA0 | 142 | SCL |
| 35 | $V_{SS}$ | 71 | $\overline{S1}$ | 107 | $V_{SS}$ | 143 | $V_{DD}$ |
| 36 | $V_{SS}$ | 72 | NC | 108 | $V_{SS}$ | 144 | $V_{DD}$ |

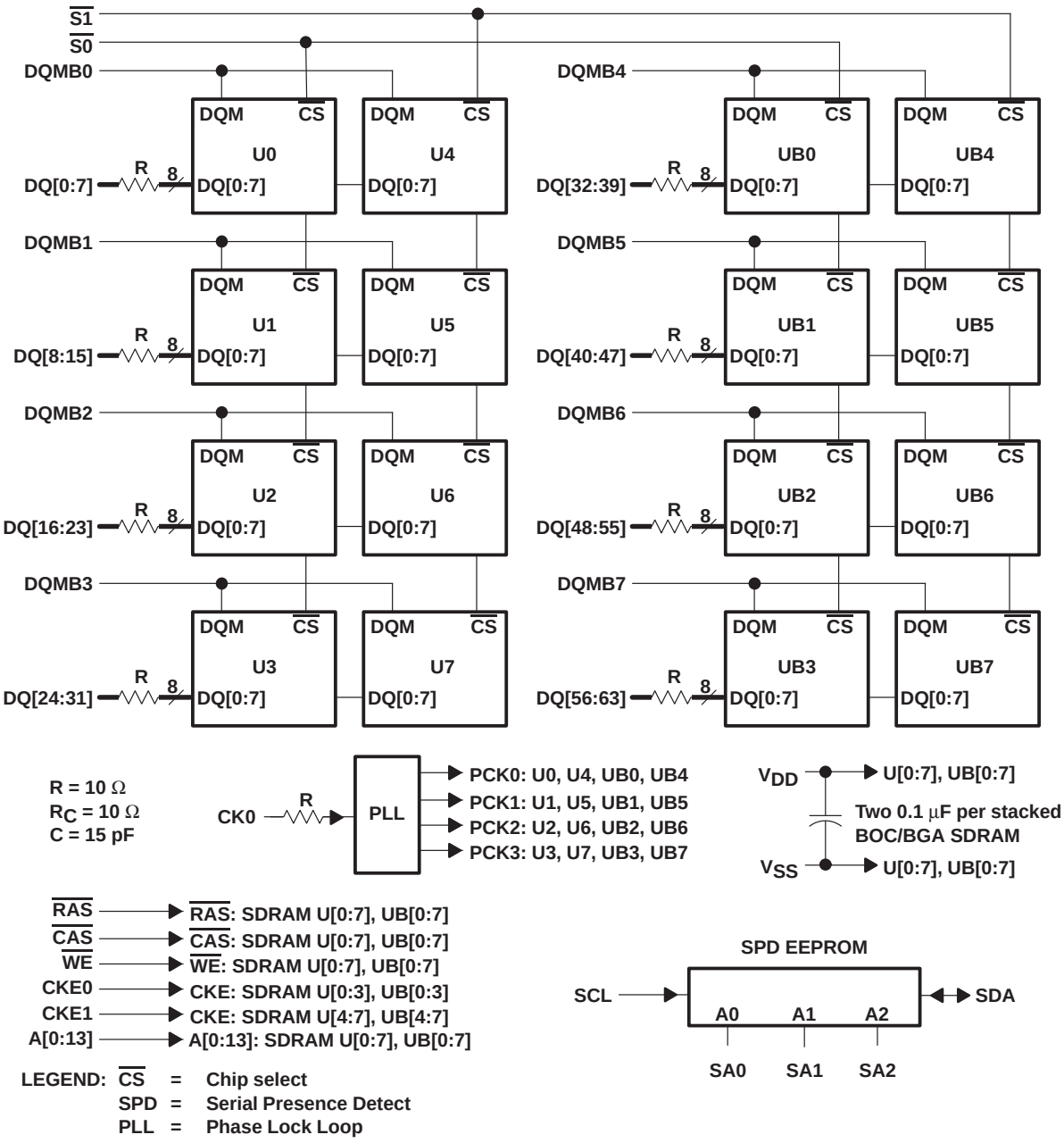
PRODUCT PREVIEW

## small-outline dual-in-line memory module and components

The small-outline dual-in-line memory module and components include:

- PC substrate: 1,10 ± 0,1 mm (0.04 inch) nominal thickness
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

## functional block diagram




NOTES: A. Ux devices are mounted on the top side and UBx devices are mounted on the bottom side of the module.
B. U[0:3] and UB[0:3] are located on top of the stack and U[4:7] and UB[4:7] are located on bottom of the stack.
C. DQMBx is connected to a single stacked device.

### absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ . . . . . –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 16 W
Ambient temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to $V_{SS}$.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_{IH}$ | High-level input voltage | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IH-SPD}$ | High-level input voltage for SPD device | 2 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | –0.3 | | 0.8 | V |
| $T_A$ | Ambient temperature | 0 | | 70 | °C |

### capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

| PARAMETER | | TM16SM64JBN | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $C_{i(CK)}$ | Input capacitance, CK input | | 35 | pF |
| $C_{i(AC)}$ | Input capacitance, address and control inputs: A0–A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | | 50 | pF |
| $C_{i(CKE)}$ | Input capacitance, CKE input | | 50 | pF |
| $C_o$ | Output capacitance | | 20 | pF |
| $C_{i(DQMBx)}$ | Input capacitance, DQMBx input | | 20 | pF |
| $C_{i(Sx)}$ | Input capacitance, $\overline{Sx}$ input | | 50 | pF |
| $C_{i/o(SDA)}$ | Input/output capacitance, SDA input | | 12 | pF |
| $C_{i(SPD)}$ | Input capacitance, SPD inputs (except SDA) | | 10 | pF |

NOTE 2: $V_{DD}$ = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

PRODUCT PREVIEW

## electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

| PARAMETER | | TEST CONDITIONS | | '16SM64JBN-10 MIN | '16SM64JBN-10 MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = – 2 mA | | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_I$ | Input current (leakage) | 0 V < $V_I$ < $V_{DD}$ + 0.3 V, All other pins = 0 V to $V_{DD}$ | | | ±10 | µA |
| $I_O$ | Output current (leakage) | 0 V < $V_O$ < $V_{DD}$ +0.3 V, Output disabled | | | ±10 | µA |
| $I_{CC1}$ | Operating current | Burst length = 1, $t_{RC} \geq t_{RC}$ MIN, $I_{OH}/I_{OL}$ = 0 mA, (see Notes 4, 5, and 6) | CAS latency = 2 | | 860 | mA |
| | | | CAS latency = 3 | | 920 | mA |
| $I_{CC2P}$ | Precharge standby current in power-down mode | CKE ≤ $V_{IL}$ MAX, $t_{CK}$ = 15 ns (see Note 7) | | | 16 | mA |
| $I_{CC2PS}$ | | CKE and CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Note 8) | | | 16 | |
| $I_{CC2N}$ | Precharge standby current in non-power-down mode | CKE ≥ $V_{IH}$ MIN, $t_{CK}$ = 15 ns (see Note 7) | | | 640 | mA |
| $I_{CC2NS}$ | | $t_{CK}$ = infinite (see Note 8) | | | 80 | |
| $I_{CC3P}$ | Active standby current in power-down mode | CKE ≤ $V_{IL}$ MAX, $t_{CK}$ = 15 ns (see Notes 4 and 7) | | | 80 | mA |
| $I_{CC3PS}$ | | CKE and CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Notes 4 and 8) | | | 80 | |
| $I_{CC3N}$ | Active standby current in non-power-down mode | CKE ≥ $V_{IH}$ MIN, $t_{CK}$ = 15 ns (see Notes 4 and 7) | | | 880 | mA |
| $I_{CC3NS}$ | | CKE ≥ $V_{IH}$ MIN, CK ≤ $V_{IL}$ MAX, $t_{CK}$ = ∞ (see Notes 4 and 8) | | | 160 | |
| $I_{CC4}$ | Burst current | Page burst, $I_{OH}/I_{OL}$ = 0 mA All banks activated, $n_{CCD}$ = one cycle (see Notes 9 and 10) | CAS latency = 2 | | 976 | mA |
| | | | CAS latency = 3 | | 1416 | |
| $I_{CC5}$ | Auto-refresh current | $t_{RC} \leq t_{RC}$ MIN (see Notes 5 and 8) | CAS latency = 2 | | 1280 | mA |
| | | | CAS latency = 3 | | 1280 | |
| $I_{CC6}$ | Self-refresh current | CKE ≤ $V_{IL}$ MAX | | | 32 | mA |

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Only one bank is activated.
5. $t_{RC} \geq$ MIN
6. Control and address inputs change state twice during $t_{RC}$.
7. Control and address inputs change state once every 30 ns.
8. Control and address inputs do not change state (stable).
9. Control and address inputs change once every cycle.
10. Continuous burst access, $n_{CCD}$ = 1 cycle

PRODUCT PREVIEW

## ac timing requirements†‡

| | | | '16SM64JBN-10 | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{CK2}$ | Cycle time, CK | CAS latency = 2 | 15 | | ns |
| $t_{CK3}$ | Cycle time, CK | CAS latency = 3 | 10 | | ns |
| $t_{CH}$ | Pulse duration, CK high | | 3 | | ns |
| $t_{CL}$ | Pulse duraction, CK low | | 3 | | ns |
| $t_{AC2}$ | Access time, CK high to data out (see Note 11) | CAS latency = 2 | | 7.5 | ns |
| $t_{AC3}$ | Access time, CK high to data out (see Note 11) | CAS latency = 3 | | 7.5 | ns |
| $t_{OH}$ | Hold time, CK high to data out | | 3 | | ns |
| $t_{LZ}$ | Delay time, CK high to DQ in low-impedance state (see Note 12) | | 2 | | ns |
| $t_{HZ}$ | Delay time, CK high to DQ in high-impedance state (see Note 13) | | | 10 | ns |
| $t_{IS}$ | Setup time, address, control, and data input | | 2 | | ns |
| $t_{IH}$ | Hold time, address, control, and data input | | 1 | | ns |
| $t_{CESP}$ | Power down/self-refresh exit time | | 8 | | ns |
| $t_{RAS}$ | Delay time, ACTV command to DEAC or DCAB command | | 50 | 100000 | ns |
| $t_{RC}$ | Delay time, ACTV, MRS, REFR, or SLFR to ACTV, MRS, REFR,or SLFR command | | 80 | | ns |
| $t_{RCD}$ | Delay time ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 14) | | 30 | | ns |
| $t_{RP}$ | Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command | | 30 | | ns |
| $t_{RRD}$ | Delay time, ACTV command in one bank to ACTV command in the other bank | | 20 | | ns |
| $t_{RSA}$ | Delay time, MRS command to ACTV, MRS, REFR,or SLFR command | | 20 | | ns |
| $t_{APR}$ | Final data out of READ-P operation to ACTV, MRS, SLFR,or REFR command | | $t_{RP} - (CL-1) * t_{CK}$ | | ns |
| $t_{APW}$ | Final data in of WRT-P operation to ACTV, MRS, SLFR,or REFR command | | $t_{RP} + 1\ t_{CK}$ | | ns |
| $t_T$ | Transition time | | 1 | 5 | ms |
| $t_{REF}$ | Refresh interval | | | 64 | ms |
| $n_{CCD}$ | Delay time, READ or WRT command to an interrupting command | | 1 | | cycles |
| $n_{CDD}$ | Delay time, CS low or high to input enabled or inhibited | | 0 | | cycles |
| $n_{CLE}$ | Delay time, CKE high or low to CLK enabled or disabled | | 1 | 1 | cycles |
| $n_{CWL}$ | Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P | | 1 | | cycles |
| $n_{DID}$ | Delay time, ENBL or MASK command to enabled or masked data in | | 0 | 0 | cycles |
| $n_{DOD}$ | Delay time, ENBL or MASK command to enabled or masked data out | | 2 | 2 | cycles |
| $n_{HZP2}$ | Delay time, DEAC or DCAB, command to DQ in high-impedance state | CAS latency = 2 | | 2 | cycles |
| $n_{HZP3}$ | Delay time, DEAC or DCAB, command to DQ in high-impedance state | CAS latency = 3 | | 3 | cycles |
| $n_{WR}$ | Delay time, final data in of WRT operation to DEAC or DCAB command | | 1 | | cycles |
| $n_{WCD}$ | Delay time, WRT command to first data in | | 0 | 0 | cycles |

† All references are made to the rising transition of CK unless otherwise noted.
‡ Specifications in this table represent a single SDRAM device.

NOTES: 11. $t_{AC}$ is referenced from the rising transition of CK that precedes the data-out cycle. For example, the first data out $t_{AC}$ is referenced from the rising transition of CK that is read latency (one cycle after the READ command). Access time is measured at output reference level 1.4 V.
12. $t_{LZ}$ is measured from the rising transition of CK that is read latency (one cycle after the READ command).
13. $t_{HZ}$ (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
14. For read or write operations with automatic deactivate, $t_{RCD}$ must be set to satisfy minimum $t_{RAS}$.

PRODUCT PREVIEW

## serial presence detect

The serial presence detect (SPD) is contained in a 256 byte serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see Table 1). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD standards. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details. Table 1 lists SPD contents as follows:

**Table 1. Serial Presence Detect Data**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM16SM64JBN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 0 | Defines number of bytes written into serial memory during module manufacturing | 128 bytes | 80h |
| 1 | Total number of bytes of SPD memory device | 256 bytes | 08h |
| 2 | Fundamental memory type (FPM, EDO, SDRAM, . . .) | SDRAM | 04h |
| 3 | Number of row addresses on this assembly | 12 | 0Ch |
| 4 | Number of column addresses on this assembly | 9 | 09h |
| 5 | Number of module rows on this assembly | 2 banks | 02h |
| 6 | Data width of this assembly | 64 bits | 40h |
| 7 | Data width continuation | | 00h |
| 8 | Voltage interface standard of this assembly | LVTTL | 01h |
| 9 | SDRAM cycle time at maximum supported CAS latency (CL), CL = X | $t_{CK}$ = 10 ns | A0h |
| 10 | SDRAM access from clock at CL = X | $t_{AC}$ = 7.5 ns | 75h |
| 11 | SODIMM configuration type (non-parity, parity, error correcting code [ECC]) | Non-Parity | 00h |
| 12 | Refresh rate/type | 15.6 µs/ self-refresh | 80h |
| 13 | SDRAM width, primary DRAM | x8 | 08h |
| 14 | Error-checking SDRAM data width | N/A | 00h |
| 15 | Minimum clock delay, back-to-back random column addresses | 1 CK cycle | 01h |
| 16 | Burst lengths supported | 1, 2, 4, and 8 | 0Fh |
| 17 | Number of banks on each SDRAM device | 4 banks | 04h |
| 18 | CAS latencies supported | 2, 3 | 06h |
| 19 | CS latency | 0 | 01h |
| 20 | Write latency | 0 | 01h |
| 21 | SDRAM module attributes | Non-buffered/ Non-registered | 00h |
| 22 | SDRAM device attributes: general | $V_{DD}$ tolerance = (±10%) Burst read/write, precharge all, auto precharge | 0Eh |
| 23 | Minimum clock cycle time at CL = X – 1 | $t_{CK}$ = 15 ns | F0h |
| 24 | Maximum data-access time from clock at CL = X – 1 | $t_{AC}$ = 7.5 ns | 75h |
| 25 | Minimum clock cycle time at CL = X – 2 | N/A | 00h |
| 26 | Maximum data-access time from clock at CL = X – 2 | N/A | 00h |

## serial presence detect (continued)

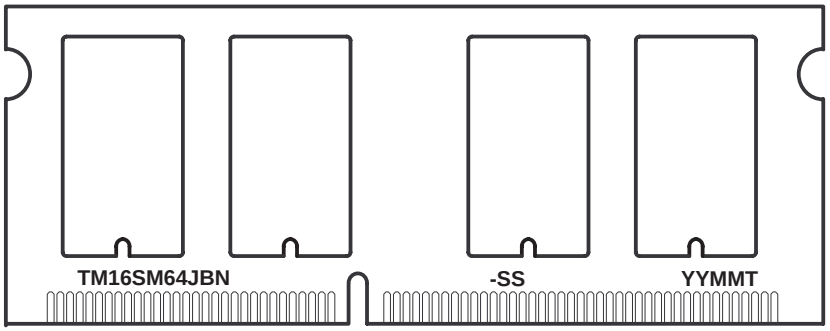
**Table 1. Serial Presence Detect Data (Continued)**

| BYTE NO. | DESCRIPTION OF FUNCTION | TM16SM64JBN-10 | |
|---|---|---|---|
| | | ITEM | DATA |
| 27 | Minimum row-precharge time | $t_{RP}$ = 30 ns | 1Eh |
| 28 | Minimum row-active to row-active delay | $t_{RRD}$ = 20 ns | 14h |
| 29 | Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay | $t_{RCD}$ = 30 ns | 1Eh |
| 30 | Minimum $\overline{RAS}$ pulse width | $t_{RAS}$ =50 ns | 32h |
| 31 | Density of each bank on module | 64M Bytes | 10h |
| 32 | Command and address signal input setup time | $t_{IS}$ = 2 ns | 20h |
| 33 | Command and address signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 34 | Data signal input setup time | $t_{IS}$ = 2 ns | 20h |
| 35 | Data signal input hold time | $t_{IH}$ = 1 ns | 10h |
| 36–61 | Superset features (may be used in the future) | | |
| 62 | SPD revision | Rev. 1.2 | 12h |
| 63 | Checksum for byte 0–62 | 19 | 13h |
| 64–71 | Manufacturer's JEDEC ID code per JEP–106E | 97h | 9700...00h |
| 72 | Manufacturing location† | TBD | |
| 73 | Manufacturer's part number | T | 54h |
| 74 | Manufacturer's part number | M | 4Dh |
| 75 | Manufacturer's part number | 1 | 31h |
| 76 | Manufacturer's part number | 6 | 36h |
| 77 | Manufacturer's part number | S | 53h |
| 78 | Manufacturer's part number | M | 4Dh |
| 79 | Manufacturer's part number | 6 | 36h |
| 80 | Manufacturer's part number | 4 | 34h |
| 81 | Manufacturer's part number | J | 4Ah |
| 82 | Manufacturer's part number | B | 42h |
| 83 | Manufacturer's part number | N | 4Eh |
| 84 | Manufacturer's part number | – | 2Dh |
| 85 | Manufacturer's part number | 1 | 31h |
| 86 | Manufacturer's part number | 0 | 30h |
| 87–90 | Manufacturer's part number | SPACE | 20h |
| 91 | Die revision code† | TBD | |
| 92 | PCB revision code† | TBD | |
| 93–94 | Manufacturing date† | TBD | |
| 95–98 | Assembly serial number† | TBD | |
| 99–125 | Manufacturer-specific data† | TBD | |
| 126 | Clock frequency | 66 MHz | 66h |
| 127 | SDRAM component and clock interconnection details | 199 | C7h |
| 128–166 | System-integrator's-specific data‡ | TBD | |
| 167–255 | Open | | |

† TBD indicates values that are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

## device symbolization



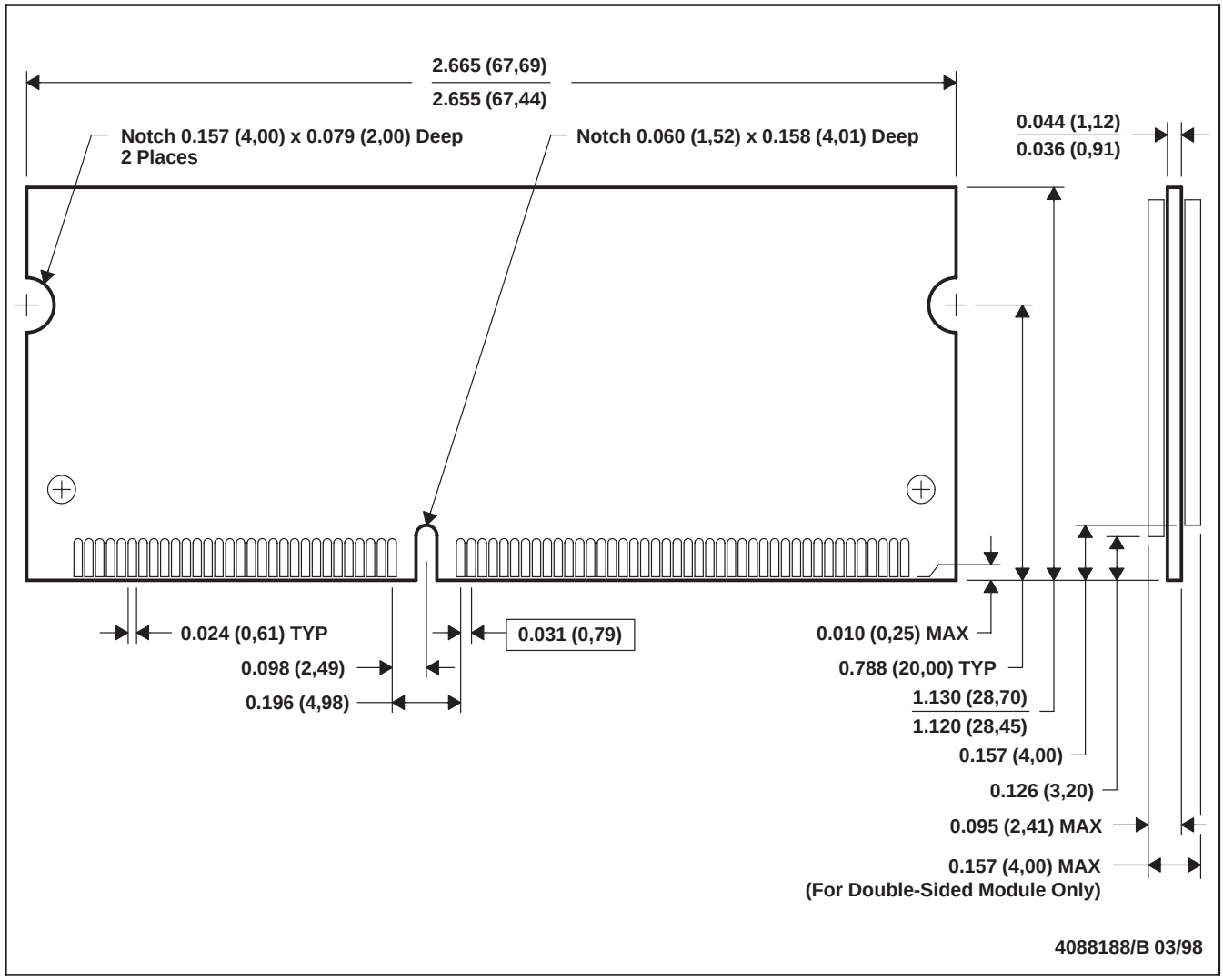

**YY = Year Code**
**MM = Month Code**
**T = Assembly Site Code**
**-SS = Speed Code**

NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

## MECHANICAL DATA

**BDQ (R-SODIMM-N144)** **SMALL OUTLINE DUAL IN-LINE MEMORY MODULE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-190

PRODUCT PREVIEW

## IMPORTANT NOTICE

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