- **Organization**
  - **TM4EN64xPU-xx . . . 4194304 × 64 Bits**
  - **TM8EN64xPU-xx . . . 8388608 × 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM4EN64xPU-xx — Utilizes Four 64M-Bit High-Speed (4M×16-Bit) Dynamic RAMs**
- **TM8EN64xPU-xx — Utilizes Eight 64M-Bit High-Speed (4M×16-Bit) Dynamic RAMs**
- **High-Speed, Low-Noise LVTTL Interface**
- **High-Reliability 50-Lead 400-Mil-Wide Surface-Mount Thin Small-Outline Package (TSOP) (DGE Suffix)**
- **Long Refresh Periods:**
  - **TMxEN64KPU: 64 ms (4096 Cycles)**
  - **TMxEN64NPU: 64 ms (8192 Cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Serial-Presence-Detect (SPD) Using EEPROM**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Performance Ranges**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	EDO CYCLE t_{HPC} (MIN)
'xEN64xPU–40	40 ns	11 ns	20 ns	16 ns
'xEN64xPU–50	50 ns	13 ns	25 ns	20 ns
'xEN64xPU–60	60 ns	15 ns	30 ns	25 ns

PRODUCT PREVIEW

description

The TM4EN64KPU is a 32M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of four TMS465169, 4194304 × 16-bit 4K-refresh EDO dynamic random-access memory (DRAM) devices, each in a 400-mil, 50-pin plastic thin small-outline package (TSOP) (DGE suffix) mounted on a substrate with decoupling capacitors. See the TMS465169 data sheet (literature number SMHS566).

The TM4EN64NPU is a 32M-byte, 168-pin DIMM. The DIMM is composed of four TMS464169, 4194304 × 16-bit 8K-refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors. See the TMS464169 data sheet (literature number SMHS566).

The TM8EN64KPU is a 64M-byte ,168-pin DIMM. The DIMM is composed of eight TMS465169, 41934304 × 16-bit 4K-refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors. See the TMS465169 data sheet (literature number SMHS566).

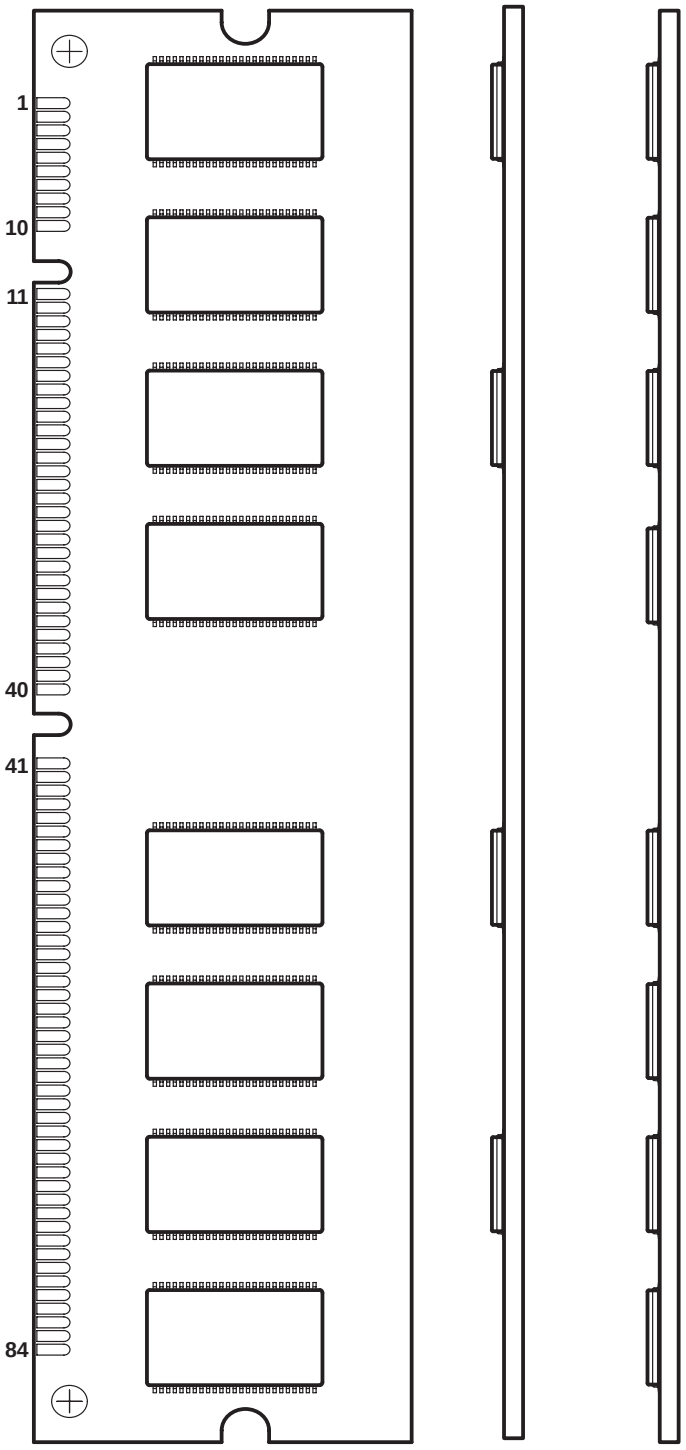
The TM8EN64NPU is a 64M-byte ,168-pin DIMM. The DIMM is composed of eight TMS464169, 41934304 × 16-bit 8K-refresh EDO DRAMs, each in a 400-mil, 50-pin plastic TSOP (DGE suffix) mounted on a substrate with decoupling capacitors. See the TMS464169 data sheet (literature number SMHS566).

operation

The TM4EN64xPU operates as four TMS46x169s that are connected as shown in the TM4EN64xPU functional block diagram. The TM8EN64xPU operates as 18 TMS46x169s that are connected as shown in the TM8EN64xPU functional block diagram.

PRODUCT PREVIEW

DUAL-IN-LINE MEMORY MODULE (TOP VIEW) **TM4EN64xPU (SIDE VIEW)** **TM8EN64xPU (SIDE VIEW)**



PIN NOMENCLATURE – TMxEN64KPU	
A[0:11]	Row Address Inputs
A[0:9]	Column Address Inputs
$\overline{DQ}[0:63]$	Data In / Data Out
$\overline{CAS}[0:7]$	Column-Address Strobe
$\overline{RAS}[0:3]$	Row-Address Strobe
$\overline{WE0}$ and $\overline{WE2}$	Write Enable
$\overline{OE0}$ and $\overline{OE2}$	Output Enable
SA[0:2]	Serial-Presence-Detect (SPD) Device Add Input
SDA	Serial PD Address / Data
SCL	Serial PD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

PIN NOMENCLATURE – TMxEN64NPU	
A[0:12]	Row Address Inputs
A[0:8]	Column Address Inputs
$\overline{DQ}[0:63]$	Data In / Data Out
$\overline{CAS}[0:7]$	Column-Address Strobe
$\overline{RAS}[0:3]$	Row-Address Strobe
$\overline{WE0}$ and $\overline{WE2}$	Write Enable
$\overline{OE0}$ and $\overline{OE2}$	Output Enable
SA[0:2]	Serial-Presence-Detect (SPD) Device Add Input
SDA	Serial PD Address / Data
SCL	Serial PD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

Pin Assignments

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	$\overline{RAS3}$
4	DQ2	46	$\overline{CAS2}$	88	DQ34	130	$\overline{CAS6}$
5	DQ3	47	$\overline{CAS3}$	89	DQ35	131	$\overline{CAS7}$
6	V_{DD}	48	$\overline{WE2}$	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	V_{SS}	106	NC	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE0}$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	$\overline{CAS4}$	154	DQ57
29	$\overline{CAS1}$	71	DQ26	113	$\overline{CAS5}$	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	$\overline{RAS1}$	156	DQ59
31	$\overline{OE0}$	73	V_{DD}	115	NC	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	A12	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	NC	83	SCL	125	NC	167	SA2
42	NC	84	V_{DD}	126	NC	168	V_{DD}

PRODUCT PREVIEW

dual-in-line memory module and components

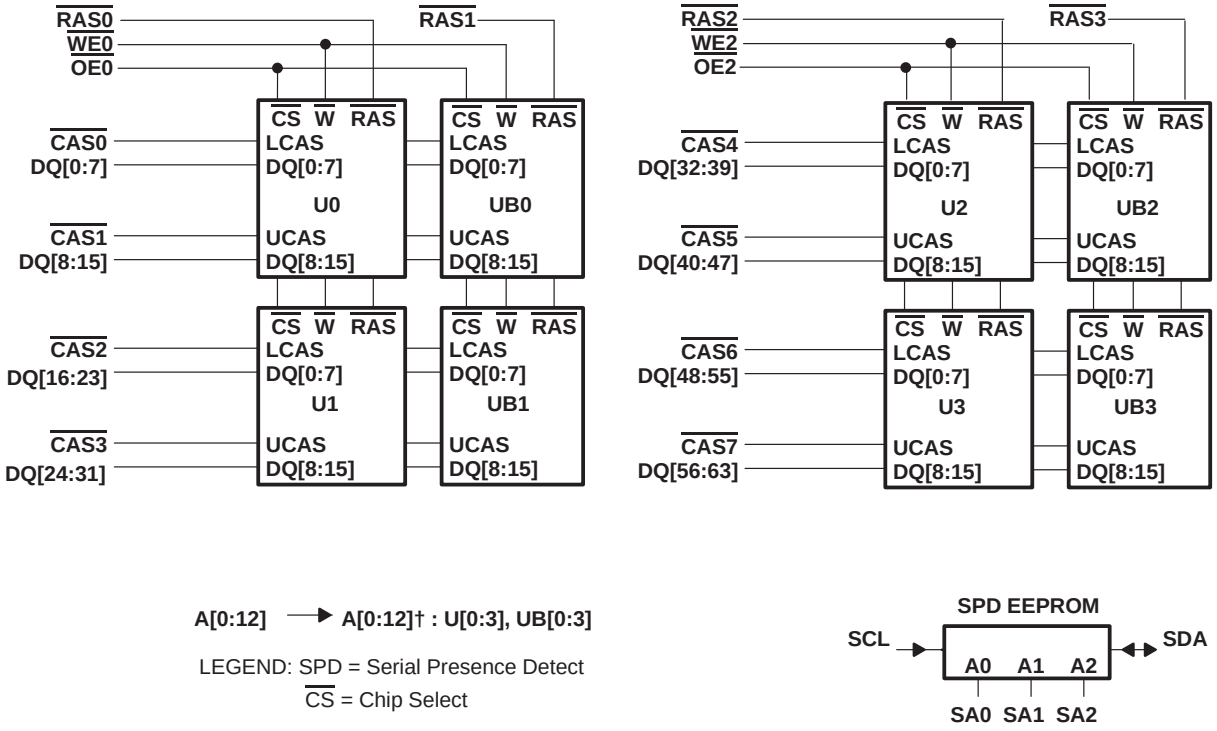
The dual-in-line memory module and components include:

- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

Table 1. Component Table

Module	Devices Used
TM4EN64xPU	U[0:3]
TM8EN64xPU	U[0:3], UB[0:3]

functional block diagram for the TMxEN64xPU



A[0:12] → A[0:12]† : U[0:3], UB[0:3]

LEGEND: SPD = Serial Presence Detect
$\overline{CS}$ = Chip Select

† A12 is not used in TM4EN64KPU, TM8EN64KPU

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM4EN64xPU . . . . . 4 W
TM8EN64xPU . . . . . 8 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH}-SPD	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM4EN64KPU

PARAMETER		TEST CONDITIONS†		'4EN64KPU-40		'4EN64KPU-50		'4EN64KPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD}–0.2		V_{DD}–0.2		V_{DD}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{DD}}$ = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			640		520		440	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			4		4		4	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			2		2		2	mA
I_{CC3}‡§	Average refresh current ($\overline{RASx}$-only refresh or CBR)	$\overline{V_{DD}}$ = 3.6 V, Minimum cycle, $\overline{RASx}$ cycling, $\overline{CASx}$ high ($\overline{RASx}$-only refresh), $\overline{RASx}$ low after $\overline{CASx}$ low (CBR)			640		520		440	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{DD}}$ = 3.6 V, $\overline{RASx}$ low, t_{HPC} = MIN, $\overline{CASx}$ cycling			600		480		400	mA
I_{CC5}	Average CBR refresh current	$\overline{V_{DD}}$ = 3.6 V, Minimum cycle, $\overline{RASx}$ low after $\overline{CASx}$ low			640		520		440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM4EN64NPU

PARAMETER		TEST CONDITIONS†		'4EN64NPU-40		'4EN64NPU-50		'4EN64NPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD}–0.2		V_{DD}–0.2		V_{DD}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, CASx high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			540		440		400	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			4		4		4	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high			2		2		2	mA
I_{CC3}‡§	Average refresh current (RAS-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RASx-only refresh), RASx low after CASx low (CBR)			540		440		400	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, RASx low, CASx cycling			560		440		360	mA
I_{CC5}	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, RASx low after CASx low			640		520		440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM8EN64KPU

PARAMETER		TEST CONDITIONS†		'8EN64KPU-40		'8EN64KPU-50		'8EN64KPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD}–0.2		V_{DD}–0.2		V_{DD}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{DD}}$ = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CAS}$x high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			644		524		444	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			4		4		4	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			2		2		2	mA
I_{CC3}‡§	Average refresh current (RAS-only refresh or CBR)	$\overline{V_{DD}}$ = 3.6 V, Minimum cycle, $\overline{RAS}$x cycling, $\overline{CAS}$x high ($\overline{RAS}$x-only refresh), $\overline{RAS}$x low after $\overline{CAS}$x low (CBR)			644		524		444	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{DD}}$ = 3.6 V, $\overline{RAS}$x low, $t_{\overline{HPC}}$ = MIN, $\overline{CAS}$x cycling			604		484		404	mA
I_{CC5}‡¶	Average CBR refresh current	$\overline{V_{DD}}$ = 3.6 V, Minimum cycle, $\overline{RAS}$x low after $\overline{CAS}$x low			640		520		440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$x = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM8EN64NPU

PARAMETER		TEST CONDITIONS†		'8EN64NPU-40		'8EN64NPU-50		'8EN64NPU-60		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD}–0.2		V_{DD}–0.2		V_{DD}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			544		444		404	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			4		4		4	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			2		2		2	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, $\overline{RASx}$ cycling, $\overline{CASx}$ high ($\overline{RASx}$-only refresh), $\overline{RASx}$ low after $\overline{CASx}$ low (CBR)			544		444		404	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, $\overline{RASx}$ low, t_{HPC} = MIN, $\overline{CASx}$ cycling			560		440		360	mA
I_{CC5}‡¶	Average CBR refresh current	V_{DD} = 3.6 V, Minimum cycle, $\overline{RASx}$ low after $\overline{CASx}$ low			640		520		440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		'4EN64xPU		'8EN64xPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0 – A12		22		42	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}x$		30		58	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}x$		9		16	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}x$		30		30	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}x$		30		58	pF
C_o	Output capacitance		9		16	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitance,SA0,SA1,SA2,SCL inputs		7		7	pF

NOTE 2: V_{DD} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		'xEN64xPU-40		'xEN64xPU-50		'xEN64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		20		25		30	ns
t_{CAC}	Access time from $\overline{CAS}x$ (see Note 4)		11		13		15	ns
t_{CPA}	Access time from $\overline{CAS}x$ precharge (see Note 4)		22		28		35	ns
t_{RAC}	Access time from $\overline{RAS}x$ (see Note 4)		40		50		60	ns
t_{OEA}	Access time from $\overline{OE}x$ (see Note 4)		11		13		15	ns
t_{CLZ}	Delay time, $\overline{CAS}x$ to output in low-impedance state	0		0		0		ns
t_{OEZ}	Output buffer turn off delay from $\overline{OE}x$ (see Note 5)	3	11	3	13	3	15	ns
t_{REZ}	Output buffer turn off delay from $\overline{RAS}x$ (see Note 5)	3	11	3	13	3	15	ns
t_{CEZ}	Output buffer turn off delay from $\overline{CAS}x$ (see Note 5)	3	11	3	13	3	15	ns
t_{WEZ}	Output buffer turn off delay from $\overline{WE}x$ (see Note 5)	3	11	3	13	3	15	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The MAX specifications of t_{REZ}, t_{CEZ}, t_{WEZ}, and t_{OEZ} are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements

		'xEN64xPU-40		'xEN64xPU-50		'xEN64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	16		20		25		ns
t_{PRWC}	Cycle time, EDO read-write	47		57		68		ns
t_{CSH}	Delay time, $\overline{RAS}x$ active to $\overline{CAS}x$ precharge	32		40		48		ns
t_{CHO}	Hold time, $\overline{OE}x$ from $\overline{CAS}x$	5		5		5		ns
t_{DOH}	Hold time, output from $\overline{CAS}x$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CAS}x$ active (see	6	10000	8	10000	10	10000	ns
t_{WPE}	Pulse duration, $\overline{WE}x$ active (output disable only)	5		5		5		ns
t_{CP}	Pulse duration, $\overline{CAS}x$ precharge	6		8		10		ns
t_{OCH}	Setup time, $\overline{OE}x$ before $\overline{CAS}x$	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}x$	5		5		5		ns

ac timing requirements (see Note 3)

		’xEN64xPU-40		’xEN64xPU-50		’xEN64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	69		84		104		ns
t_{RWC}	Cycle time, read-write	92		111		135		ns
t_{RASP}	Pulse duration, $\overline{RAS}$x active, page mode (see Note 6)	40	100 000	50	100 000	60	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$x active, nonpage mode (see Note 6)	40	10 000	50	10 000	60	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$x precharge	25		30		40		ns
t_{WP}	Pulse duration, write command	6		8		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 7)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$x precharge	6		8		10		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$x precharge	6		8		10		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$x active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$x active (CBR refresh only)	5		5		5		ns
t_{CSR}	Setup time, $\overline{CAS}$x referenced to $\overline{RAS}$x (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	6		8		10		ns
t_{DH}	Hold time, data in (see Note 7)	6		8		10		ns
t_{RAH}	Hold time, row address	6		8		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$x (see Note 8)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$x (see Note 8)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$x active (early-write only)	6		8		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$x active from $\overline{CAS}$x precharge	22		28		35		ns
t_{OEH}	Hold time, $\overline{OE}$x command	11		13		15		ns
t_{ROH}	Hold time, $\overline{RAS}$x referenced to $\overline{OE}$x	6		8		10		ns
t_{WRH}	Hold time, write after $\overline{RAS}$x active (CBR refresh only)	6		8		10		ns
t_{CHS}	Hold time, $\overline{CAS}$x active after $\overline{RAS}$x precharge (self-refresh)	– 50		– 50		– 50		ns
t_{AWD}	Delay time, column address to write command (read-write only)	35		42		49		ns
t_{CHR}	Delay time, $\overline{CAS}$x referenced to $\overline{RAS}$x (CBR refresh only)	6		8		10		ns
t_{CRP}	Delay time, $\overline{CAS}$x precharge to $\overline{RAS}$x	5		5		5		ns
t_{CWD}	Delay time, $\overline{CAS}$x to write command (read-write operation only)	26		30		34		ns
t_{OED}	Delay time, $\overline{OE}$x to data in	11		13		15		ns
t_{RAD}	Delay time, $\overline{RAS}$x to column address (see Note 9)	8	20	10	25	12	30	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$x precharge	20		25		30		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$x precharge	12		15		18		ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. Referenced to the later of $\overline{CAS}$x or $\overline{WE}$x in write operations
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

ac timing requirements (see Note 3) (continued)

		’xEN64xPU-40		’xEN64xPU-70		’xEN64xPU-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RCD}	Delay time, $\overline{RAS}$x to $\overline{CAS}$x (see Note 9)	10	29	12	37	14	45	ns
t_{RPC}	Delay time, $\overline{RAS}$x precharge to $\overline{CAS}$x	5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$x active to $\overline{RAS}$x precharge	6		8		10		ns
t_{RWD}	Delay time, $\overline{RAS}$x active to write command (read-write only)	55		67		79		ns
t_{CPW}	Delay time, $\overline{CAS}$x precharge to write command (read-write only)	37		45		54		ns
t_{RASS}	Pulse duration, $\overline{RAS}$x active, self-refresh (see Note 10)	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$x precharge after self-refresh	70		90		110		ns
t_{REF}	Refresh time interval		64		64		64	ms
t_T	Transition time	1	50	1	50	1	50	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
9. The maximum value is specified only to ensure access time.
10. During the period of 10 µs $\leq$ tRASS $\leq$ 100 µs, the device is in transition state from normal operational mode to self–refresh mode.

PRODUCT PREVIEW

serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 2—TM4EN64KPU Table 3—TM4EN64NPU

Table 4—TM8EN64KPU Table 5—TM8EN64NPU

Table 2. Serial-Presence-Detect Data for the TM4EN64KPU

BYTE NO.	FUNCTION DESCRIBED	’4EN64KPU-40		’4EN64KPU-50		’4EN64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	DIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	38	26h	50	32h	62	3Eh
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h

PRODUCT PREVIEW

serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM4EN64KPU (Continued)

BYTE NO.	FUNCTION DESCRIBED	'4EN64KPU-40		'4EN64KPU-50		'4EN64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer's part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator's specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

serial presence detect (continued)

Table 3. Serial-Presence-Detect Data for the TM4EN64NPU

BYTE NO.	FUNCTION DESCRIBED	’4EN64NPU-40		’4EN64NPU-50		’4EN64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	tRAC = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	08h	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	DIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	38	26h	50	32h	62	3Eh
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

serial presence detect (continued)

Table 4. Serial-Presence-Detect Data for the TM8EN64KPU

BYTE NO.	FUNCTION DESCRIBED	’8EN64KPU-40		’8EN64KPU-50		’8EN64KPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	DIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	39	27h	51	33h	63	3Fh
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

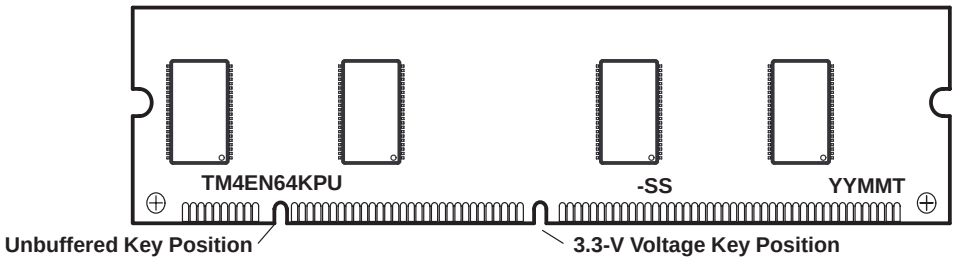
Table 5. Serial-Presence-Detect Data for the TM8EN64NPU

BYTE NO.	FUNCTION DESCRIBED	'8EN64NPU-40		'8EN64NPU-50		'8EN64NPU-60	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	13	0Dh	13	0Dh	13	0Dh
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 40 ns	28h	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 11 ns	0Bh	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh
11	DIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x16	10h	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	39	27h	51	33h	63	3Fh
64–71	Manufacturer's JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer's part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator's specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

device symbolization (TM4EN64KPU illustrated)



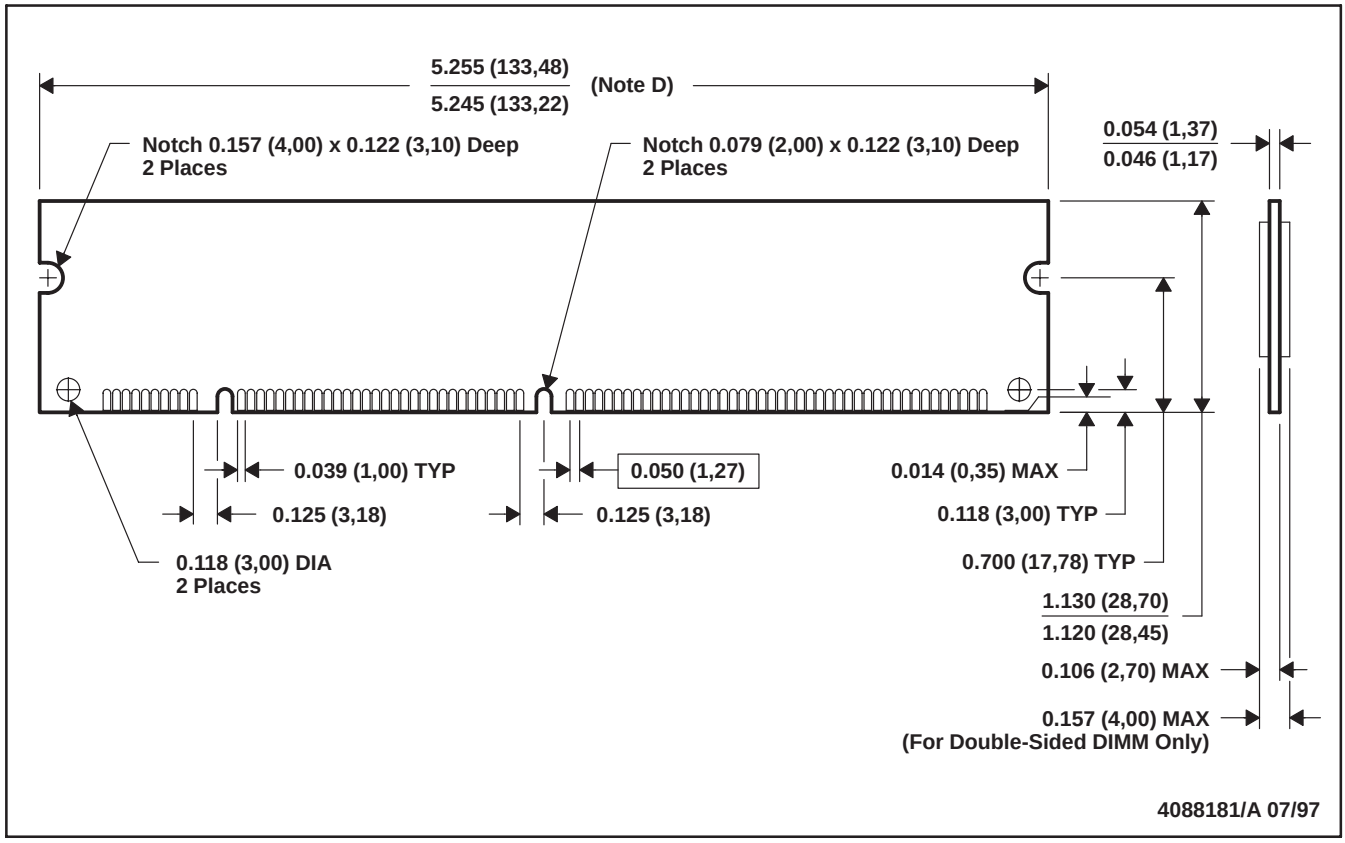
YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

MECHANICAL DATA

BS (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes de-panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.