

TM497FBK32, TM497FBK32S 4194304 BY 32-BIT TM893GBK32, TM893GBK32S 8388608 BY 32-BIT EXTENDED DATA OUT DYNAMIC RAM MODULES

SMMS668 – NOVEMBER 1996

- **Organization**
 - TM497FBK32/S: 4 194 304 x 32
 - TM893GBK32/S: 8 388 608 x 32
- **Single 5-V Power Supply ($\pm 10\%$ Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497FBK32/S – Uses Eight 16M-Bit Dynamic Random-Access Memories (DRAMs) in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893GBK32/S – Uses Sixteen 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
32 ms (2 048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Extended Data Out (EDO) Operation With $\overline{\text{CAS}}$ -Before-RAS (CBR), RAS-Only, and Hidden Refresh**

- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME	ACCESS TIME	ACCESS TIME	EDO CYCLE
	t_{RAC} (MAX)	t_{AA} (MAX)	t_{CAC} (MAX)	t_{HPC} (MIN)
'497FBK32/S-60	60 ns	30 ns	15 ns	25 ns
'497FBK32/S-70	70 ns	35 ns	18 ns	30 ns
'497FBK32/S-80	80 ns	40 ns	20 ns	35 ns
'893GBK32/S-60	60 ns	30 ns	15 ns	25 ns
'893GBK32/S-70	70 ns	35 ns	18 ns	30 ns
'893GBK32/S-80	80 ns	40 ns	20 ns	35 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
0°C to 70°C
- **Gold-Tabbed Version Available:[†]**
TM497FBK32, TM893GBK32
- **Tin-Lead (Solder-) Tabbed Version**
Available: TM497FBK32S, TM893GBK32S

description

The TM497FBK32 is a 16M-byte dynamic random-access memory (DRAM) organized as four times 4194304 $\times$ 8 bits in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417409DJ, 4194304 $\times$ 4-bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417409DJ is described in the TMS416409, TMS417409 data sheet (literature number SMKS884).

The TM497FBK32 SIMM is available in the single-sided BK leadless module for use with sockets. The TM497FBK32 features RAS access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

The TM893GBK32/S is a 32M-byte DRAM organized as four times 8388608 $\times$ 8 bits in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS417409DJ 4194304 $\times$ 4-bit DRAMs.

The TM893GBK32/S SIMM is available in the double-sided BK leadless module for use with sockets. The TM893GBK32/S features RAS access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497FBK32/S operates as eight TMS417409DJs connected as shown in Figure 1 and in Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

The TM893GBK32/S operates as sixteen TMS417409DJs connected as shown in Figure 2 and in Table 2. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TM893GBK32, TM893GBK32S 8388608 BY 32-BIT
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SMMS668 – NOVEMBER 1996

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2 048 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

power up

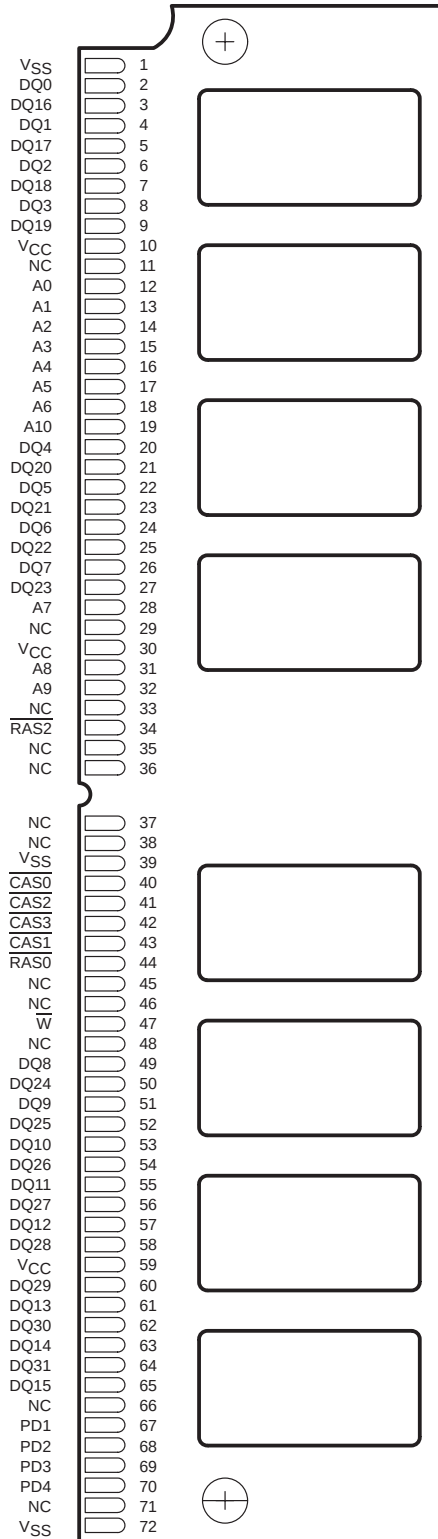
To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{\text{RAS}}$ -only or CBR) cycle.



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SMMS668 – NOVEMBER 1996

**BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)**



**TM497FBK32/S
(SIDE VIEW)**



**TM893GBK32/S
(SIDE VIEW)**



PIN NOMENCLATURE

A0–A10	Address Inputs
CAS0–CAS3	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
RAS0–RAS3	Row-Address Strobe
V _{CC}	5-V Supply
V _{SS}	Ground
W	Write Enable

PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497FBK32/S	80 ns	V _{SS}	NC	NC	V _{SS}
	70 ns	V _{SS}	NC	V _{SS}	NC
	60 ns	V _{SS}	NC	NC	NC
TM893GBK32/S	80 ns	NC	V _{SS}	NC	V _{SS}
	70 ns	NC	V _{SS}	V _{SS}	NC
	60 ns	NC	V _{SS}	NC	NC

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SMMS668 – NOVEMBER 1996

Table 1. TM497FBK32/S Connection Table

DATA BLOCK	$\overline{\text{RAS}}_x$	$\overline{\text{CAS}}_x$
DQ0–DQ7	$\overline{\text{RAS}}_0$	$\overline{\text{CAS}}_0$
DQ8–DQ15	$\overline{\text{RAS}}_0$	$\overline{\text{CAS}}_1$
DQ16–DQ23	$\overline{\text{RAS}}_2$	$\overline{\text{CAS}}_2$
DQ24–DQ31	$\overline{\text{RAS}}_2$	$\overline{\text{CAS}}_3$

Table 2. TM893GBK32/S Connection Table

DATA BLOCK	$\overline{\text{RAS}}_x$		$\overline{\text{CAS}}_x$
	Side 1	Side 2	
DQ0–DQ7	$\overline{\text{RAS}}_0$	$\overline{\text{RAS}}_1$	$\overline{\text{CAS}}_0$
DQ8–DQ15	$\overline{\text{RAS}}_0$	$\overline{\text{RAS}}_1$	$\overline{\text{CAS}}_1$
DQ16–DQ23	$\overline{\text{RAS}}_2$	$\overline{\text{RAS}}_3$	$\overline{\text{CAS}}_2$
DQ24–DQ31	$\overline{\text{RAS}}_2$	$\overline{\text{RAS}}_3$	$\overline{\text{CAS}}_3$

single-in-line memory module and components

PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

Contact area for TM497FBK32 and TM893GBK32: Nickel plate and gold plate over copper

Contact area for TM497FBK32S and TM893GBK32S: Nickel plate and tin-lead over copper

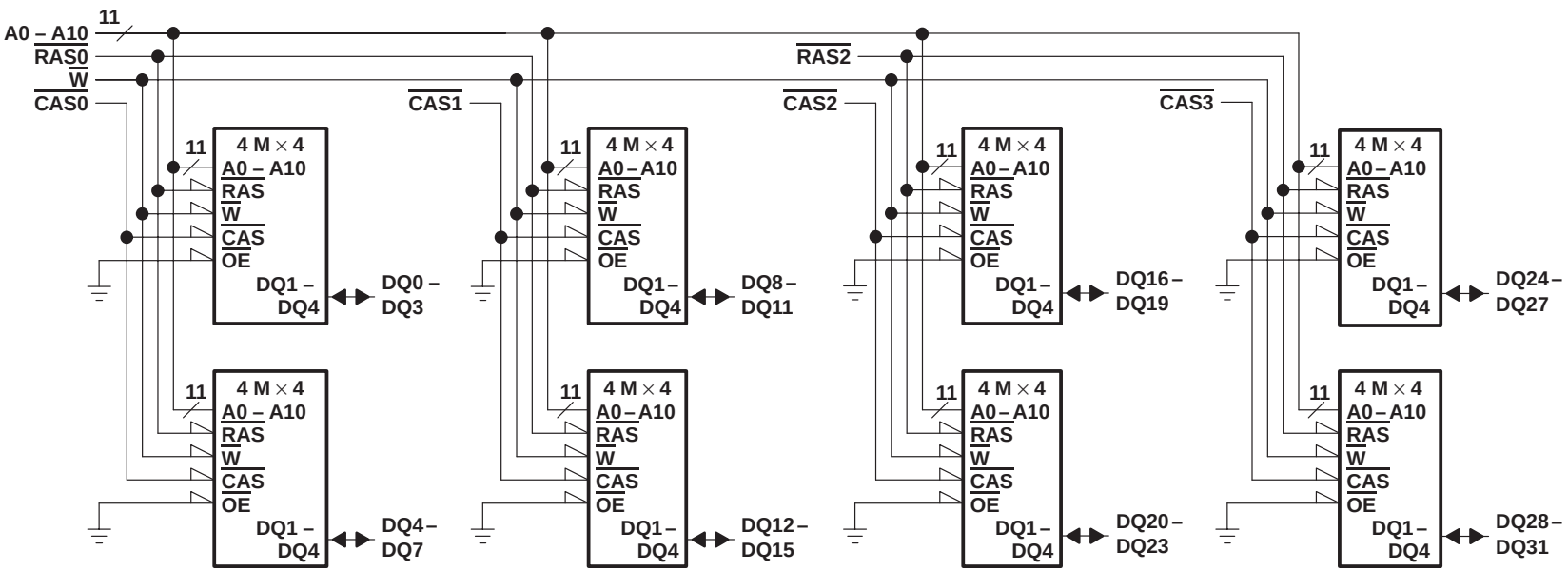
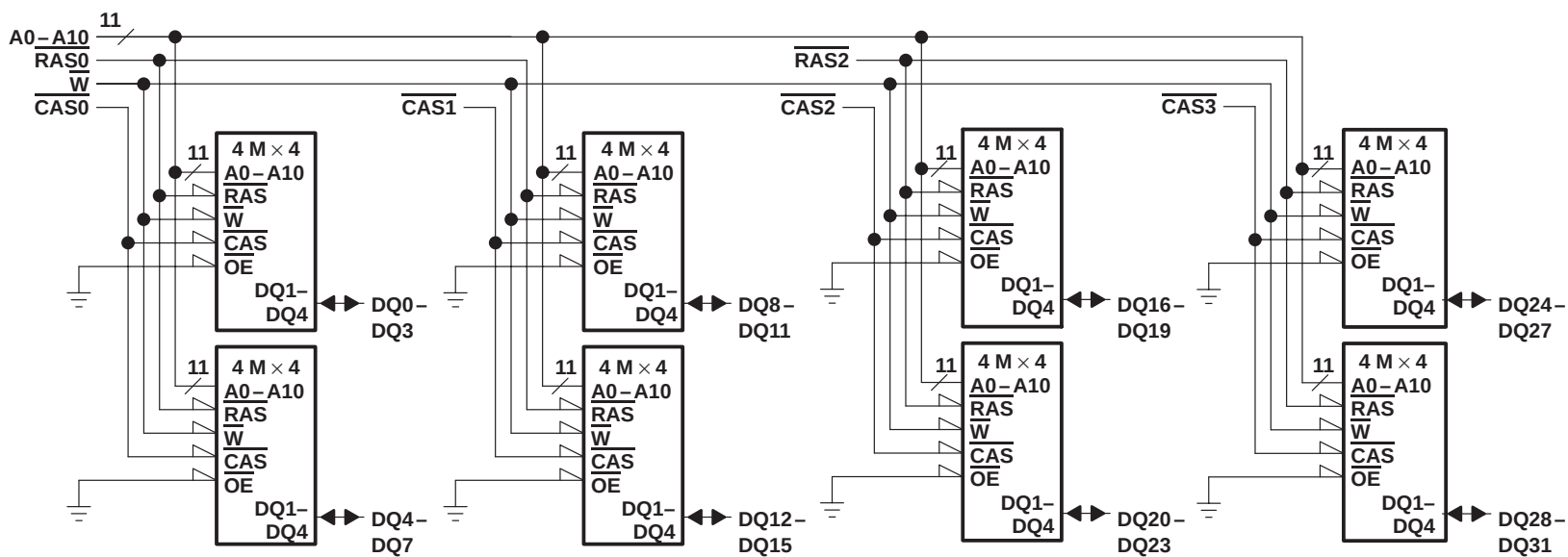


Figure 1. Functional Block Diagram of TM497FBK32

TM497FBK32, TM497FBK32S 4 194 304 BY 32-BIT
 TM893GBK32, TM893GBK32S 8 388 608 BY 32-BIT
 EXTENDED DATA OUT DYNAMIC RAM MODULES
 SMMS668 - NOVEMBER 1996

side 1



side 2

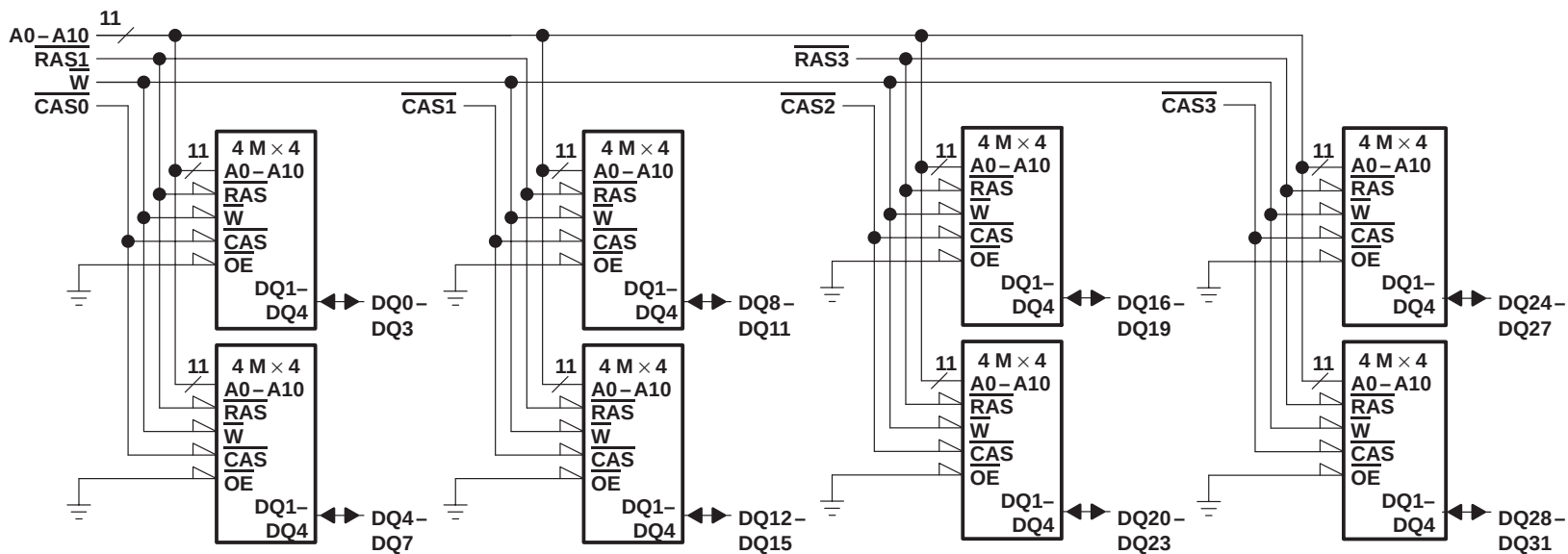


Figure 2. Functional Block Diagram of TM893GBK32/S

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	8 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2.4		6.5	V
V_{IL} Low-level input voltage (see Note 2)	– 1		0.8	V
T_A Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS [‡]	'497FBK32-60		'497FBK32-70		'497FBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH} High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL} Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC} , CAS high		± 10		± 10		± 10	µA
I_{CC1} Read- or write-cycle current (see Note 3)	$V_{CC} = 5.5$ V, Minimum cycle		880		800		720	mA
I_{CC2} Standby current	$V_{IH} = 2.4$ V (TTL), After one memory cycle, RAS and CAS high		16		16		16	mA
	$V_{IH} = V_{CC} - 0.2$ V (CMOS), After one memory cycle, RAS and CAS high		8		8		8	mA
I_{CC3} Average refresh current (RAS only or CBR) (see Note 3)	$V_{CC} = 5.5$ V, Minimum cycle, RAS cycling, CAS high (RAS only); RAS low after CAS low (CBR)		880		800		720	mA
I_{CC4} Average page current (see Note 4)	$V_{CC} = 5.5$ V, $t_{PC} = \text{MIN}$, RAS low, CAS cycling		560		480		400	mA

[‡] For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$
 4. Measured with a maximum of one address change while $\text{CAS} = V_{IH}$

**TM497FBK32, TM497FBK32S 4 194 304 BY 32-BIT
TM893GBK32, TM893GBK32S 8 388 608 BY 32-BIT
EXTENDED DATA OUT DYNAMIC RAM MODULES**

SMMS668 – NOVEMBER 1996

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'893GBK32-60		'893GBK32-70		'893GBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 5 mA	2.4		2.4		2.4		V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA		0.4		0.4		0.4	V
I _I Input current (leakage)	V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All others = 0 V to V _{CC}		± 20		± 20		± 20	µA
I _O Output current (leakage)	V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , CASx high		± 20		± 20		± 20	µA
I _{CC1} Read- or write-cycle current (see Note 3)	V _{CC} = 5.5 V, Minimum cycle		896		816		736	mA
I _{CC2} Standby current	V _{IH} = 2.4 V (TTL), After one memory cycle, RASx and CASx high		32		32		32	mA
	V _{IH} = V _{CC} – 0.2 V (CMOS), After one memory cycle, RASx and CASx high		16		16		16	mA
I _{CC3} Average refresh current (RAS only or CBR) (see Note 3)	V _{CC} = 5.5 V, RASx cycling, (RASx only); Minimum cycle CASx low (CBR) CASx high RASx low after		1760		1600		1440	mA
I _{CC4} Average page current (see Note 4)	V _{CC} = 5.5 V, t _{PC} = MIN, RASx low, CASx cycling		576		496		416	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$

4. Measured with a maximum of one address change while $\text{CAS} = V_{IH}$

**capacitance over recommended ranges of supply voltage and operating free-air temperature,
f = 1 MHz (see Note 5)**

PARAMETER	TM497FBK32		TM893GBK32		UNIT
	MIN	MAX	MIN	MAX	
C _{i(A)} Input capacitance, address inputs		50		80	pF
C _{i(R)} Input capacitance, $\overline{\text{RAS}}$ inputs		33		28	pF
C _{i(C)} Input capacitance, $\overline{\text{CAS}}$ inputs		17		28	pF
C _{i(W)} Input capacitance, write-enable input		66		112	pF
C _{o(DQ)} Output capacitance on DQ pins		9		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.



TM497FBK32, TM497FBK32S 4 194 304 BY 32-BIT
 TM893GBK32, TM893GBK32S 8 388 608 BY 32-BIT
 EXTENDED DATA OUT DYNAMIC RAM MODULES

SMMS668 – NOVEMBER 1996

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'497FBK32-60 '893GBK32-60		'497FBK32-70 '893GBK32-70		'497FBK32-80 '893GBK32-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address		30		35		40	ns
t _{CAC} Access time from $\overline{\text{CAS}}$ low		15		18		20	ns
t _{CPA} Access time from column precharge		35		40		45	ns
t _{RAC} Access time from $\overline{\text{RAS}}$ low		60		70		80	ns
t _{CLZ} $\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t _{OH} Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t _{OFF} Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

	'497FBK32-60 '893GBK32-60		'497FBK32-70 '893GBK32-70		'497FBK32-80 '893GBK32-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{HPC} Cycle time, EDO page mode read or write	25		30		35		ns
t _{PRWC} Cycle time, EDO read-write	80		90		100		ns
t _{CSH} Hold time, $\overline{\text{CAS}}$ after $\overline{\text{RAS}}$	50		55		60		ns
t _{DOH} Hold time, output after $\overline{\text{RAS}}$	3		3		3		ns
t _{CAS} Pulse duration, $\overline{\text{CAS}}$	10	10 000	12	10 000	15	10 000	ns
t _{WPE} Pulse duration, $\overline{\text{W}}$ (output disable only)	5		5		5		ns
t _{CP} Precharge time, $\overline{\text{CAS}}$	5		5		5		ns



TM497FBK32, TM497FBK32S 4 194 304 BY 32-BIT
TM893GBK32, TM893GBK32S 8 388 608 BY 32-BIT
EXTENDED DATA OUT DYNAMIC RAM MODULES

SMMS668 – NOVEMBER 1996

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497FBK32-60 '893GBK32-60		'497FBK32-70 '893GBK32-70		'497FBK32-80 '893GBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t _{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t _{RASP}	Pulse duration, page-mode, $\overline{\text{RAS}}$ low	60	100 000	70	100 000	80	100 000	ns
t _{RAS}	Pulse duration, non-page-mode, $\overline{\text{RAS}}$ low	60	10 000	70	10 000	80	10 000	ns
t _{CAS}	Pulse duration, $\overline{\text{CAS}}$ low	15	10 000	18	10 000	20	10 000	ns
t _{CP}	Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t _{RP}	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t _{WP}	Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t _{ASC}	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{ASR}	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t _{DS}	Setup time, data before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{RCS}	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWL}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{CAS}}$ high	10		12		15		ns
t _{RWL}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{RAS}}$ high	10		12		15		ns
t _{WCS}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{WRP}	Setup time, $\overline{\text{W}}$ -high before $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CAH}	Hold time, column address after $\overline{\text{CAS}}$ low	10		12		15		ns
t _{RHCP}	Hold time, $\overline{\text{RAS}}$ high after $\overline{\text{CAS}}$ precharge	35		40		45		ns
t _{DH}	Hold time, data after $\overline{\text{CAS}}$ low	10		12		15		ns
t _{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t _{RCH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t _{RRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns
t _{WCH}	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low	10		12		15		ns
t _{WRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t _{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
t _{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	50		55		60		ns
t _{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t _{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t _{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t _{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t _{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10)	20	45	20	52	20	60	ns
t _{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	0		0		0		ns
t _{RSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	10		12		15		ns
t _{REF}	Refresh time interval		32		32		32	ms
t _T	Transition time	3	30	3	30	3	30	ns

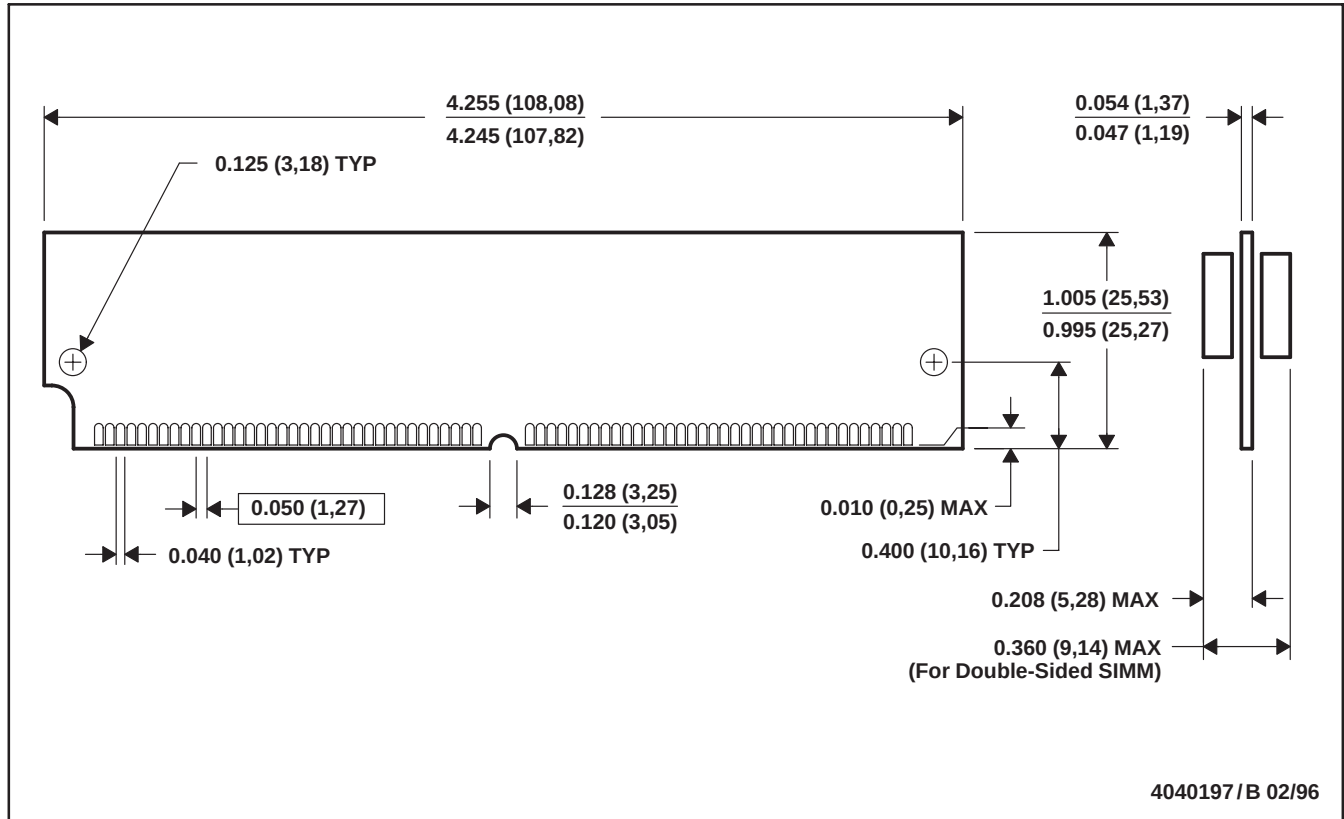
- NOTES: 7. All cycles assume $t_T = 5$ ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP} .
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.



MECHANICAL DATA

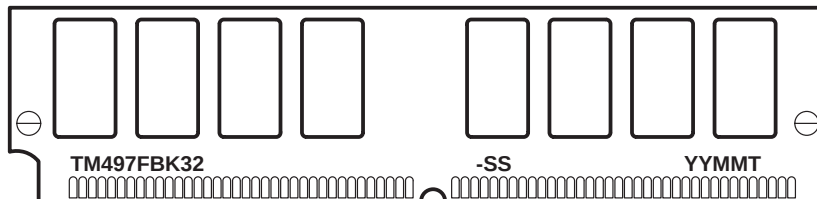
BK (R-PSIM-N72)

SINGLE-IN-LINE MEMORY MODULE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

device symbolization



YY = Year Code
 MM = Month Code
 T = Assembly Site Code
 -SS = Speed Code

NOTE: The location of the part number may vary.

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