TM124MBK36E, TM124MBK36T 1048576 BY 36-BIT DYNAMIC RAM MODULE
TM248NBK36E, TM248NBK36T 2097152 BY 36-BIT DYNAMIC RAM MODULE

- **Organization**
  TM124MBK36E . . . 1 048 576 × 36
  TM248NBK36E . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Leadless Single-In-Line Memory Module (SIMM)**
- **TM124MBK36E – Utilizes Eight 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 2-Megabit Dual-$\overline{\text{CAS}}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248NBK36E – Utilizes Sixteen 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Four 2-Megabit Dual-$\overline{\text{CAS}}$ Dynamic RAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$, $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
’124MBK36E-60	60 ns	30 ns	15 ns	110 ns
’124MBK36E-70	70 ns	35 ns	18 ns	130 ns
’124MBK36E-80	80 ns	40 ns	20 ns	150 ns
’248NBK36E-60	60 ns	30 ns	15 ns	110 ns
’248NBK36E-70	70 ns	35 ns	18 ns	130 ns
’248NBK36E-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range: 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  – TM124MBK36E
  – TM248NBK36E
- **Tin-Lead (Solder) Tabbed Versions Available:**
  – TM124MBK36T
  – TM248NBK36T

description

The TM124MBK36E is a dynamic random-access memory (RAM) organized as four times 1048576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in a 20/26-lead plastic small-outline J-lead (SOJ) package, and two TMS42260DJ, 1 048 576 × 2-bit dual-$\overline{\text{CAS}}$ dynamic RAMs, each in a 24/26-lead plastic small-outline J-lead (SOJ) package, mounted on a substrate with decoupling capacitors. Each TMS44400DJ or TMS42260DJ is described in the TMS44400 or TMS42260 data sheet, respectively.

The TM124MBK36E is available in the single-sided BK leadless module for use with sockets. It features $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

The TM248NBK36E is a dynamic random-access memory (RAM) organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of sixteen TMS44400DJ, 1 048 576 × 4-bit dynamic RAMs, each in a 20/26-lead plastic small-outline J-lead (SOJ) package, and four TMS42260DJ, 1 048 576 × 2-bit dual-$\overline{\text{CAS}}$ dynamic RAMs, each in a 24/26-lead plastic small-outline J-lead (SOJ) package, mounted on a substrate with decoupling capacitors. Each TMS44400DJ or TMS42260DJ is described in the TMS44400 or TMS42260 data sheet, respectively.

The TM248NBK36E is available in the double-sided BK leadless module for use with sockets. It features $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

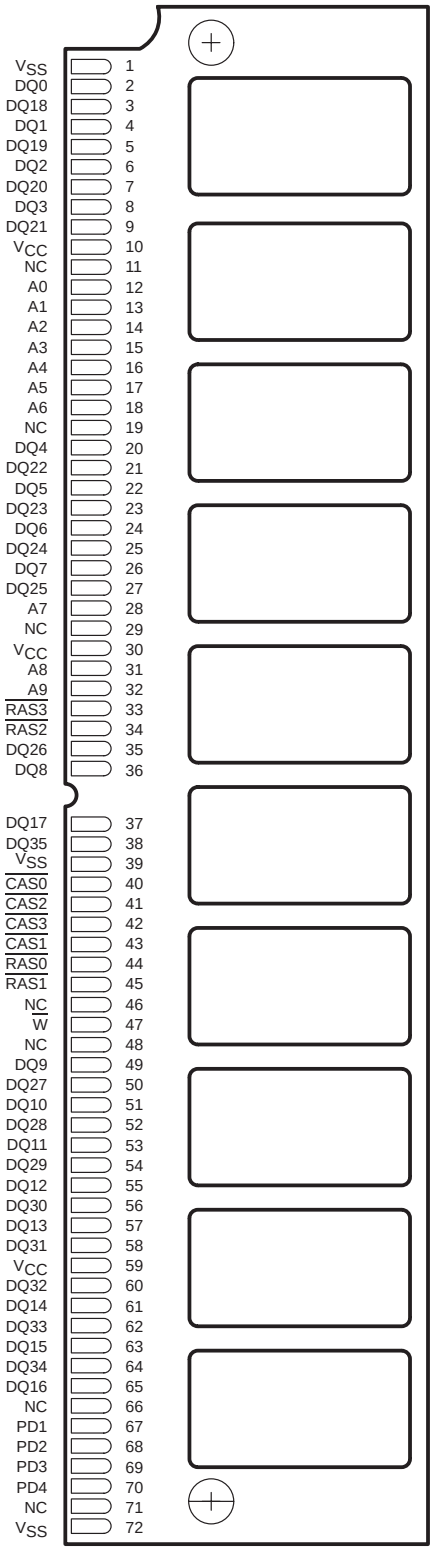
operation

The TM124MBK36E operates as eight TMS44400DJs and two TMS42260DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

The TM248NBK36E operates as sixteen TMS44400DJs and four TMS42260DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

BK SINGLE-IN-LINE MEMORY MODULE

(TOP VIEW)

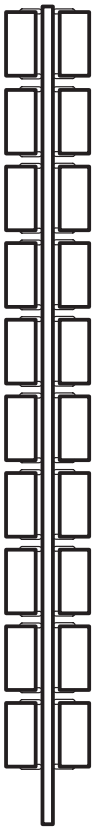


TM124MBK36E

(SIDE VIEW)

TM248NBK36E

(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36E	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36E	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

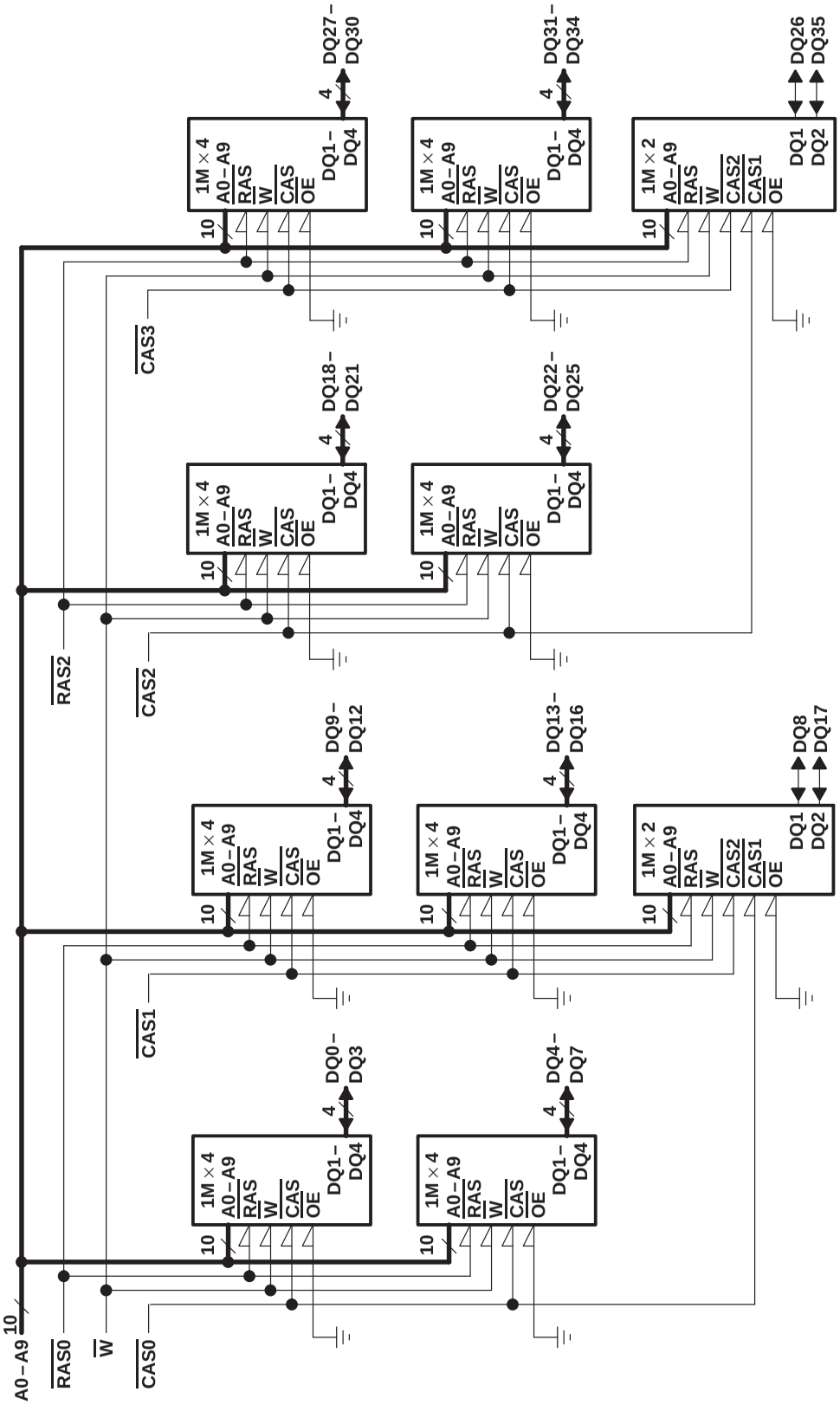
DATA BLOCK	$\overline{\text{RAS}}$x		$\overline{\text{CAS}}$x
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS0}}$
DQ8	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS0}}$
DQ9–DQ16	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS1}}$
DQ17	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS1}}$
DQ18–DQ25	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS2}}$
DQ26	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS2}}$
DQ27–DQ34	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS3}}$
DQ35	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS3}}$

† Side 2 applies to the TM248NBK36E only.

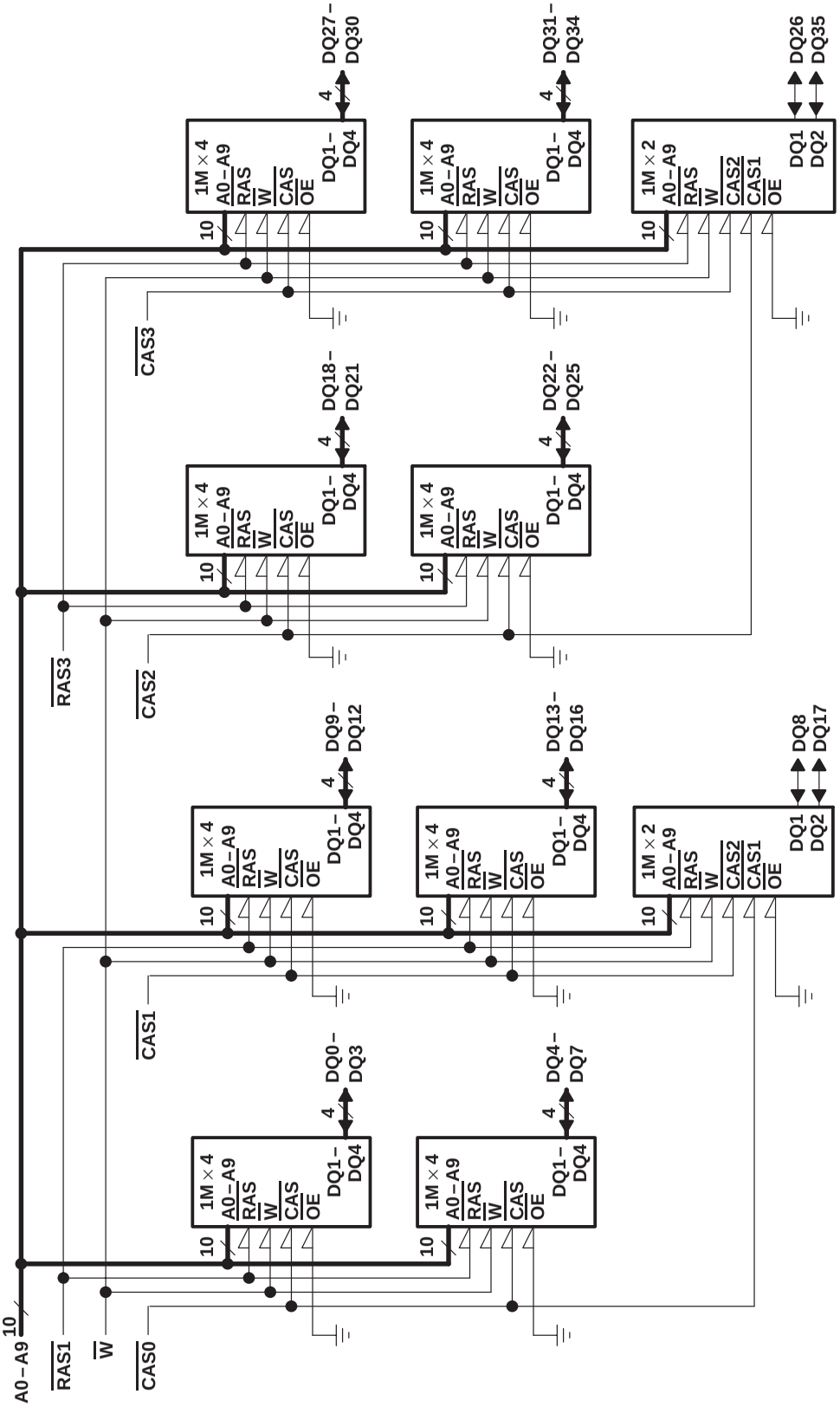
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36E and TM248NBK36E: Nickel plate and gold plate over copper
Contact area for TM124MBK36T and TM248NBK36T: Nickel plate and tin/lead over copper

functional block diagram (TM124MBK36E and TM248NBK36E, side 1)



functional block diagram (TM248NBK36E, side 2)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Input voltage range (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 10 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36E-60		'124MBK36E-70		'124MBK36E-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1050		900		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		10		10		10	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1050		900		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		900		800		700	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36E-60		'248NBK36E-70		'248NBK36E-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1070		920		820	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		40		40		40	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		20		20		20	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		2100		1800		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		920		820		720	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36E		'248NBK36E		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		50		100	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		35		35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		21		42	pF
$C_{i(W)}$	Input capacitance, write-enable input		70		140	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124MBK36E-60 '248NBK36E-60		'124MBK36E-70 '248NBK36E-70		'124MBK36E-80 '248NBK36E-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124MBK36E-60 '248NBK36E-60		'124MBK36E-70 '248NBK36E-70		'124MBK36E-80 '248NBK36E-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (see Note 9)	10		10		10		ns

NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only

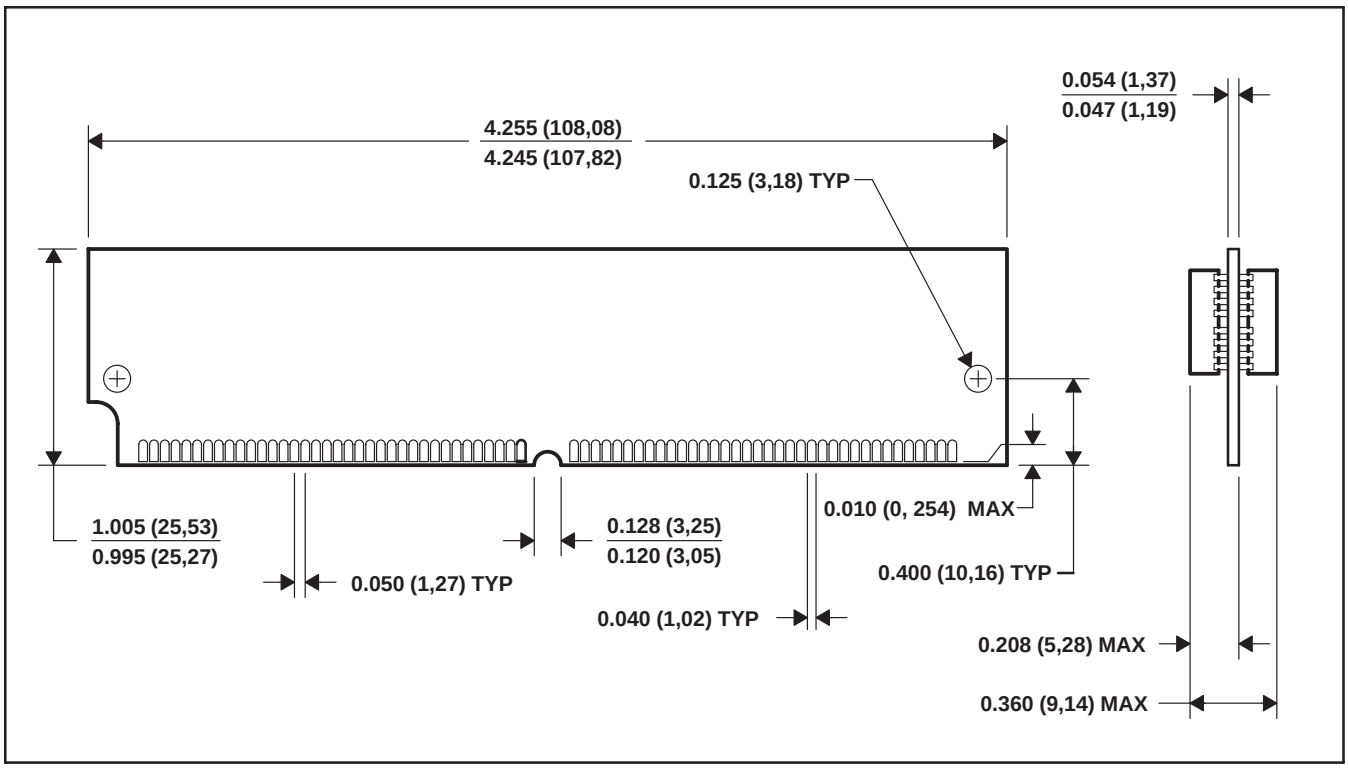
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’124MBK36E-60 ’248NBK36E-60		’124MBK36E-70 ’248NBK36E-70		’124MBK36E-80 ’248NBK36E-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

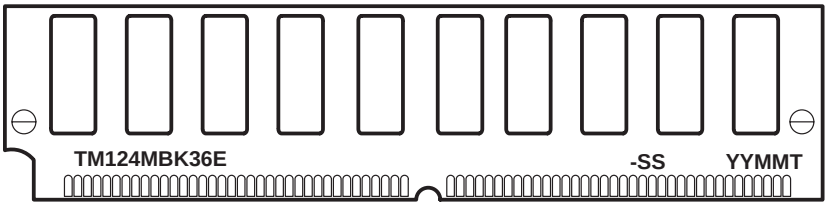
MECHANICAL DATA

BK–72 LEAD SINGLE IN-LINE MEMORY MODULE — BK/R–PSIP–N72



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization (TM124MBK36E illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

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