

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000pF
- Low Quiescent Current
- 5 V to 40 V Operation
- Thermal Protection

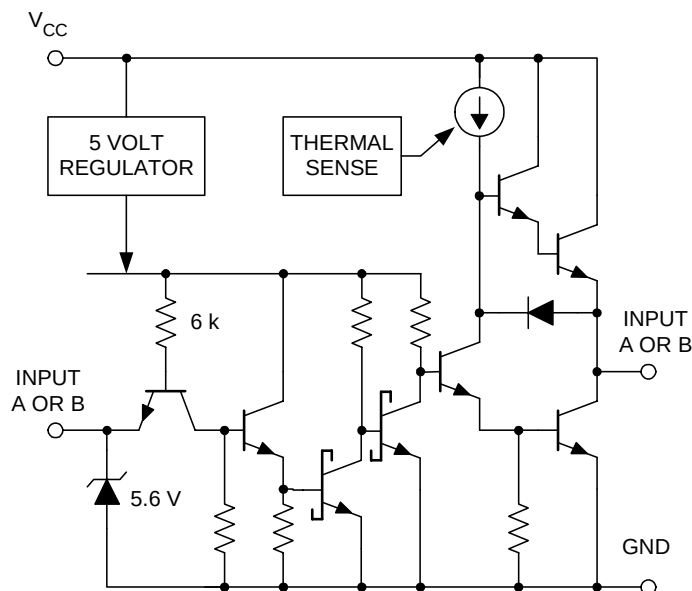
description

The UC3709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 A of either source or sink current from a totem-pole output stage configured for minimal cross-conduction current spike.

The UC3709 is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30 V. This design also includes thermal shutdown protection.

simplified schematic (only one driver shown)



UDG-00068

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)^{†‡}

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40 V	40V
Output Current (Source or Sink)		
Steady-State	±500 mA	±500 mA
Peak Transient	±1.5 A	±1.0 A
Capacitive Discharge Energy	20 mJ	15 mJ
Digital Inputs [‡]	5.5 V	5.5 V
Power Dissipation at $T_A = 25^\circ\text{C}$	1 W	1 W
Power Dissipation at $T_C = 25^\circ\text{C}$	3 W	2 W
Operating Temperature Range	-55°C to 125°C	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C	-65°C to 150°C
Lead Temperature (Soldering, 10 Seconds)	300°C	300 °C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All currents are positive into and negative out of the specified terminals. Digital drive can exceed 5.5V if input is limited to 10A. Consult the Packaging Section of the Databook for thermal limitations and considerations of the package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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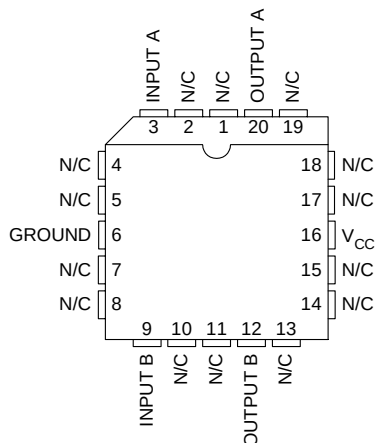
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UC1709, UC2709, UC3709

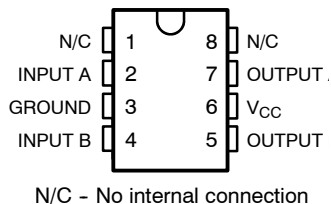
DUAL HIGH-SPEED FET DRIVER

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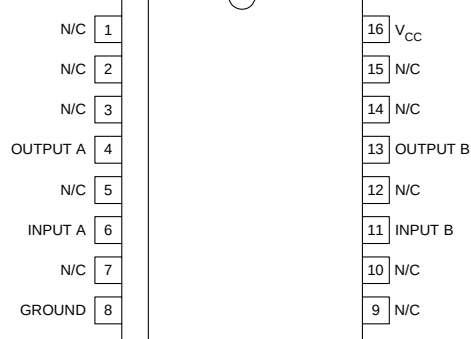
**PLCC-20, LCC-20 (TOP VIEW)
Q, L PACKAGES**



**8 PIN DIL N OR J PACKAGE
(TOP VIEW)**



**SOIC-16 (TOP VIEW)
DW PACKAGE**



**electrical characteristics over recommended operating free-air temperature range, $T_A = 55^\circ\text{C}$ to 125°C for the UC1709, -40°C to 85°C for the UC2709, and 0°C to 70°C for the UC3709;
 $V_{CC} = 20\text{ V}$, $T_A = T_J$.**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	Both outputs low		10	12	mA
	Both outputs high		7	10	mA
Logic 0 input voltage				0.8	V
Logic 1 input voltage		2.2			V
Input current	$V_I = 0$		-0.6	-1.0	mA
Input leakage	$V_I = 5\text{ V}$		0.05	0.1	mA
Output high saturation $V_{CC}-V_O$	$I_O = -50\text{ mA}$		1.5	2.0	V
	$I_O = -500\text{ mA}$		2.0	2.5	V
Output low saturation V_O	$I_O = 50\text{ mA}$		0.1	0.4	V
	$I_O = 500\text{ mA}$		2.0	2.5	V
Thermal shutdown			155		mA

typical switching characteristics, $V_{CC} = 20\text{ V}$, $T_A = 25^\circ\text{C}$, delays measured to 10% output change

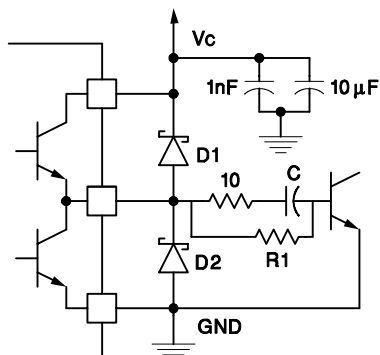
PARAMETER	TEST CONDITIONS	OUTPUT $C_L =$		UNITS
		0 nF	2.2 nF	
Rise time delay		80	80	ns
10% to 90% rise		20	40	ns
Fall time delay		60	80	ns
10% to 90% fall		20	40	ns
VCC cross-conduction current spike duration	Output rise	25		ns
	Output fall	0		ns

NOTE: Refer to UC1705 specifications for further information.



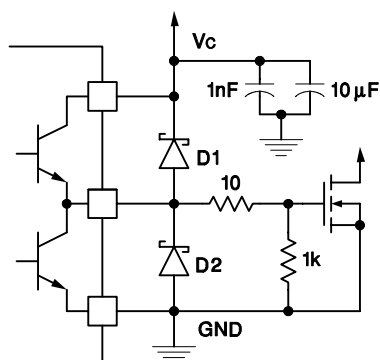
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APPLICATION INFORMATION



D1, D2: UC3611 Schottky Diodes

Figure 1. Power bipolar drive circuit.



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET drive circuit.

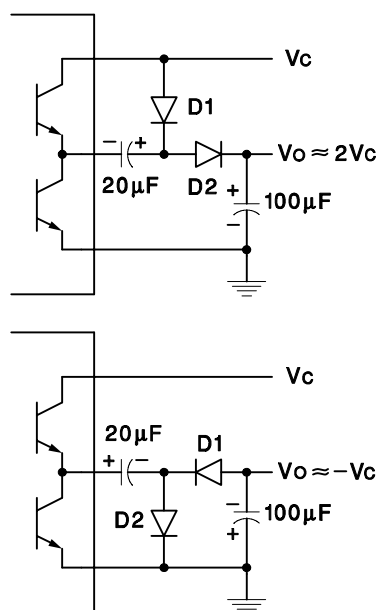


Figure 3. Charge pump circuits.

UC1709, UC2709, UC3709 DUAL HIGH-SPEED FET DRIVER

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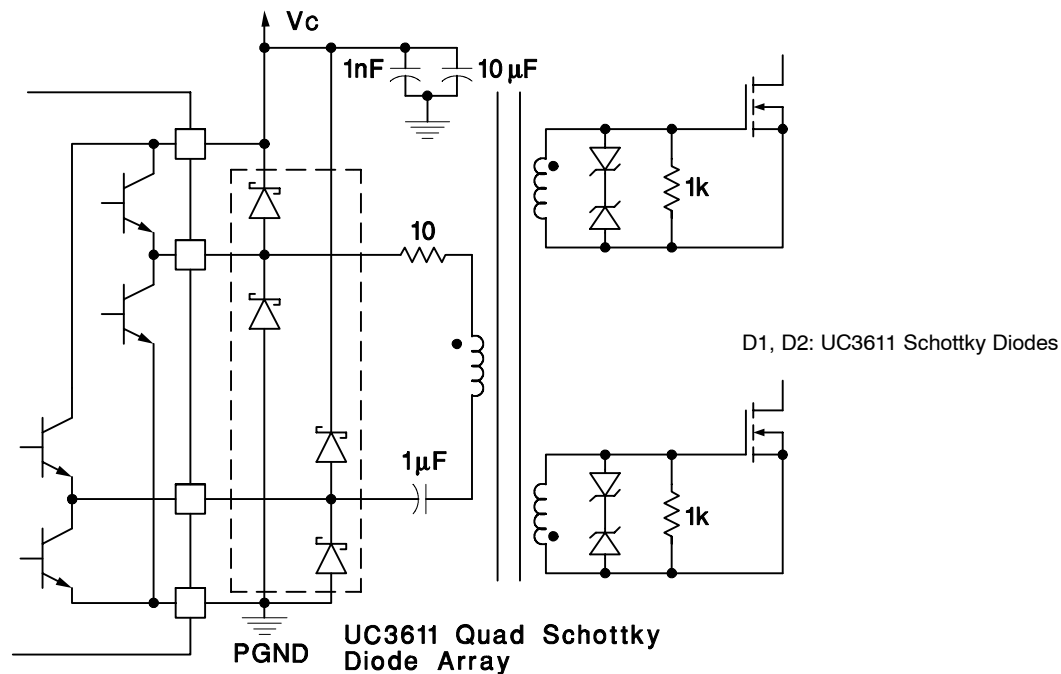


Figure 4. Transformer coupled push-pull MOSFET drive circuit.

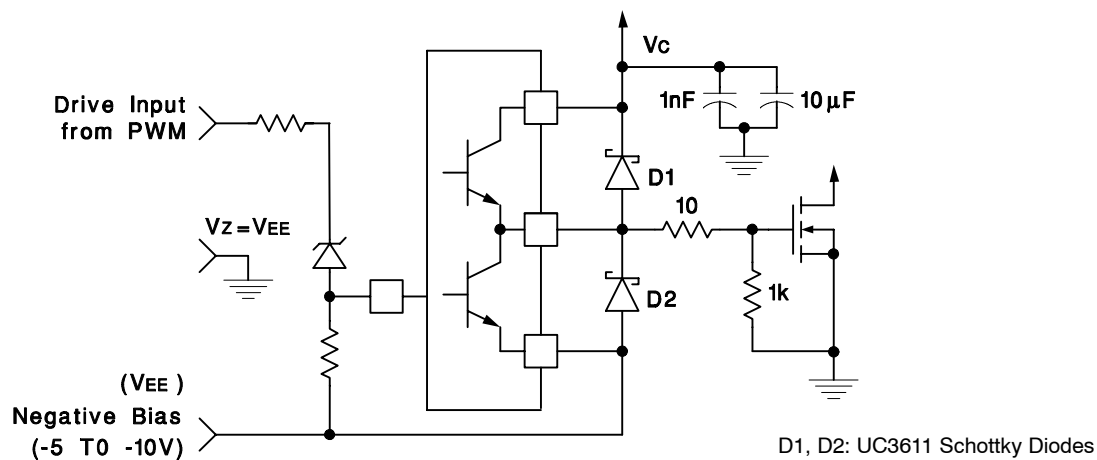
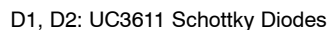


Figure 5. Power MOSFET drive circuit using negative bias voltage and level shifting to ground referenced PWM



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