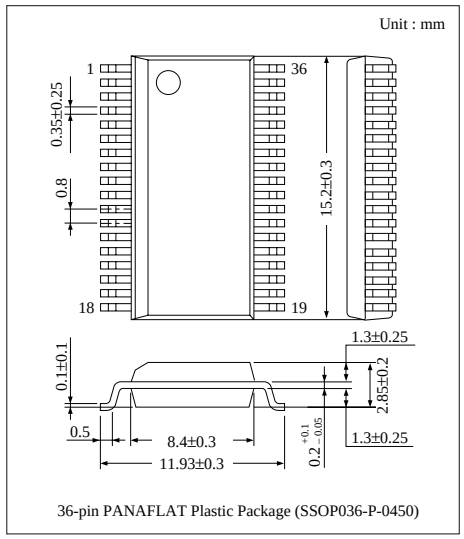
DN8643S

24-bit Shift Register Latch Driver IC

■ Overview

The DN8643S is an IC which incorporates a 24-bit shift register and a latch driver to meet high-speed operation, low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 24-step shift register block and latch block are composed of CMOS, and the 24-step parallel driver block is bipolar.

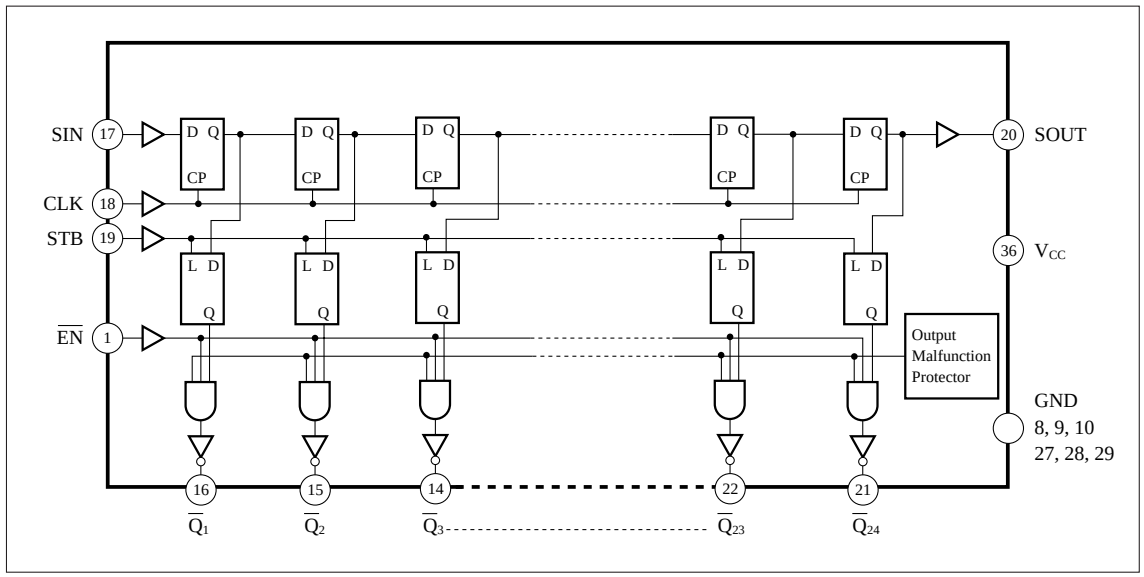


36-pin PANAFLAT Plastic Package (SSOP036-P-0450)

■ Features

- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current at stanby I_{CC}=≤100µA
- High-breakdown, large current drive type output steps
  Breakdown : 30V
  Output current : 120mA
- Surface mountable USONF-36D package (pin pitch : 0.8mm)

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	0 to 7	V
Output voltage	V_O	0 to 30	V
Output current	I_O	120	mA
Power dissipation	P_D	1.3 *	W
Operating ambient temperature	T_{opr}	–20 to + 75	˚C
Storage temperature	T_{stg}	–55 to + 125	˚C

* When mounting onto the PCB, power dissipation is reduced at a rate of 10.4mW/˚C from Ta=25˚C

■ Recommended Operating Range (Ta=25˚C)

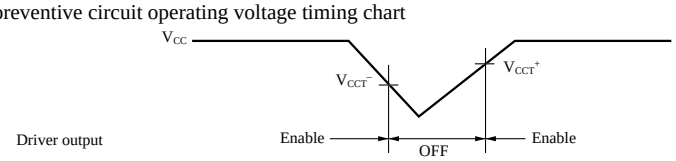
Parameter		Symbol	Condition	mim	typ	max	Unit
Supply voltage		V_{CC}		4	5	6	V
Output voltage		V_O		—	—	30	V
Output current *		I_O		—	—	100	mA
Clock frequency		f_{CLK}	Input Duty 40 to 60%	—	—	10	MHz
Input pulse width	CLK	t_w		40	—	—	ns
	STB			40	—	—	ns
Setup time	SIN	t_{su}		30	—	—	ns
	STB			40	—	—	ns
Hold time	SIN	t_h		20	—	—	ns
	STB			0	—	—	ns
Clock pulse rise time		t_r		—	—	500	ns
Clock pulse fall time		t_f		—	—	500	ns

* An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

■ Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V_{IH}	V_{CC}=4 to 6V	0.7V_{CC}	—	V_{CC}	V
	V_{IL}		0	—	0.3V_{CC}	V
Input current	I_{IH}	V_{IH}=5V	—	—	25	µA
	I_{IL}	V_{IL}=0V	—	—	–25	µA
Output voltage	V_{OH}	I_O= –1µA	4.9	—	—	V
	V_{OL}	I_O=1µA	—	—	0.1	V
Output current	I_{OH}	V_{OH}=4.5V	–4	—	—	mA
	I_{OL}	V_{OL}=0.4V	4	—	—	mA
Output saturation voltage	$V_{CE\ (sat)\ 1}$	I_{OL}=100mA	—	—	0.4	V
	$V_{CE\ (sat)\ 2}$	I_{OL}=80mA	—	—	0.35	V
Output leakage current	I_{OLK1}	V_O=30V (output OFF)	—	—	50	µA
	I_{OLK2}	V_O=15V (output Off)	—	—	25	µA
Supply current	I_{CC1}	Total driver output OFF	—	—	100	µA
	I_{CC2}	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive circuit operating voltage *	V_{CCT^+}		2.9	—	3.9	V
	V_{CCT^-}		2.6	—	3.6	V

* Output malfunctioning preventive circuit operating voltage timing chart

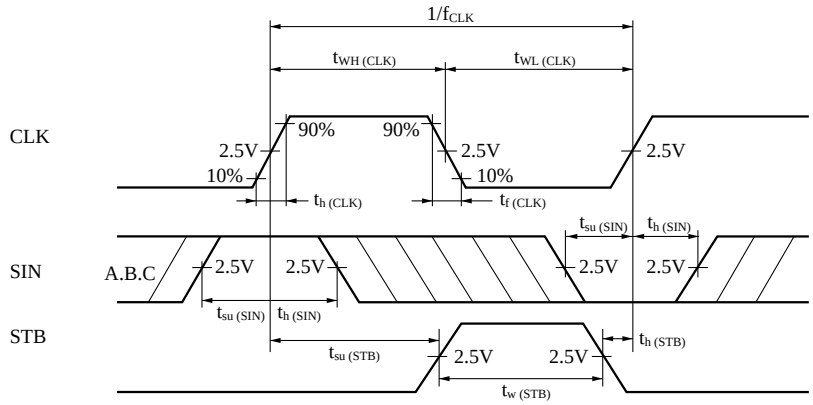


■ Switching Characteristics (Ta=25˚C)

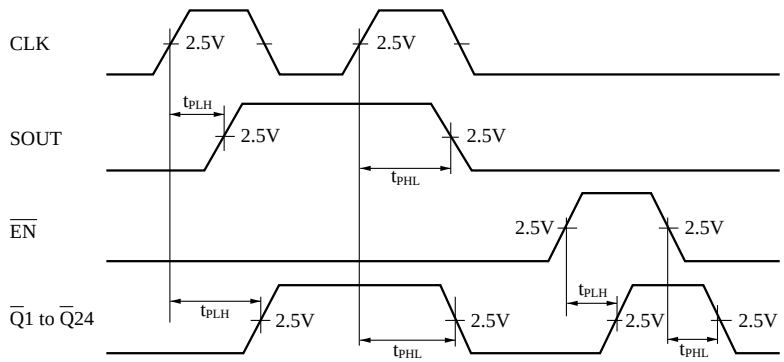
Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	f_{max}	CLK			10	—	—	MHz
Propagation delay time	t_{PLH}	CLK	SOUT	V_{CC}=5V C_L=15pF	—	—	100	ns
	t_{PHL}				—	—	100	ns
	t_{PLH}	CLK	$\overline{Q}n$	V_{CC}=5V R_L=100Ω C_L=15pF	—	—	2	µs
	t_{PHL}				—	—	0.5	µs
	t_{PLH}	$\overline{EN}$	$\overline{Q}n$		—	—	2	µs
	t_{PHL}				—	—	0.5	µs

■ Timing Chart

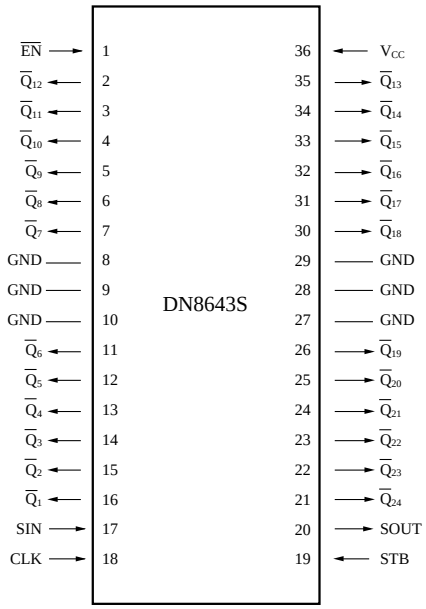
1. Input Timing



2. Propagation Delay Time



■ Pin Assignments



(Top View)

■ Functions Table

Input				Driver output		SOUT
CLK	$\overline{EN}$	STB	SIN	$\overline{Q}_l$	$\overline{Q}_n$	
↑	H	×	×	H	H	Q'_{23}
↓	H	×	×	H	H	nc
↑	L	L	×	nc	nc	Q'_{23}
↑	L	H	L	H	$\overline{Q}_{n-1}$	Q'_{23}
↑	L	H	H	L	$\overline{Q}_{n-1}$	Q'_{23}
↓	L	H	×	nc	nc	nc

Note) H=High level, L=Low level, × = Either “H” or “L” will do, ↑ = Transition from “H” or “L” , ↓ = Transition from “H” to “L” , nc=No change, Q'_{23}=Status of the 23rd shift register