



## Features

- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier ( $P_{out}$  typically 26.5 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF typically 1.8 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components

Electrostatic sensitive device.  
Observe precautions for handling.



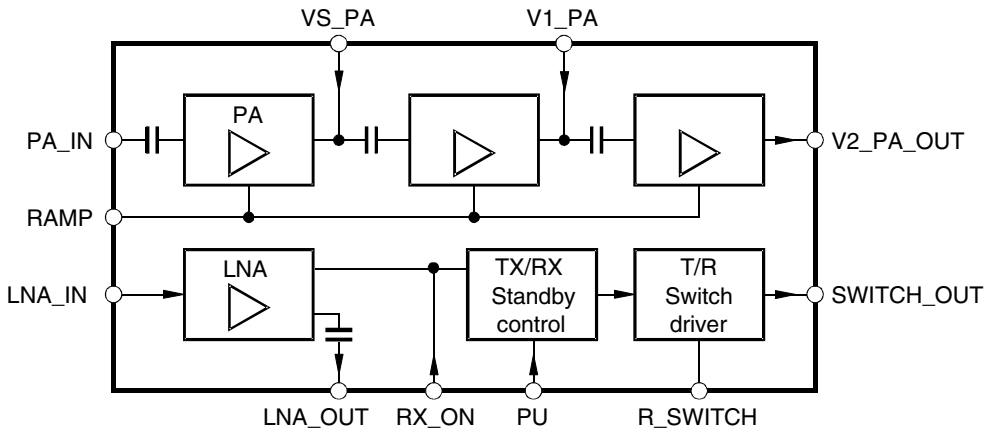
## DECT SiGe Front End IC with High PAE

### U7006B

## Description

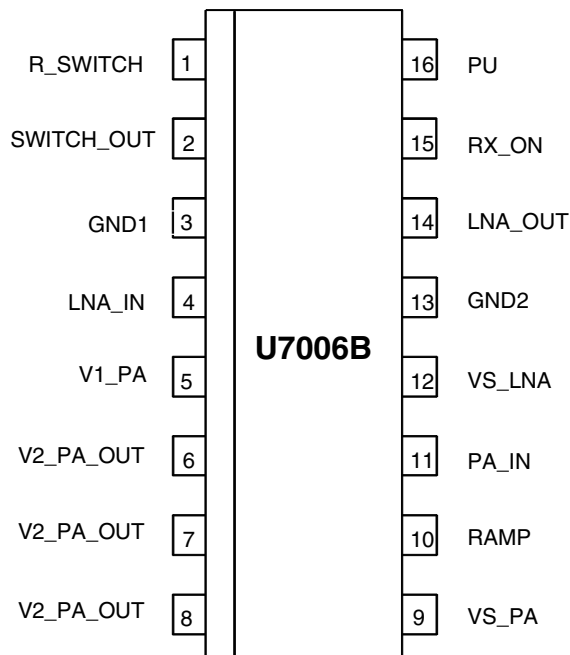
The U7006B is a monolithic SiGe transmit/receive front end IC with power amplifier, 50- $\Omega$  internal matching, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT. Due to the ramp-control feature and a very low quiescent current, an external switch transistor for  $V_S$  is not required.

Figure 1. Block Diagram



## Pin Configuration

Figure 2. Pinning PSSO16



## Pin Description

Pin	Symbol	Function
1	R_SWITCH	Resistor to GND sets the PIN diode current
2	SWITCH_OUT	Switched current output for PIN diode
3	GND1	Ground
4	LNA_IN	Low-noise amplifier input
5	V1_PA	Inductor to power supply for power amplifier
6	V2_PA-OUT	Inductor to power supply and matching network for power amplifier output
7		
8		
9	VS_PA	Supply voltage for power amplifier
10	RAMP	Power-ramping control input
11	PA_IN	Power amplifier input
12	VS_LNA	Supply-voltage input for low-noise amplifier
13	GND2	Ground
14	LNA_OUT	Low-noise amplifier output
15	RX_ON	RX active high
16	PU	Power-up active high

## Absolute Maximum Ratings

All voltages refer to GND (Pins 3 and slug), ESD protection according to ESD-S5.2-1994, Class M1.

Parameters	Symbol	Value	Unit
Supply voltage; pins 6, 10, 13 and 16 (no RF)	$V_S$	5	V
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-40 to +125	°C
Input power PA, Pin 11	$P_{inPA}$	+10	dBm
Input power LNA, Pin 4	$P_{inLNA}$	-5	dBm

## Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	30	K/W

## Operating Range

All voltages refer to GND (Pins 3, 13 and slug). The following table represents the sum of all supply currents depending on the TX/RX mode. Power supply points are VS\_LNA, VS\_PA, V1\_PA, V2\_PA\_OUT.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage pins 5, 6, 7, 8 and 9	$V_S$	2.7	3	4.6	V
Supply voltage pin 12	$V_S$	2.7	3.6	4.6	V
Supply current TX	$I_S$		350		mA
RX	$I_S$		8		mA
Standby current PU = 0	$I_S$		10		µA
Ambient temperature	$T_{amb}$	-25	+25	+70	°C

## Electrical Characteristics

Test conditions (unless otherwise specified):  $V_S = 3\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ , CW mode

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Power Amplifier <sup>(1)</sup></b>						
Supply voltage	Pins 5, 6, 7, 8 and 9	$V_S$	2.7	3	4.6	V
Supply current	TX	$I_{S\_TX}$		350		mA
Supply current	RX (PA off)	$I_{S\_RX}$			10	µA
Standby current	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	$f$	1.88		1.94	GHz
Power gain	TX, pin 11 to pins 6, 7, 8	$G_p$		28		dB
Gain-control range	TX	$\Delta G_p$		48		dB
Ramping voltage	TX, power gain (max), pin 10	$V_{RAMP\ max}$		2.1		V
Ramping current	TX, power gain (max), pin 10	$I_{RAMP}$		0.5	2.0	mA
Power-added efficiency	TX	PAE		40		%

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: TBD
  2. With external matching network (see Figure 13 )
  3. Low-noise amplifier shall be unconditionally stable

## Electrical Characteristics (Continued)

Test conditions (unless otherwise specified):  $V_S = 3\text{ V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ , CW mode

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Saturated output power	TX, referred to pins 6, 7, 8 $V_S = 3.6\text{ V}$	$P_{\text{sat}}$		26.5		dBm
Input matching <sup>(2)</sup>	TX, pin 11	VSWRin		< 2:1		
Output matching <sup>(2)</sup>	TX, pins 6, 7, 8	VSWRout		< 2:1		
Harmonics at P 1dB	TX, pins 6, 7, 8	2 fo 3 fo		-30		dBc
Maximum input power	Pin 11	$P_{\text{inPA}}$		10		dBm
Stability (non harmonic emission)	TX, pin 10 $P_{\text{in}} = 2\text{ dBm}$ , $V_{\text{RAMP}} = 2\text{ V}$ VSWRout < 10:1 (all phases)			-60		dBc
<b>T/R Switch Driver (Currently Programmed by External Resistor from R_SWITCH to GND)</b>						
Switch-out current output	Standby, pin 2	$I_{\text{S\_O\_standby}}$			2	$\mu\text{A}$
	RX	$I_{\text{S\_O\_RX}}$			2	$\mu\text{A}$
	TX at 100 $\Omega$	$I_{\text{S\_O\_100}}$		1		mA
	TX at 1.2 k $\Omega$	$I_{\text{S\_O\_1k2}}$		3		mA
	TX at 33 k $\Omega$	$I_{\text{S\_O\_33k}}$		10		mA
<b>Low-noise Amplifier <sup>(3)</sup></b>						
Supply voltage	All, pin 12	$V_S$	2.7	3.6	4.6	V
Supply current	RX	$I_S$		8		mA
Supply current (LNA and control logic)	TX (control logic active), pin 12	$I_S$		300		$\mu\text{A}$
Standby current	Standby, pin 12	$I_S$		1	10	$\mu\text{A}$
Frequency range	RX	f	1.88		1.94	GHz
Power gain	RX, pin 4 to pin 14	Gp	17	19		dB
Noise figure	RX	NF		1.8	2.0	dB
Gain compression	RX, refer to pin 14	P1dB		-7		dBm
3rd-order input interception point	RX	IIP3		-15		dBm
Input matching	RX	VSWRin		< 2:1		
Output matching	RX	VSWRin		< 2:1		
<b>Logic Input Levels (RX_ON, PU)</b>						
High input level	= 1, pins 5 and 16	$V_{\text{IH}}$	2.4		$V_S$	V
Low input level	= 0	$V_{\text{IL}}$	0		0.5	V
High input current	= 1	$I_{\text{IH}}$		40		$\mu\text{A}$
Low input current	= 0	$I_{\text{IL}}$		0		$\mu\text{A}$

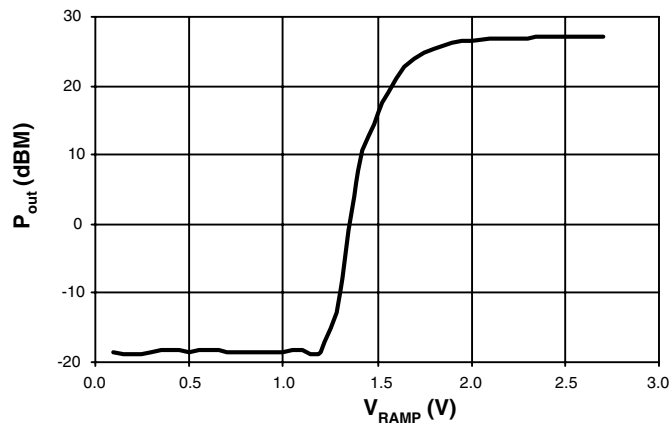
- Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: TBD  
2. With external matching network (see Figure 13 )  
3. Low-noise amplifier shall be unconditionally stable

## Control Logic

**Table 1.** Control Logic for LNA and T/R Switch Driver

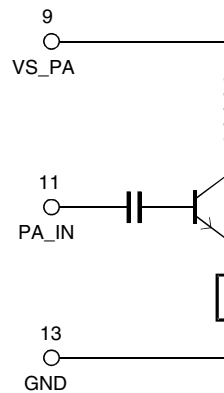
Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

**Figure 3.** Output Power versus Ramp Voltage

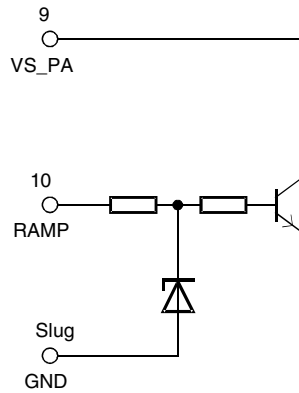


## Input/Output Circuits

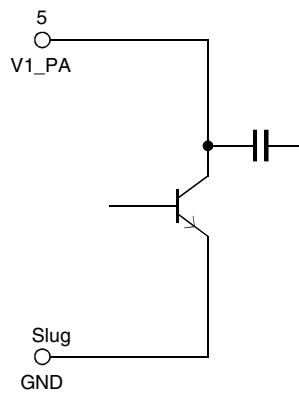
**Figure 4.** Input Circuit PA\_IN/VS\_PA



**Figure 5.** Input Circuit RAMP/VS\_PA



**Figure 6.** Input Circuit V1\_PA



**Figure 7.** Input/Output Circuit V2\_PA

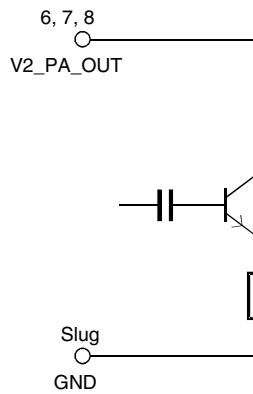


Figure 8. Input Circuit LNA\_IN/VS\_LNA

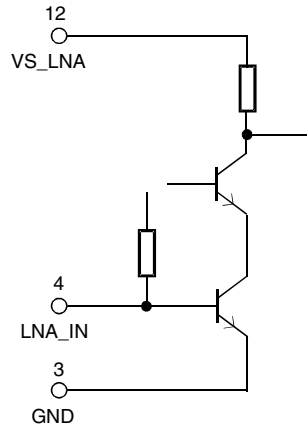
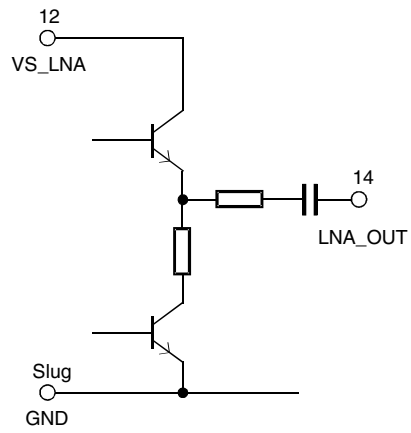
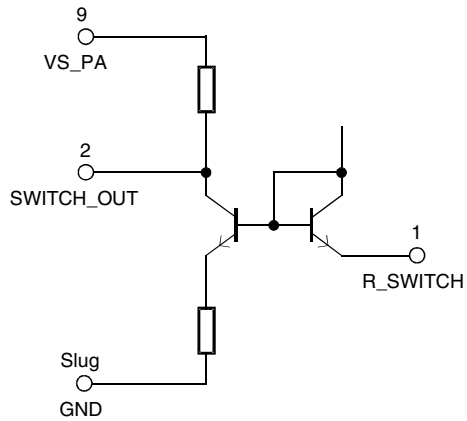


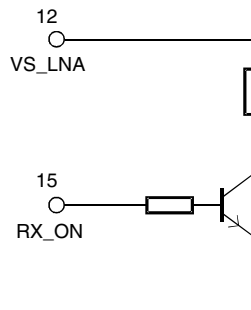
Figure 9. Output Circuit LNA\_OUT



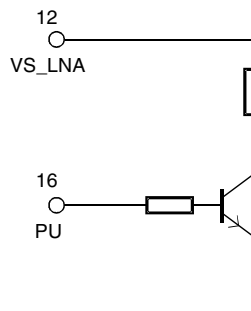
**Figure 10.** Input Circuit SWITCH\_OUT/R\_SWITCH



**Figure 11.** Input Circuit RX\_ON



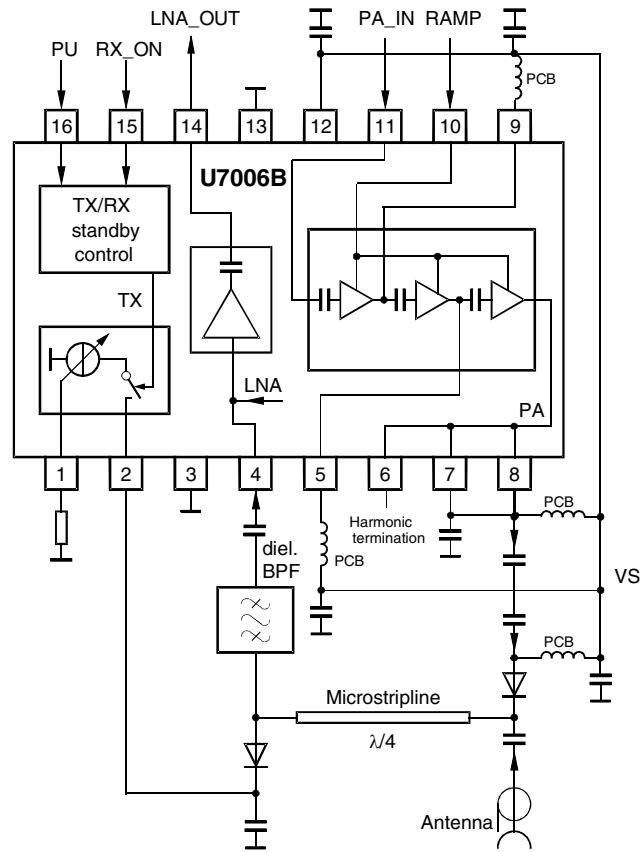
**Figure 12.** Input Circuit PU



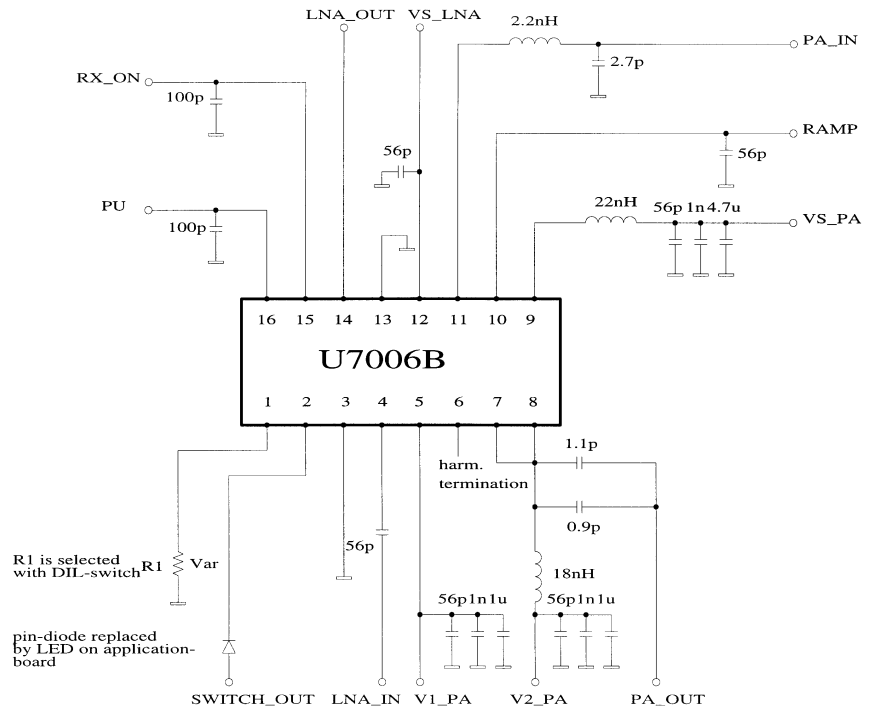


# Typical Application Circuit

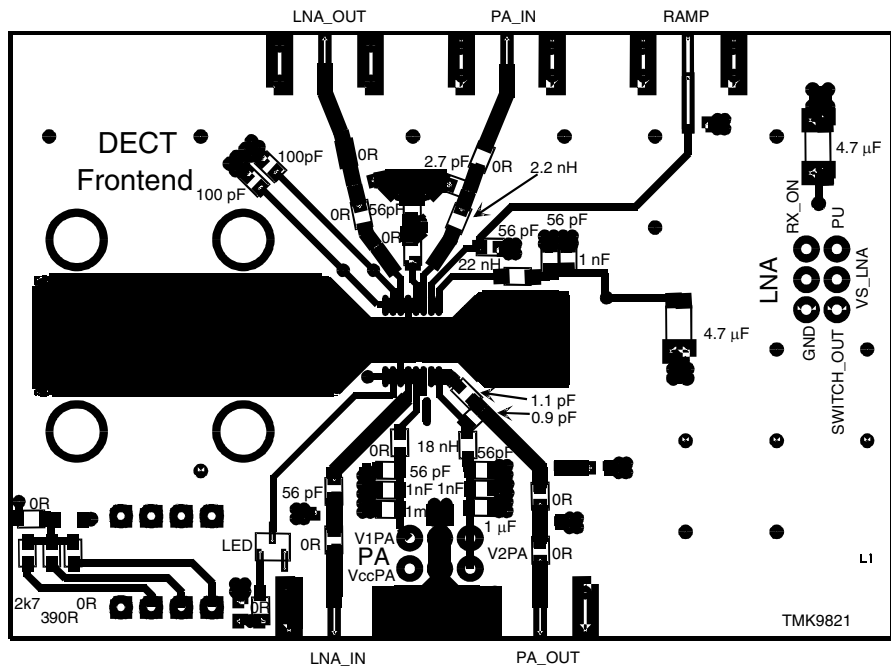
Figure 13. Typical Schematic



**Figure 14. U7006B Application Board Schematic**



**Figure 15. U7006B Application Board Layout**



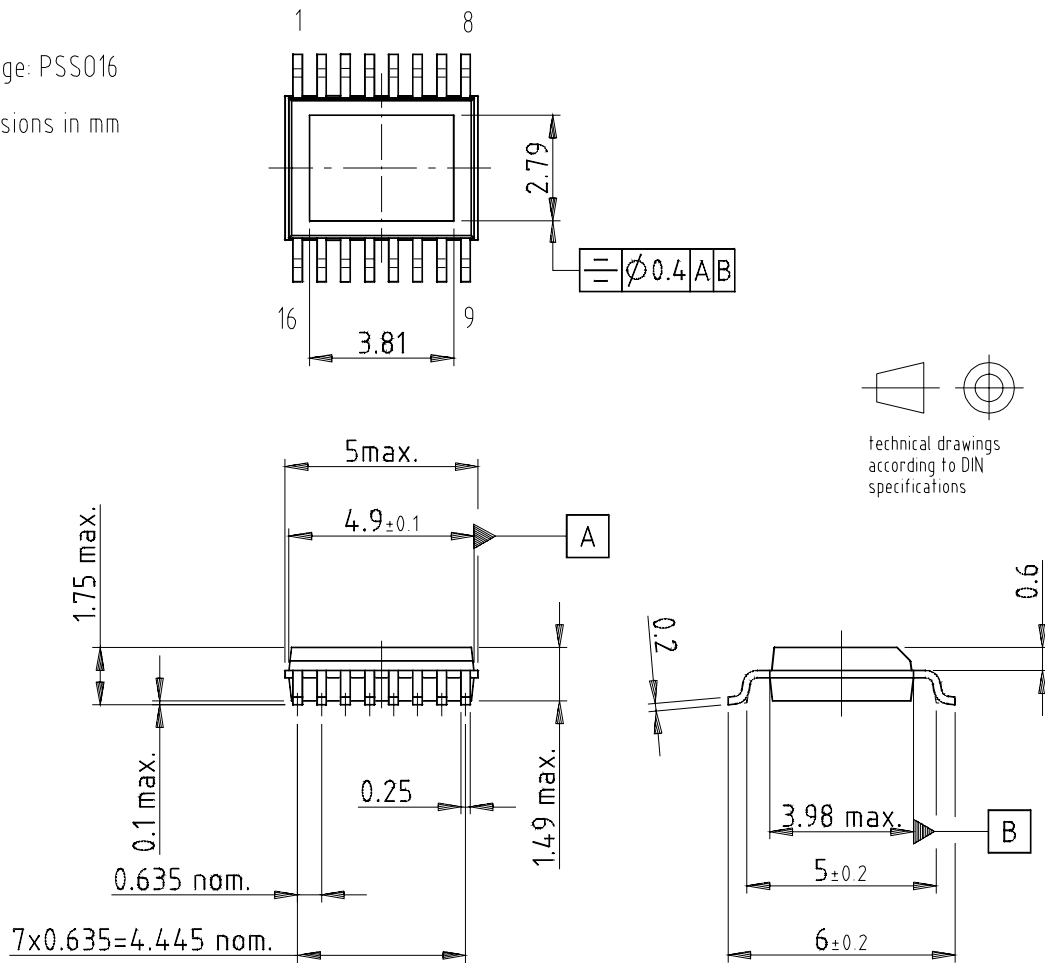
### Ordering Information

Extended Type Number	Package	Remarks
U7006B-MLB	PSSO16	Tube
U7006B-MLBG3	PSSO16	Taped and reeled

### Package Information

Package: PSSO16

Dimensions in mm



Drawing-No.: 6.543-5067.01-4

Issue: 3; 08.08.00



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenaux 41  
Case Postale 80  
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Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
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Hong Kong  
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Fax: (852) 2722-1369

### Japan

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1-24-8 Shinkawa  
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Japan  
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Fax: (81) 3-3523-7581

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### e-mail

[literature@atmel.com](mailto:literature@atmel.com)

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