



N-Channel 30-V (D-S) MOSFET

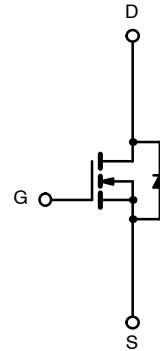
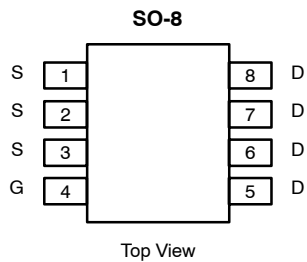
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0125 @ $V_{GS} = 10$ V	11
	0.014 @ $V_{GS} = 4.5$ V	10

FEATURES

- TrenchFET® Gen II Power MOSFET

APPLICATIONS

- High-Side DC/DC Conversion
 - Notebook
 - Desktop
 - Server
- Notebook Logic DC/DC, Low-Side



Ordering Information: Si4348DY—E3 (Lead Free)
Si4348DY-T1—E3 (Lead Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	11	8.0
		$T_A = 70^\circ\text{C}$	8.9	6.5
Pulsed Drain Current	I_{DM}	40		A
Continuous Source Current (Diode Conduction) ^a	I_S	2.2	1.20	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5	1.31
		$T_A = 70^\circ\text{C}$	1.6	0.84
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	43	50
		Steady State	74	95
Maximum Junction-to-Foot (Drain)	R_{thJF}	19	25	$^\circ\text{C/W}$

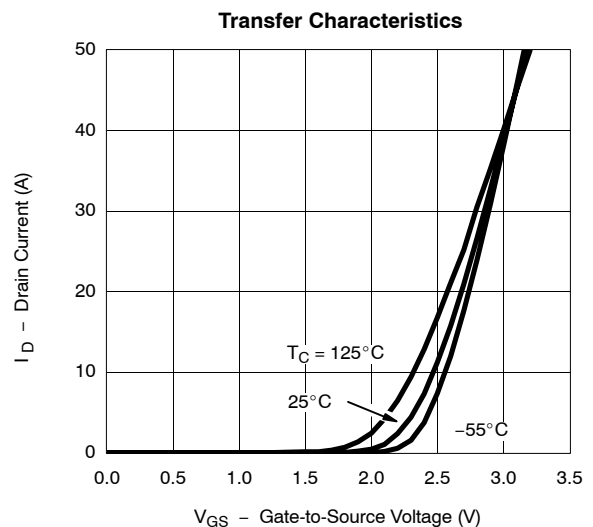
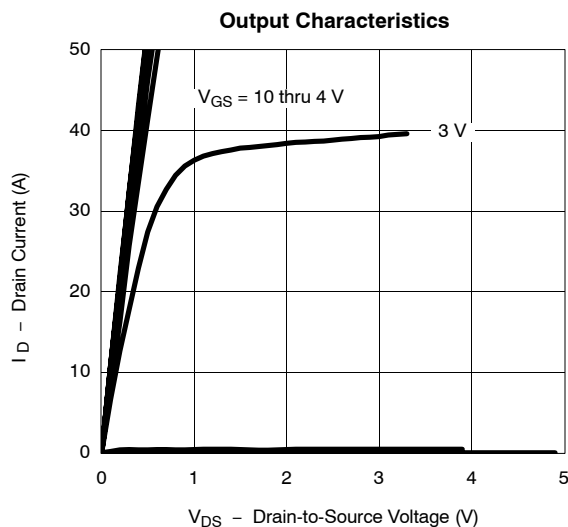
Notes
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8		2.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 11 A		0.0105	0.0125	Ω
		V _{GS} = 4.5 V, I _D = 10 A		0.0115	0.014	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 11 A		40		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.2 A, V _{GS} = 0 V		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 11 A		15	23	nC
Gate-Source Charge	Q _{gs}		5			
Gate-Drain Charge	Q _{gd}		4.3			
Gate Resistance	R _g			0.5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		10	15	ns
Rise Time	t _r		11	17		
Turn-Off Delay Time	t _{d(off)}		55	85		
Fall Time	t _f		9	15		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.2 A, di/dt = 100 A/μs		22	35	

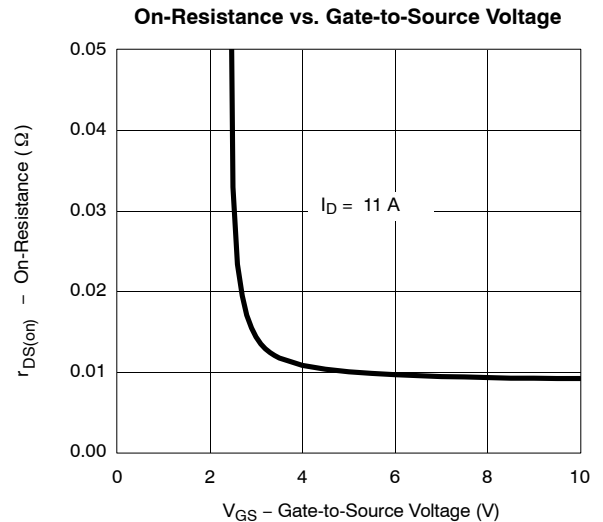
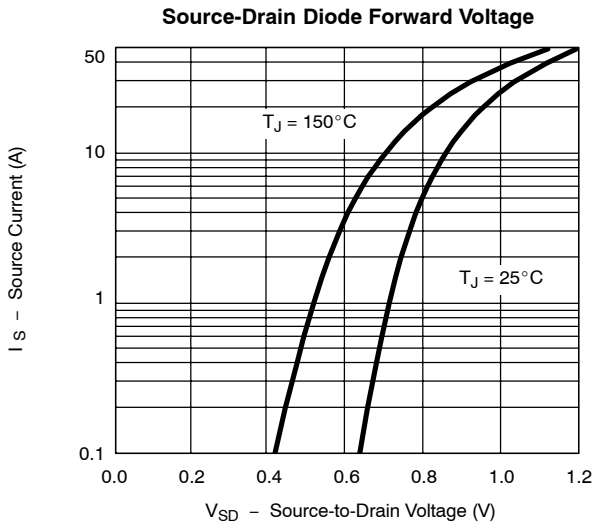
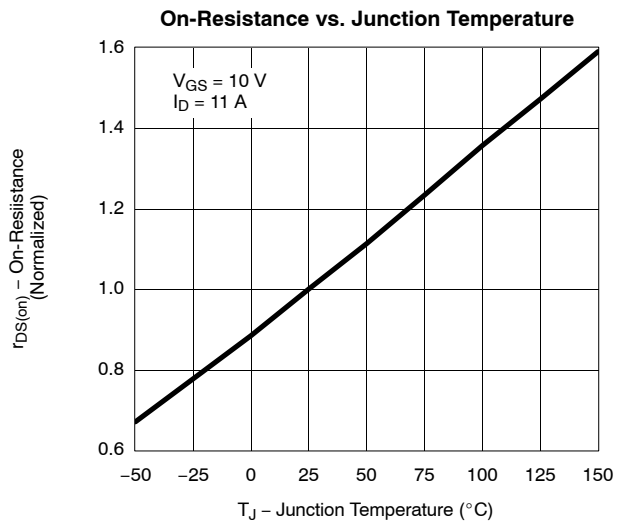
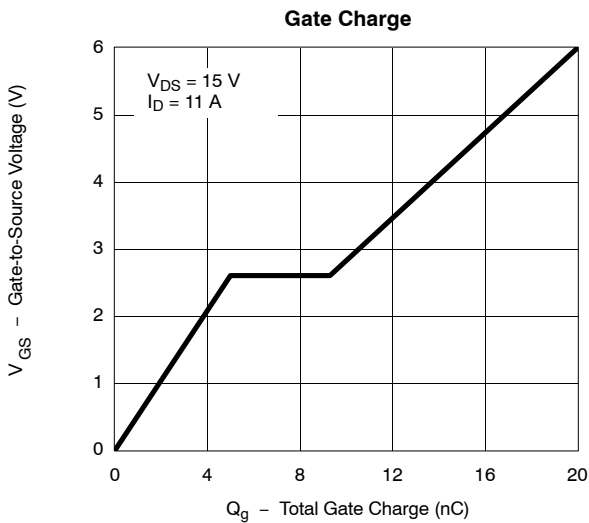
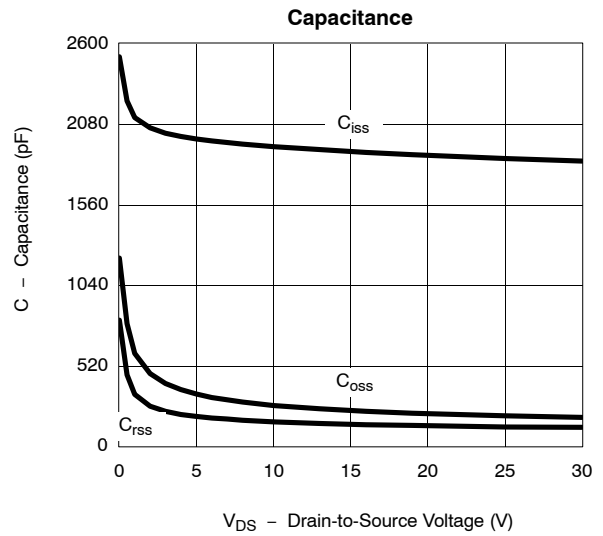
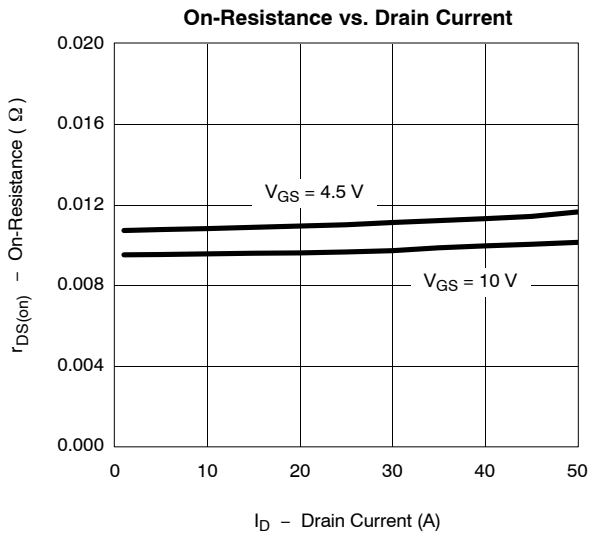
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

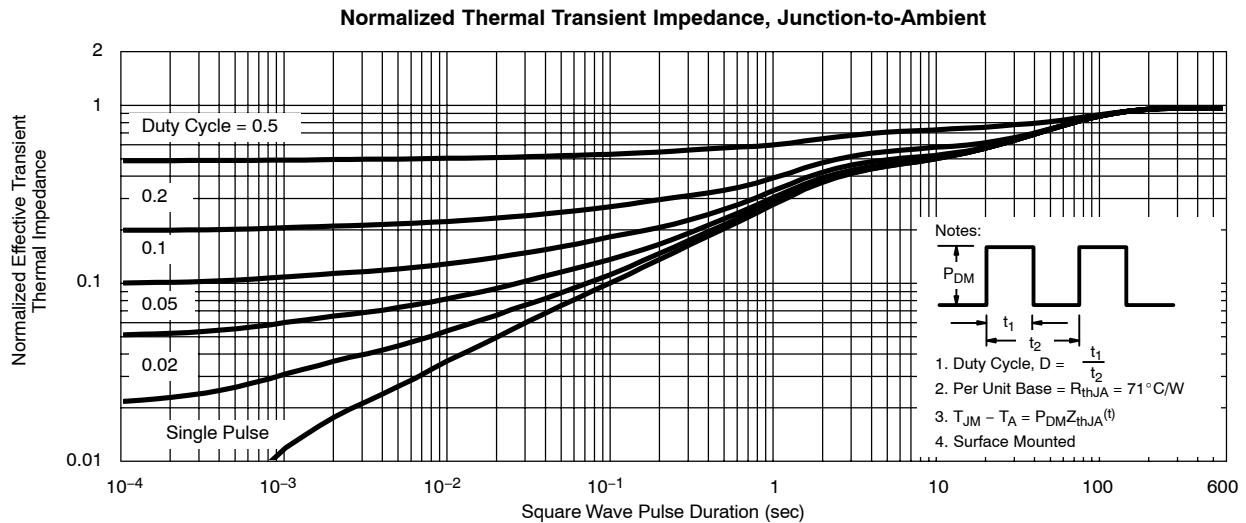
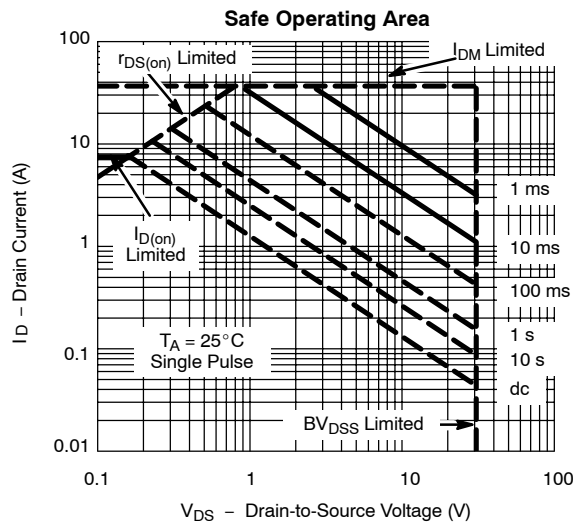
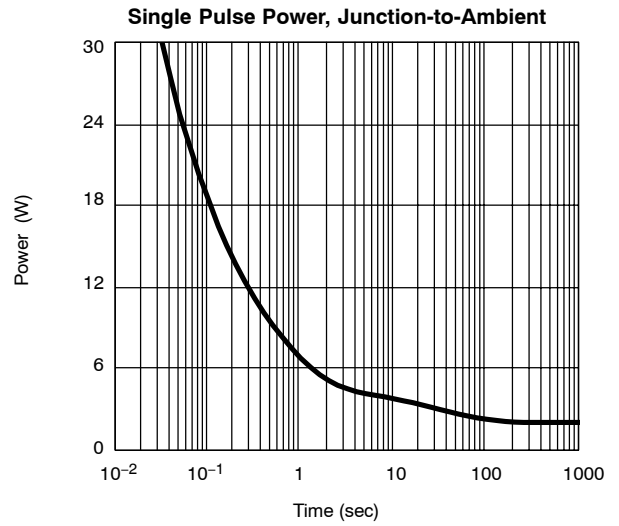
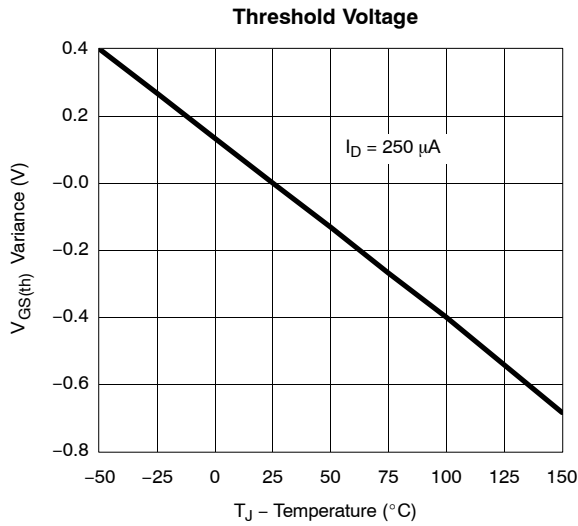


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