1-Mbit (64K x 16) Static RAM

Features

- **Temperature Ranges**
  - **— Commercial: 0°C to 70°C**
  - **— Industrial: –40°C to 85°C**
  - **— Automotive: –40°C to 125°C**
- **High speed**
  - **— t_{AA} = 12 ns (Commercial & Industrial)**
  - **— t_{AA} = 15 ns (Automotive)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 770 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in Pb-free and non Pb-free 44-pin TSOP II and 44-pin 400-mil-wide SOJ**

Functional Description[1]

The CY7C1021B is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

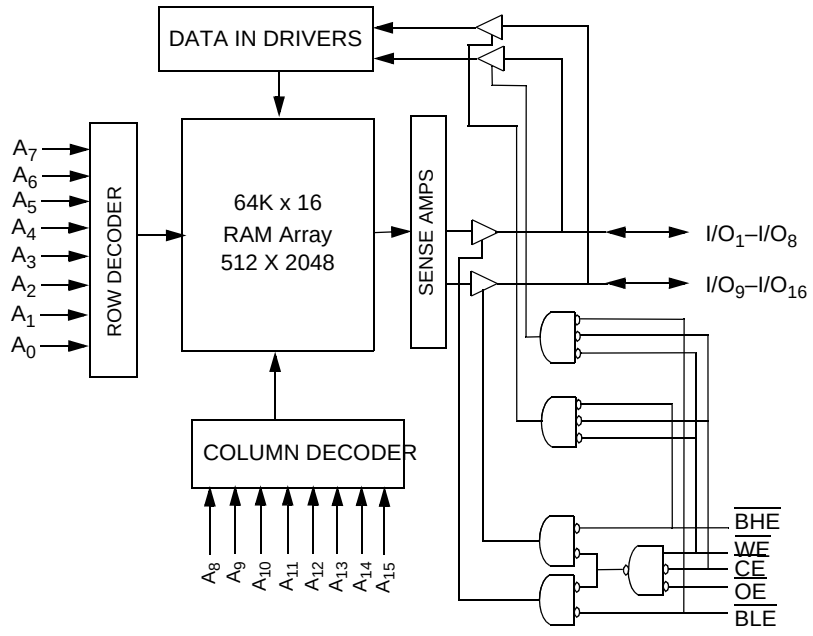
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1021B is available in standard 44-pin TSOP Type II and 44-pin 400-mil-wide SOJ packages.

Logic Block Diagram



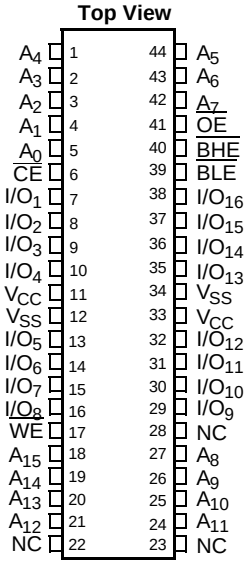
Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Selection Guide

		-12	-15
Maximum Access Time (ns)		12	15
Maximum Operating Current (mA)	Com'l/Ind'l	140	130
	Automotive		130
Maximum CMOS Standby Current (mA)	Com'l/Ind'l	10	10
	Automotive		15
	L Version	0.5	0.5

Pin Configurations

SOJ/TSOP II
Top View



Pin Definitions

Pin Name	SOJ, TSOP–Pin Number	I/O Type	Description
A_0–A_{15}	1–5,18–21, 24–27, 42–44	Input	**Address Inputs used to select one of the address locations.**
I/O_1–I/O_{16}	7–10, 13–16, 29–32, 35–38	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	**No Connect**s. Not connected to the die.
$\overline{WE}$	17	Input/Control	**Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{CE}$	6	Input/Control	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	Input/Control	**Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls I/O_{16}–I/O_9, $\overline{BLE}$ controls I/O_8–I/O_1.
$\overline{OE}$	41	Input/Control	**Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V_{SS}	12, 34	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	11, 33	Power Supply	**Power Supply inputs to the device.**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .....–0.5V to V_{CC}+0.5V

DC Input Voltage[2].....–0.5V to V_{CC}+0.5V

Current into Outputs (LOW) .....20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature (T_A)[3]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Automotive	–40°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Com'l/Ind'l	–1	+1	–1	+1	µA
			Auto			–4	+4	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	Com'l/Ind'l	–1	+1	–1	+1	µA
			Auto			–4	+4	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l/Ind'l		140		130	mA
			Auto				130	mA
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		40		40	mA
			Auto				50	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		10		10	mA
			Auto				15	mA
			L Version		0.5		0.5	mA

Capacitance[4]

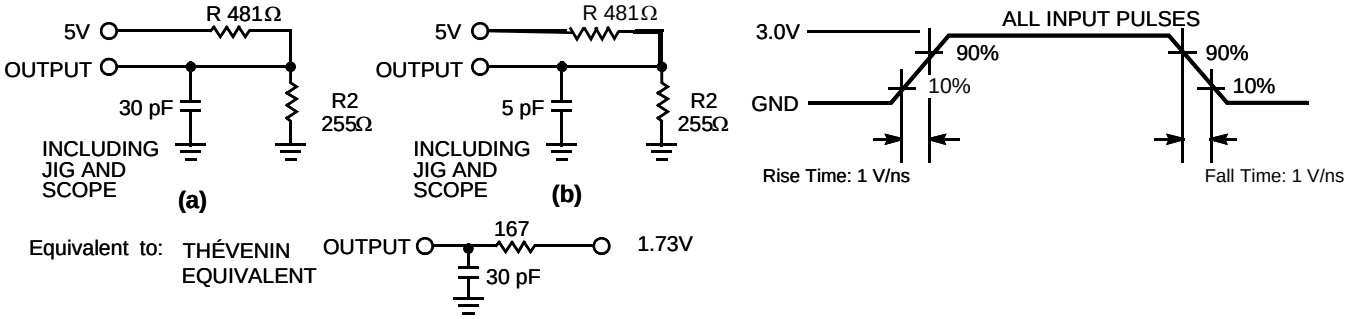
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[4]

Parameter	Description	Test Conditions	44-pin SOJ	44-pin TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	64.32	76.89	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		31.03	14.28	°C/W

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
3. T_A is the "Instant On" case temperature.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



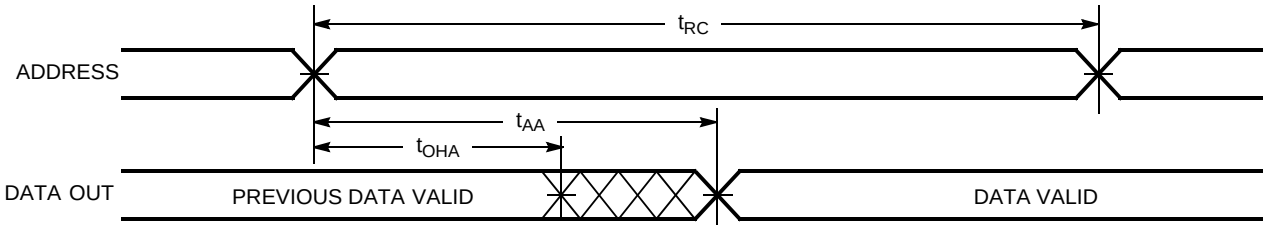
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C1021B-12		7C1021B-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15	ns
t_{DBE}	Byte Enable to Data Valid		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		6		7	ns
Write Cycle[8]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{SD}	Data Set-Up to Write End	6		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		7	ns
t_{BW}	Byte Enable to End of Write	8		9		ns

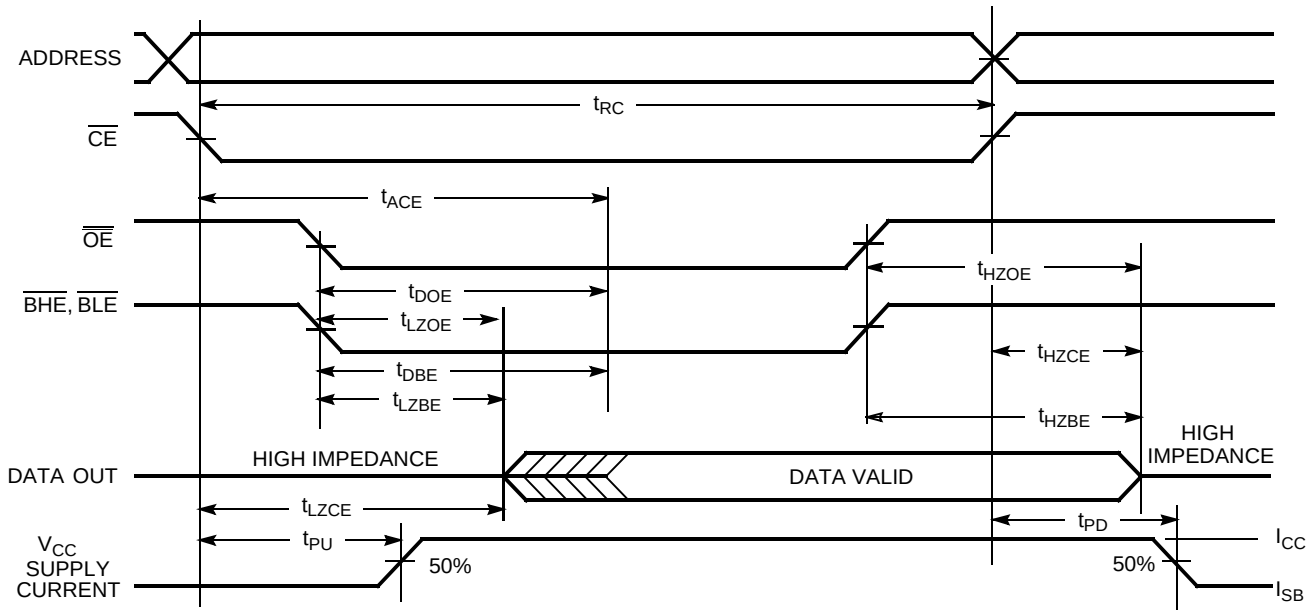
Notes:
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}/\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1[9, 10]



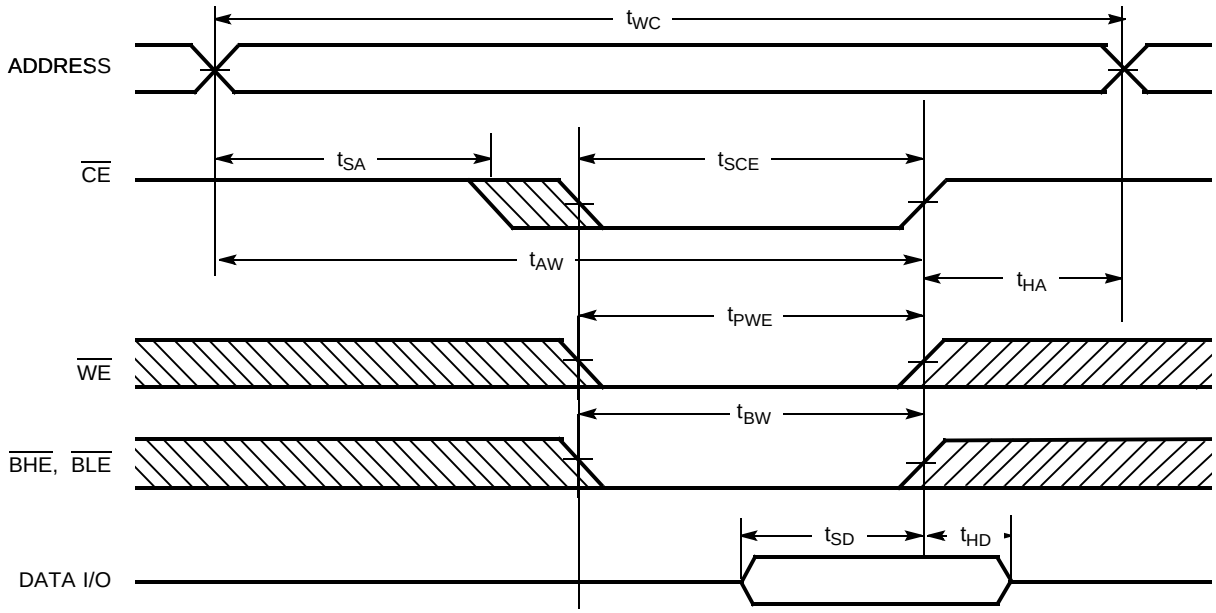
Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



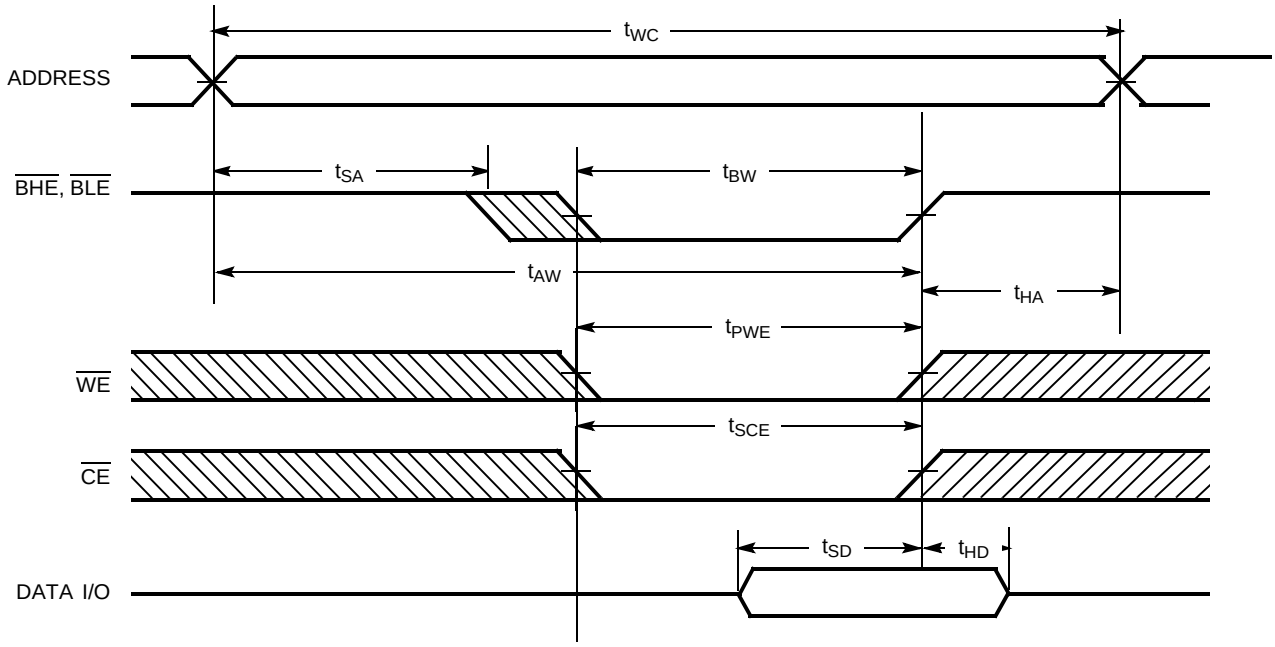
Notes:
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]



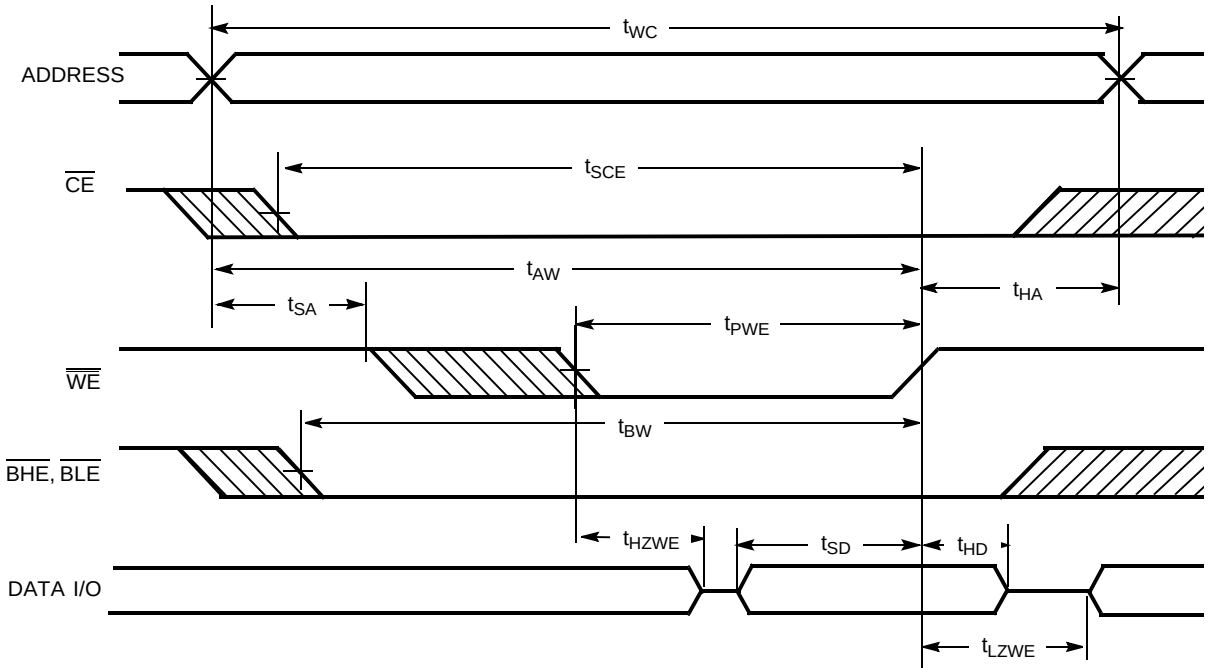
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes:
12. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_1–I/O_8$	$I/O_9–I/O_{16}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

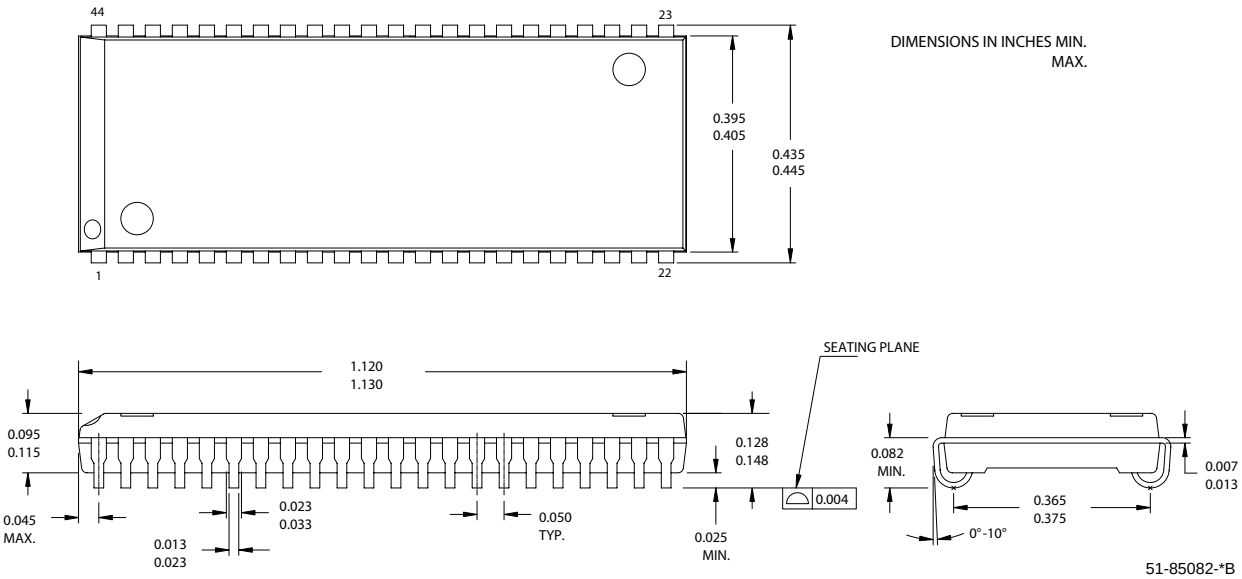
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1021B-12VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021B-12VXC		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021B-12ZC	51-85087	44-pin TSOP Type II	
	CY7C1021B-12ZXC		44-pin TSOP Type II (Pb-Free)	
	CY7C1021B-12VI	51-85082	44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021B-12VXI		44-pin (400-Mil) Molded SOJ (Pb-Free)	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021B-15VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021B-15VXC		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021B-15ZC	51-85087	44-pin TSOP Type II	
	CY7C1021B-15ZXC		44-pin TSOP Type II (Pb-Free)	
	CY7C1021B-15VI	51-85082	44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021B-15VXI		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021B-15ZI	51-85087	44-pin TSOP Type II	
	CY7C1021BL-15ZI		44-pin TSOP Type II	
	CY7C1021B-15ZXI		44-pin TSOP Type II (Pb-Free)	
	CY7C1021BL-15ZXI		44-pin TSOP Type II (Pb-Free)	
	CY7C1021B-15VE	51-85082	44-pin (400-Mil) Molded SOJ	Automotive
	CY7C1021B-15VXE		44-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1021B-15ZE	51-85087	44-pin TSOP Type II	
	CY7C1021B-15ZSXE		44-pin TSOP Type II (Pb-Free)	

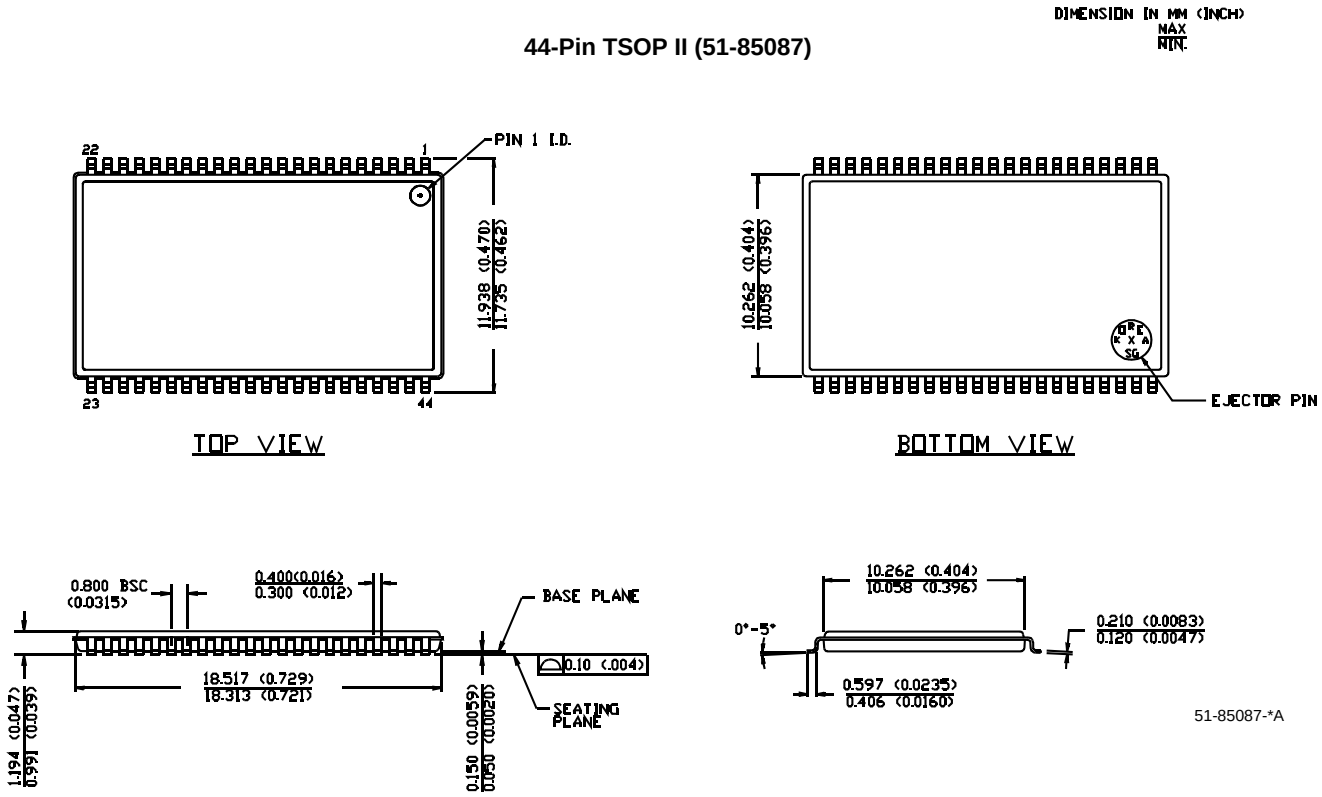
Package Diagrams

44-pin (400-Mil) Molded SOJ (51-85082)



Package Diagrams (continued)

44-Pin TSOP II (51-85087)



Document History Page

Document Title: CY7C1021B 1-Mbit (64K x 16) Static RAM Document Number: 38-05145				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109889	09/22/01	SZV	Change from Spec number: 38-00951 to 38-05145
*A	238454	See ECN	RKF	1) Added Automotive Specs to Data Sheet 2) Added Pb-Free device offering in the Ordering Information
*B	361795	See ECN	SYT	Added Pb-Free offerings in the Ordering Information
*C	505726	See ECN	NXR	Removed CY7C10211B from Product offering Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Changed teh I_{CC} Max value from 150 mA to 130 mA Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table