

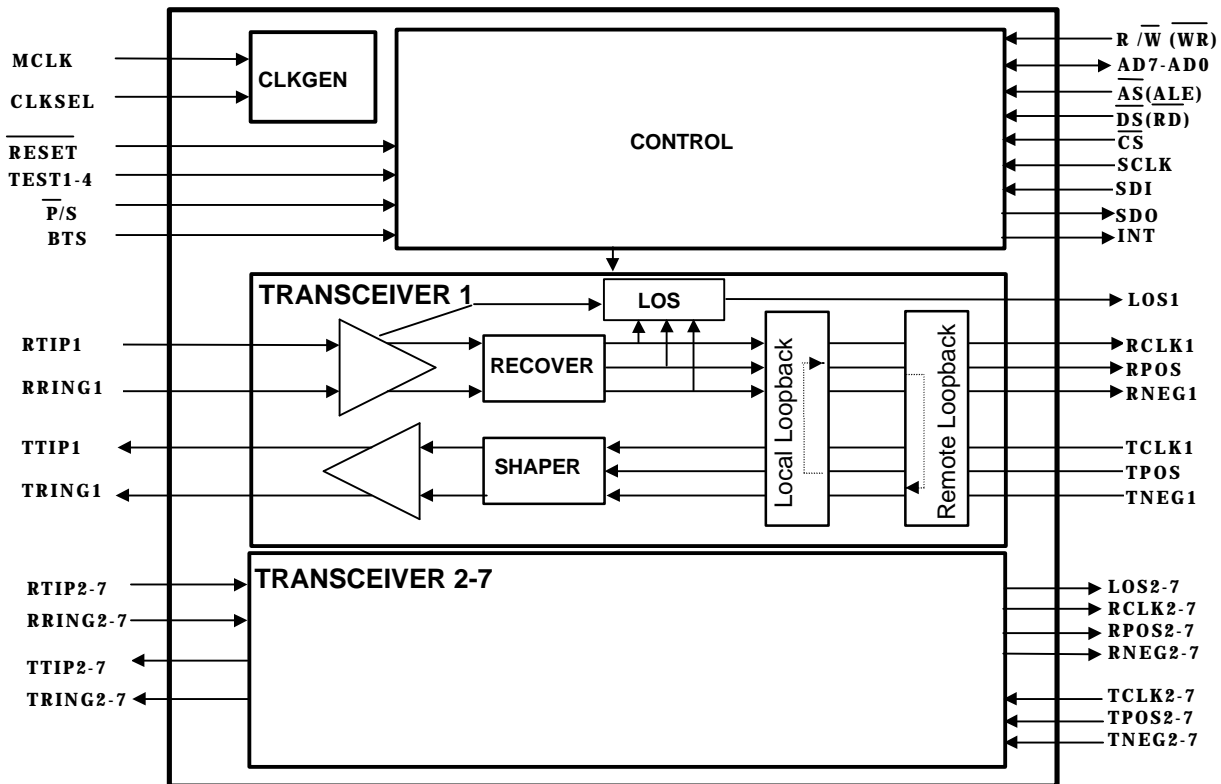
# AK2548

## 7 channel E1 Transceiver

### FEATURE

- 7ch E1 transceiver
- Jitter Tolerance: Compliant with ITU-T G.823, I.431
- Transmitter Pulse Shape: Compliant with ITU-T G.703
- Loss of Signal Detection: Compliant with ITU-T G.775
- Return loss: Compliant with ETS 300 166
- Selectable Signal Polarity
- Local/Remote Loopback
- Parallel/Serail Microprocessor Interface
- Single 3.3V±5% Operation
- Low Power Consumption
- Pin-to-pin compatible with AK2546(7 channel T1 transceiver) except serial interface
- Small Plastic Package 144pin LQFP

### BLOCK DIAGRAM

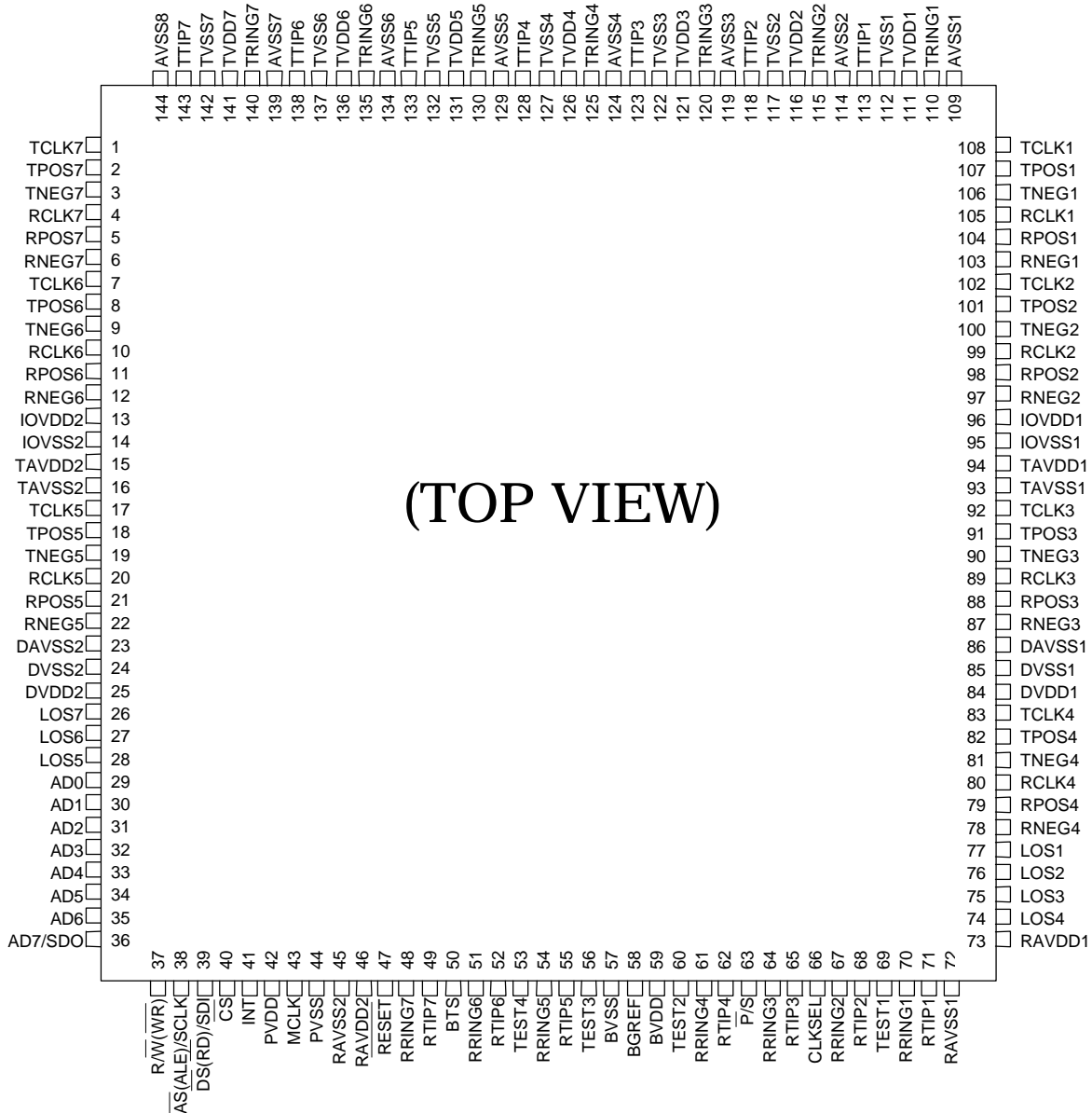


7 Channel E1 Transceiver Block Diagram

**GENERAL DESCRIPTION**

The AK2548 is the 7 channel E1 transceiver for a SDH/SONET MUX, M13 MUX, etc. It includes seven independent transmitters, clock and data recovery, LOS detector, control circuit in one LQFP-144 package which saves space, power consumption and the board design time. Internally generated transmit pulse provides the appropriate pulse shape.

**PIN ASSIGNMENTS**



## PIN CONDITION

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
1	TCLK7	I	CMOS			
2	TPOS7	I	CMOS			
3	TNEG7	I	CMOS			
4	RCLK7	O	CMOS	≤15pF		
5	RPOS7	O	CMOS	≤15pF		
6	RNEG7	O	CMOS	≤15pF		
7	TCLK6	I	CMOS			
8	TPOS6	I	CMOS			
9	TNEG6	I	CMOS			
10	RCLK6	O	CMOS	≤15pF		
11	RPOS6	O	CMOS	≤15pF		
12	RNEG6	O	CMOS	≤15pF		
13	IOVDD2	I	Power			
14	IOVSS2	I	Power			
15	TAVDD2	I	Power			
16	TAVSS2	I	Power			
17	TCLK5	I	CMOS			
18	TPOS5	I	CMOS			
19	TNEG5	I	CMOS			
20	RCLK5	O	CMOS	≤15pF		
21	RPOS5	O	CMOS	≤15pF		
22	RNEG5	O	CMOS	≤15pF		
23	DAVSS2	I	Power			
24	DVSS2	I	Power			
25	DVDD2	I	Power			
26	LOS7	O	CMOS	≤15pF		
27	LOS6	O	CMOS	≤15pF		
28	LOS5	O	CMOS	≤15pF		
29	AD0	I/O	CMOS	≤50pF		
30	AD1	I/O	CMOS	≤50pF		
31	AD2	I/O	CMOS	≤50pF		
32	AD3	I/O	CMOS	≤50pF		
33	AD4	I/O	CMOS	≤50pF		
34	AD5	I/O	CMOS	≤50pF		
35	AD6	I/O	CMOS	≤50pF		
36	AD7/SDO	I/O	CMOS	≤50pF		

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
37	R/W(WR)	I	CMOS			
38	$\overline{AS}$ (ALE)/SCLK	I	CMOS			
39	$\overline{DS}$ ( $\overline{RD}$ )/SDI	I	CMOS			
40	$\overline{CS}$	I	CMOS			
41	INT	O	Open drain			PMOS open drain
42	PVDD	I	Power			
43	MCLK	I	CMOS			
44	PVSS	I	Power			
45	RAVSS2	I	Power			
46	RAVDD2	I	Power			
47	$\overline{RESET}$	I	CMOS			
48	RRING7	I	Analog			
49	RTIP7	I	Analog			
50	BTS	I	CMOS			
51	RRING6	I	Analog			
52	RTIP6	I	Analog			
53	TEST4	I	CMOS			Note 1
54	RRING5	I	Analog			
55	RTIP5	I	Analog			
56	TEST3	I	CMOS			Note 1
57	BVSS	I	Power			
58	BGREF	O	Analog		12k $\Omega$	$\pm 1\%$ accuracy
59	BVDD	I	Power			
60	TEST2	I	CMOS			Note 1
61	RRING4	I	Analog			
62	RTIP4	I	Analog			
63	$\overline{P/S}$	I	CMOS			
64	RRING3	I	Analog			
65	RTIP3	I	Analog			
66	CLKSEL	I	CMOS			
67	RRING2	I	Analog			
68	RTIP2	I	Analog			
69	TEST1	I	CMOS			Note 1
70	RRING1	I	Analog			
71	RTIP1	I	Analog			
72	RAVSS1	I	Power			

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
73	RAVDD1	I	Power			
74	LOS4	O	CMOS	≤15pF		
75	LOS3	O	CMOS	≤15pF		
76	LOS2	O	CMOS	≤15pF		
77	LOS1	O	CMOS	≤15pF		
78	RNEG4	O	CMOS	≤15pF		
79	RPOS4	O	CMOS	≤15pF		
80	RCLK4	O	CMOS	≤15pF		
81	TNEG4	I	CMOS			
82	TPOS4	I	CMOS			
83	TCLK4	I	CMOS			
84	DVDD1	I	Power			
85	DVSS1	I	Power			
86	DAVSS1	I	Power			
87	RNEG3	O	CMOS	≤15pF		
88	RPOS3	O	CMOS	≤15pF		
89	RCLK3	O	CMOS	≤15pF		
90	TNEG3	I	CMOS			
91	TPOS3	I	CMOS			
92	TCLK3	I	CMOS			
93	TAVSS1	I	Power			
94	TAVDD1	I	Power			
95	IOVSS1	I	Power			
96	IOVDD1	I	Power			
97	RNEG2	O	CMOS	≤15pF		
98	RPOS2	O	CMOS	≤15pF		
99	RCLK2	O	CMOS	≤15pF		
100	TNEG2	I	CMOS			
101	TPOS2	I	CMOS			
102	TCLK2	I	CMOS			
103	RNEG1	O	CMOS	≤15pF		
104	RPOS1	O	CMOS	≤15pF		
105	RCLK1	O	CMOS	≤15pF		
106	TNEG1	I	CMOS			
107	TPOS1	I	CMOS			
108	TCLK1	I	CMOS			

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
109	AVSS1	I	Power			
110	TRING1	O	Analog			driver output
111	TVDD1	I	Power			
112	TVSS1	I	Power			
113	TTIP1	O	Analog			driver output
114	AVSS2	I	Power			
115	TRING1	O	Analog			driver output
116	TVDD2	I	Power			
117	TVSS2	I	Power			
118	TTIP2	O	Analog			driver output
119	AVSS3	I	Power			
120	TRING3	O	Analog			driver output
121	TVDD3	I	Power			
122	TVSS3	I	Power			
123	TTIP3	O	Analog			driver output
124	AVSS4	I	Power			
125	TRING4	O	Analog			driver output
126	TVDD4	I	Power			
127	TVSS4	I	Power			
128	TTIP4	O	Analog			driver output
129	AVSS5	I	Power			
130	TRING5	O	Analog			driver output
131	TVDD5	I	Power			
132	TVSS5	I	Power			
133	TTIP5	O	Analog			driver output
134	AVSS6	I	Power			
135	TRING6	O	Analog			driver output
136	TVDD6	I	Power			
137	TVSS6	I	Power			
138	TTIP6	O	Analog			driver output
139	AVSS7	I	Power			
140	TRING7	O	Analog			driver output
141	TVDD7	I	Power			
142	TVSS7	I	Power			
143	TTIP7	O	Analog			driver output
144	AVSS8	I	Power			

Note 1) Should be connected to VSS externally.

<b>PIN FUNCTION</b>
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Pin Name	I/O	Function	Comment
<b>E1 Transceiver</b>			
TTIP1-7	O	Transmit Tip/Ring Output	
TRING1-7	O	Bipolar output over transmit transformer	
TPOS1-7	I	Transmit Positive/Negative Data Input	
TNEG1-7	I	Input on the falling edge of TCLK	
TCLK1-7	I	Transmit Clock Input	
RTIP1-7	I	Receive Tip/Ring Input	
RRING1-7	I	Bipolar Input over receive transformer	
RPOS1-7	O	Receive Positive/Negative Data Output	
RNEG1-7	O	Output on the falling edge of RCLK	
RCLK1-7	O	Receive Clock Output recovered from receive data input	
LOS1-7	O	Loss of signal output Output "high" when detect loss of signal LOSx output is not masked by MLOSx register.	
TVDD1-7		Positive Power Supply for the Transmit Driver	
TVSS1-7		Negative Power Supply for the Transmit Driver	
AVSS1-8		Analog ground .	
<b>Common Block</b>			
MCLK	I	2.048/32.768MHz External Reference Clock Input	
$\overline{AS}$ (ALE)	I	Address Select(Address Latch Enable) Input	
INT	O	Interrupt Output(PMOS open drain, should be tied to GND through a resistor), Active High, INT output goes "high" when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.	
$\overline{DS}$ (RD)	I	Data Strobe(Read Enable) Input	
$\overline{R/W}$ (WR)	I	Read/Write(Write Enable) Input	
$\overline{CS}$	I	Chip Select Input	
BTS	I	Bus Type Select Input BTS="H" : Motorola Mode BTS="L" : Intel Mode	
SCLK	I	Serial Clock Input	
SDI	I	Serial Data Input	
SDO	O	Serial Data Output	
AD0-AD7	I/O	Address/Data Input/Output Used for read/write internal registers.	

Pin Name	I/O	Function	Comment
<b>Common Block</b>			
CLKSEL	I	MCLK Select Input CLKSEL="H":2.048MHz CLKSEL="L":34.768MHz	
$\overline{P/S}$	I	Parallel/Serial Port Select $\overline{P/S}$ ="H": Serial Port is selected $\overline{P/S}$ ="L": Parallel Port is selected	
$\overline{RESET}$	I	Reset Input Active "Low" input pulse over 200ns initializes the internal circuit and forces RPOSx/RNEGx output "low" and LOSx output "high".	
TEST1,2,3,4	I	Factory Use. Should be connected to VSS externally.	
TAVDD1,2		Positive Power Supply for the analog circuitry in the transmitters	
TAVSS1,2		Negative Power Supply for the analog circuitry in the transmitters	
RAVDD1,2		Positive Power Supply for the analog circuitry in the receivers	
RAVSS1,2		Negative Power Supply for the analog circuitry in the receivers	
DVDD1,2		Positive Power Supply for Digital	
DVSS1,2		Negative Power Supply for Digital	
DAVSS1,2		Ground for Digital	
IOVDD1,2		Positive Power Supply for I/O	
IOVSS1,2		Negative Power Supply for I/O	
BVDD		Positive Power Supply for Reference Circuit	
BVSS		Negative Power Supply for Reference Circuit	
PVDD		Positive Power Supply for PLL	
PVSS		Negative Power Supply for PLL	
BGREF		Bandgap Reference Output. 12k $\Omega$ $\pm$ 1% external register should be connected across this pin and VSS.	



<b>ABSOLUTE MAXIMUM RATINGS</b>
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Parameter	Symbol	Min	Typ	Max	Units	Condition
DC Supply	VDD	-0.3		6.5	V	
Input Voltage	VIN1	-0.3		VDD+0.3	V	Apply to except for RTIPx, RRINGx
	VIN2	-3		VDD+0.3	V	Apply to RTIPx, RRINGx
Input Current	IIN			10	mA	
Storage Temperature	Tstg	-55		130	°C	

Note) All voltages with respect to ground.

All negative voltage pins=0V. VDD apply to all positive voltage pins.

<b>RECOMMENDED OPERATING CONDITIONS</b>
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Parameter	Symbol	min	typ	max	Units	Condition
DC Supply	V+	3.135	3.3	3.465	V	3.3V±5%
Ambient Operating Temperature	Ta	-40	25	+85	°C	

Note) All voltages with respect to ground.

All negative voltage pins=0V. VDD apply to all positive voltage pins.

<b>ELECTORICAL CHARACTERISTICS</b>
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### DC CHARACTERISTICS

Parameter	Symbol	min	typ	max	Units	Condition	
Power Consumption(/ch)	75Ω	PD		75	160	mW	Note1
	120Ω			70	147	mW	
Digital High-Level Output Voltage	VOH	0.9VDD			V	IOH=-40μA	
Digital Low-Level Output Voltage	VOL			0.4	V	IOL=500μA	
Digital High-Level Input Voltage	VIH	0.7VDD			V		
Digital Low-Level Input Voltage	VIL			0.3VDD	V		
Input Leak Current	Ii			10	μA		
Output Current	IOH	1.0			mA	INT pin	

Note1: typ: 50% mark, Room temp., VDD 3.3V

max: 100% mark, Temp./VDD in all range

Not include any other load(ex. External pull up register) except lines.

**RECEIVER**

Receiver characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%, VSS, GND=0V, Ta=-40~85°C,

MCLK frequency: 2.048MHz±100ppm, 32.768MHz±100ppm.

Bipolar input frequency:2.048MHz±50ppm(reference input level: 2.37V<sub>op</sub>±10%@75Ωsystem, 3V<sub>op</sub>±10%@120Ωsystem)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input Impedance		5			kΩ	
Sensitivity		-6			dB	Note1
Loss of Signal Threshold	75Ω	0.28	0.4	0.55	V	Note2
	120Ω	0.35	0.5	0.7	V	
Allowable Consecutive Zeros before LOS		170	175	180	bits	
S/X tolerance				12	dB	Note3
Generated Jitter			16		nspp	Note4
Low pulse density immunity		1/16			Mark	
Jitter Tolerance	ITU-T G.823					

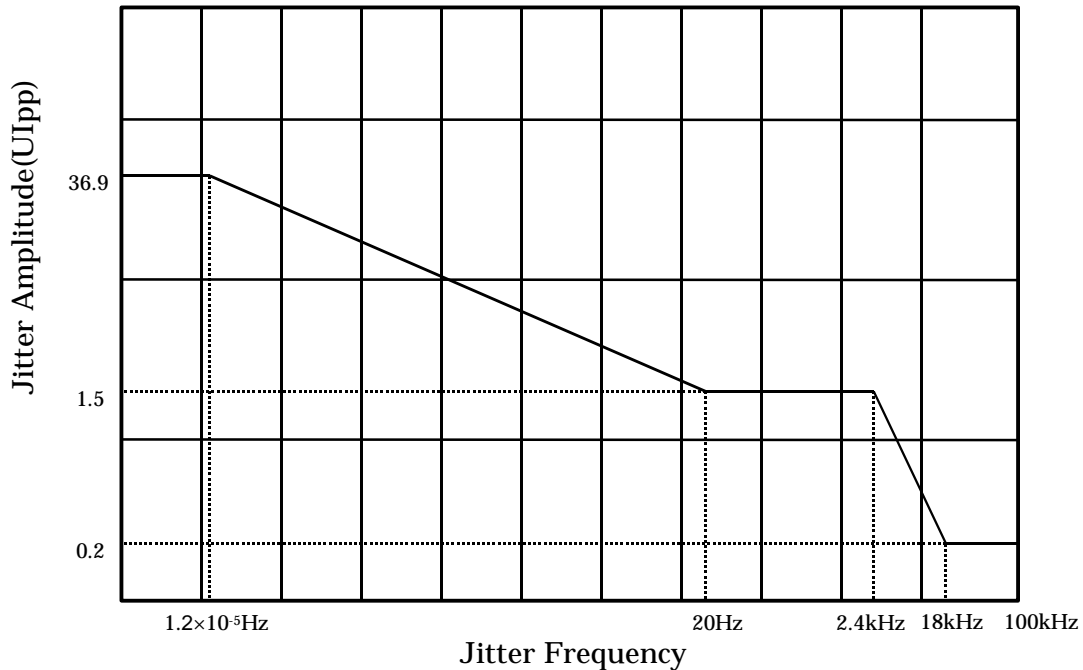
Note1: Relative value to the reference level. Compare at 1.024MHz with All mark pattern.

Note2: Level at the line side of transformer. Loss of signal is logical OR between an analog loss of signal monitors input level and a digital loss of signal check recovered data stream.

Note3: PN15 and AMI 1/4 Mark pattern input. Noise frequency is 1MHz.

Note4: PN15 pattern input.

**Jitter Tolerance(G.823)**



**TRANSMITTER**

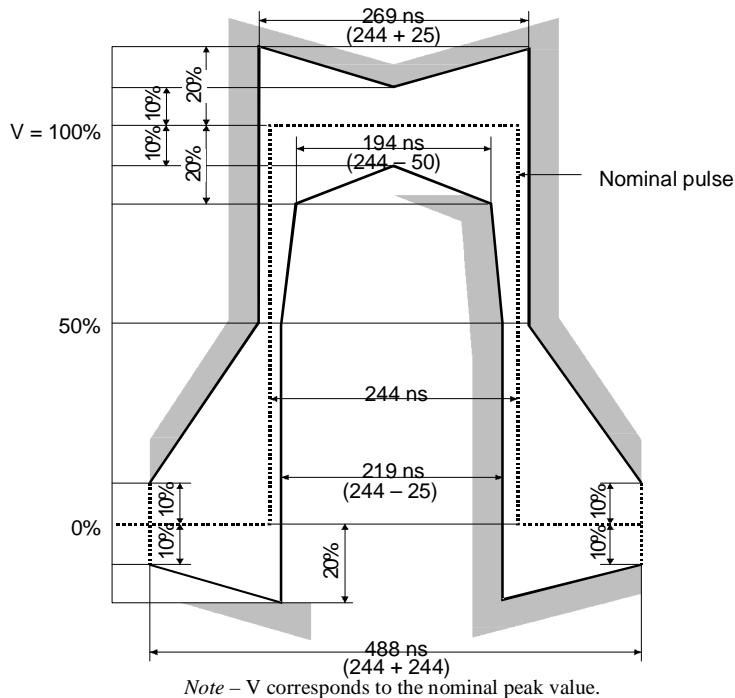
Transmitter characteristics are guaranteed on the conditions as shown below.

VDD=3.3V±5%, VSS, GND=0V, Ta=-40~85°C, MCLK frequency: 2.048MHz±100ppm, 32.768MHz±100ppm

Parameter	Symbol	Min	Typ	Max	Units	Condition
Output Pulse Shape						G.703
Output Pulse Amplitude	75Ω	2.14	2.37	2.60	V <sub>0p</sub>	Note 1
	120Ω	2.7	3.0	3.3	V <sub>0p</sub>	
Pulse Amplitude for a space	75Ω	-0.237		0.237	V <sub>0p</sub>	Note 1
	120Ω	-0.3		0.3	V <sub>0p</sub>	
Output Pulse Imbalance	amplitudes widths	-4		4	%	
		-4		4	%	
Output Jitter	20Hz-100kHz			0.05	UI <sub>pp</sub>	
Return Loss						
51kHz-102kHz		9			dB	
102kHz-2.048MHz		15			dB	
2.048MHz-3.072MHz		11			dB	

Note1: Turns Ratio, DCR and external resistors are recommended value. (P27)

**Pulse Mask Template (G.703)**



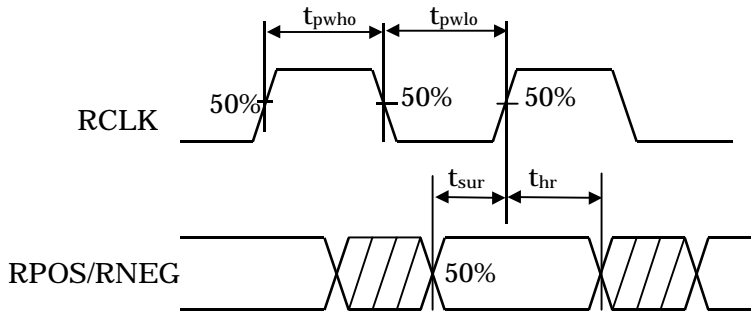
**Mask of the pulse at the 2048 kbit/s interface**

**AC CHARACTERISTICS(Clock/Data)**

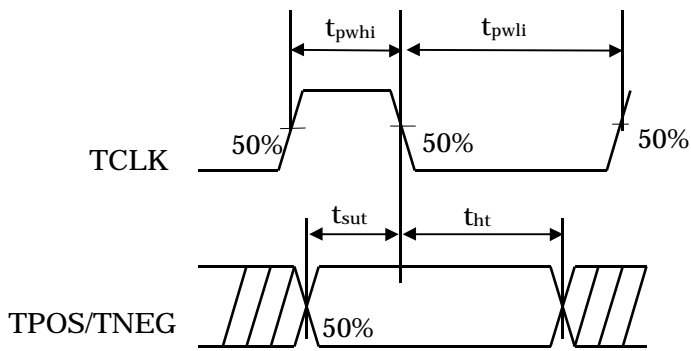
Parameter		Symbol	Min	Typ	Max	Units	Condition
Clock Frequency	MCLK	fci	2.047795	2.048000	2.048204	MHz	±100ppm
			32.76472	32.76800	32.77127	MHz	
Clock Pulse Width	TCLK	t <sub>pwhi</sub>		244		ns	Refer to Fig.2
		t <sub>pqli</sub>					
Clock Pulse Width	RCLK	t <sub>pwho</sub>		244		ns	Refer to Fig.1
		t <sub>pwho</sub>					
Duty Cycle	RCLK TCLK			50		%	Note1
Setup/Hold Time	RCLK	t <sub>su1</sub>	150			ns	Refer to Fig.1
	RPOS	t <sub>h1</sub>					
	RNEG						
Setup/Hold Time	TCLK	t <sub>su2</sub>	50			ns	Refer to Fig.2
	TPOS	t <sub>h2</sub>					
	TNEG						
Rise Time	RCLK	t <sub>r</sub>			100	ns	Refer to Fig.3 Note2
	RPOS						
	RNEG						
Fall Time	TCLK	t <sub>r</sub>			40	ns	Refer to Fig.3 Note2
	TPOS						
	TNEG						

Note1) Duty Cycle:  $(t_{pwho} / (t_{pwho} + t_{pqli})) \times 100\%$

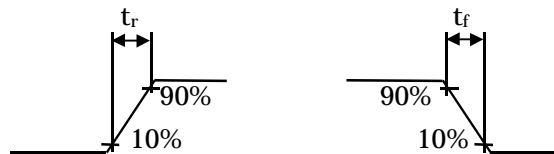
Note2) Drive 15pF Load Capacitance



**Figure 1. Receiver Timing**



**Figure 2. Transmitter Timing**



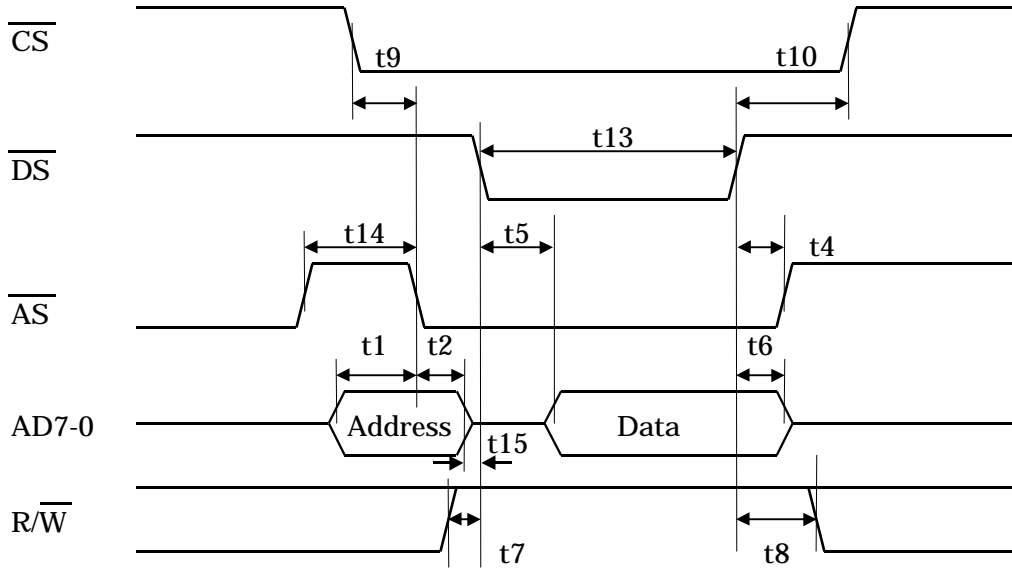
**Figure 3. Rise and Fall Times  
(RCLK,RPOS,RNEG,TCLK,TPOS,TNEG)**

**AC CHARACTERISTICS(Parallel Port)**

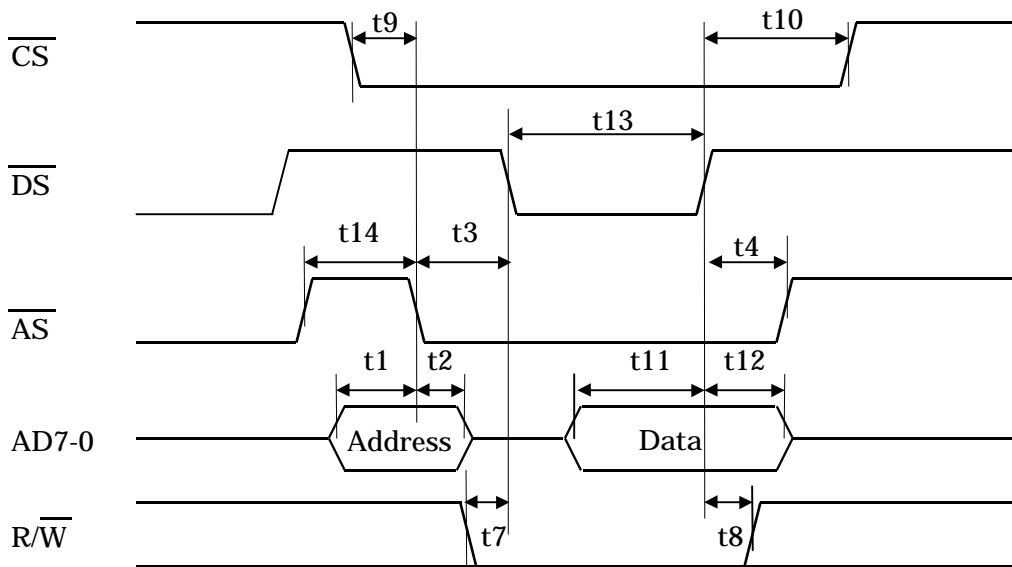
Parameter	Symbol	Min	Typ	Max	Units	Condition
Read/Write Cycle	tcyc	250			ns	
<b>Motorola Mode</b>						
Address Setup Time	t1	10	—	—	ns	
Address Hold Time	t2	10	—	—	ns	
$\overline{AS}$ to $\overline{DS}$ Delay Time	t3	20	—	—	ns	
$\overline{DS}$ to $\overline{AS}$ Delay Time	t4	20	—	—	ns	
Read Data Delay Time	t5	—	—	40	ns	
Read Data Hold Time	t6	—	—	20	ns	
R/W Setup Time	t7	10	—	—	ns	
R/W Hold Time	t8	10	—	—	ns	
$\overline{CS}$ Setup Time	t9	10	—	—	ns	
$\overline{CS}$ Hold Time	t10	15	—	—	ns	
$\overline{DS}$ to Write Data Setup Time	t11	40	—	—	ns	
$\overline{DS}$ to Write Data Hold Time	t12	20	—	—	ns	
$\overline{DS}$ Pulse Width	t13	100	—	—	ns	
$\overline{AS}$ Pulse Width	t14	20	—	—	ns	
Address Invalid to $\overline{DS}$ Delay Time	t15	0	—	—	ns	
<b>Intel Mode</b>						
Address Setup Time	t21	10	—	—	ns	
Address Hold Time	t22	10	—	—	ns	
ALE to $\overline{WR}$ Delay Time	t23	20	—	—	ns	
$\overline{WR}$ to ALE Delay Time	t24	20	—	—	ns	
$\overline{RD}$ to ALE Delay Time	t25	20	—	—	ns	
Read Data Delay Time	t26	—	—	40	ns	
Read Data Hold Time	t27	—	—	20	ns	
$\overline{CS}$ Setup Time	t28	10	—	—	ns	
$\overline{CS}$ Hold Time	t29	15	—	—	ns	
$\overline{DS}$ to Write Data Setup Time	t30	40	—	—	ns	
$\overline{DS}$ to Write Data Hold Time	t31	20	—	—	ns	
$\overline{RD}$ Pulse Width	t32	100	—	—	ns	
$\overline{WR}$ Pulse Width	t33	100	—	—	ns	
ALE Pulse Width	t34	20	—	—	ns	
Address Invalid to $\overline{RD}$ Delay Time	t35	0	—	—	ns	

Notes) CL= 50pF on AD0-AD7. All of the timing is specified at 50%VDD.

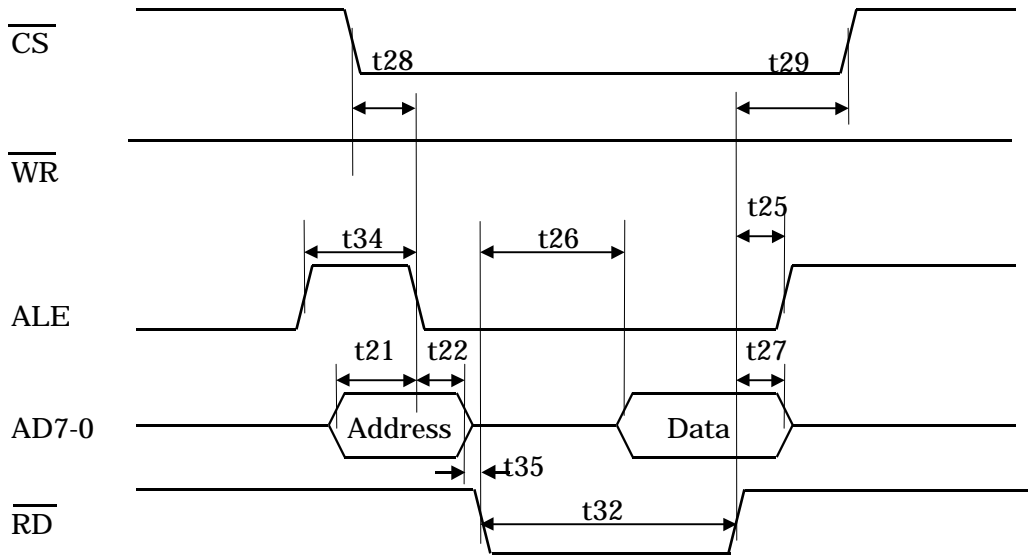
**Motorola Mode(READ)**



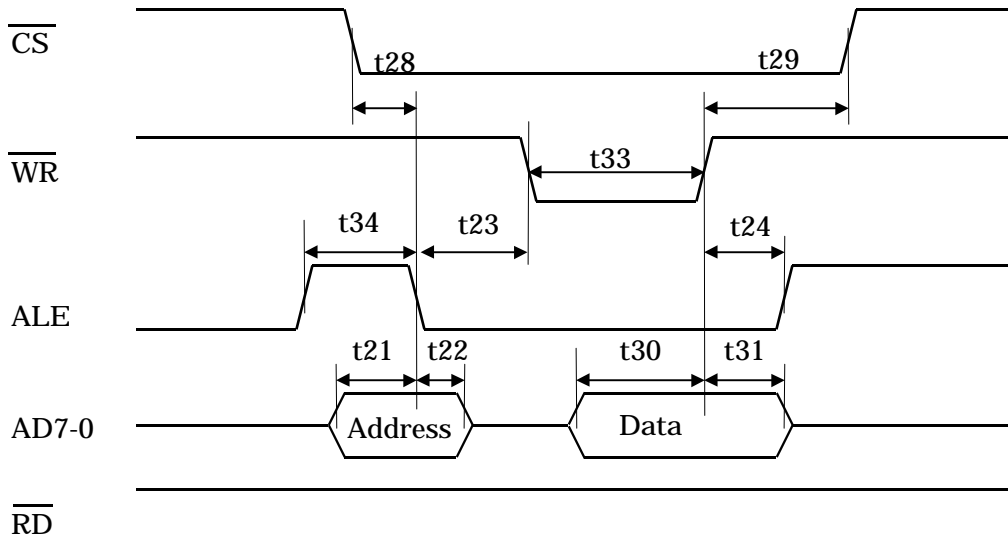
**Motorola Mode(WRITE)**



**Intel Mode(READ)**



**Intel Mode(WRITE)**



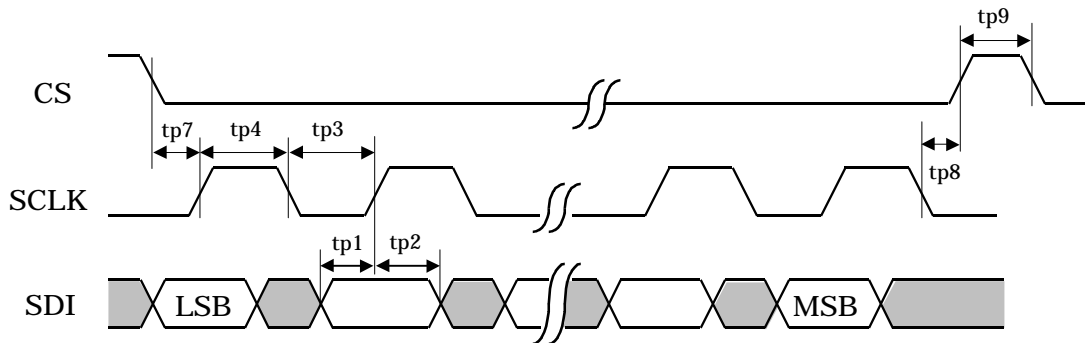


**AC CHARACTERISTICS(Serial Port)**

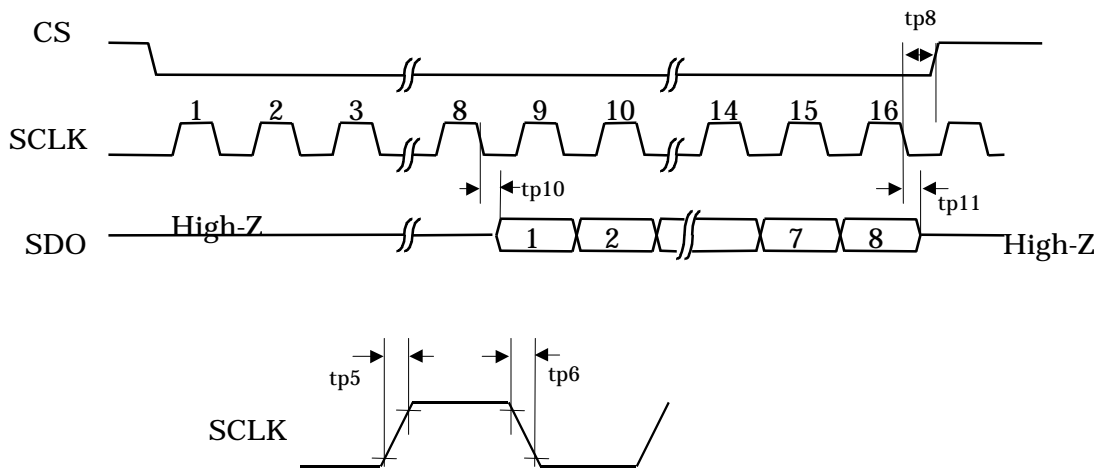
Parameter	Symbol	min	typ	max	Units	Condition
SDI Setup Time	tp1	25	—	—	ns	
SDI Hold Time	tp2	25	—	—	ns	
SCLK Low Time	tp3	100	—	—	ns	
SCLK High Time	tp4	100	—	—	ns	
SCLK Rise Time	tp5	—	—	15	ns	
SCLK Fall Time	tp6	—	—	15	ns	
CS Setup Time	tp7	20	—	—	ns	
CS Hold Time	tp8	20	—	—	ns	
CS Inactive Time	tp9	100	—	—	ns	
SCLK to SDO Valid	tp10	—	—	40	ns	
CS to SDO High Z	tp11	—	—	40	Ns	

Notes) CL= 50pF. All of the timing is specified at 50%VDD.

**Serial Port Input Timing**



**Serial Port Output Timing**



**REGISTER DESCRIPTION**

**REGISTER MAP**

\*A7-A4="0"

Address				Function								
A3	A2	A1	A0	Bit7 <AD7>	Bit6 <AD6>	Bit5 <AD5>	Bit4 <AD4>	Bit3 <AD3>	Bit2 <AD2>	Bit1 <AD1>	Bit0 <AD0>	
<b>Status Register (READ ONLY)</b>												
0	0	0	0	LOS7 (1)	LOS6 (1)	LOS5 (1)	LOS4 (1)	LOS3 (1)	LOS2 (1)	LOS1 (1)	0	
0	0	0	1	LOTC7 (1)	LOTC6 (1)	LOTC5 (1)	LOTC4 (1)	LOTC3 (1)	LOTC2 (1)	LOTC1 (1)	LOMC (1)	
<b>Mask Control Register (WRITE/READ)</b>												
0	0	1	0	MLOS7 (1)	MLOS6 (1)	MLOS5 (1)	MLOS4 (1)	MLOS3 (1)	MLOS2 (1)	MLOS1 (1)	RDEN (0)	
0	0	1	1	MLOTC7 (1)	MLOTC6 (1)	MLOTC5 (1)	MLOTC4 (1)	MLOTC3 (1)	MLOTC2 (1)	MLOTC1 (1)	MLOMC (1)	
<b>Channel Control Register (WRITE/READ)</b>												
0	1	1	0	Reserved	TAOS1 (0)	EC1 (0)	RLOOP1 (0)	LLOOP1 (0)	POLN1 (1)	MSK1 (1)	PD1 (1)	
0	1	1	1	Reserved	TAOS2 (0)	EC2 (0)	RLOOP2 (0)	LLOOP2 (0)	POLN2 (1)	MSK2 (1)	PD2 (1)	
1	0	0	0	Reserved	TAOS3 (0)	EC3 (0)	RLOOP3 (0)	LLOOP3 (0)	POLN3 (1)	MSK3 (1)	PD3 (1)	
1	0	0	1	Reserved	TAOS4 (0)	EC4 (0)	RLOOP4 (0)	LLOOP4 (0)	POLN4 (1)	MSK4 (1)	PD4 (1)	
1	0	1	0	Reserved	TAOS5 (0)	EC5 (0)	RLOOP5 (0)	LLOOP5 (0)	POLN5 (1)	MSK5 (1)	PD5 (1)	
1	0	1	1	Reserved	TAOS6 (0)	EC6 (0)	RLOOP6 (0)	LLOOP6 (0)	POLN6 (1)	MSK6 (1)	PD6 (1)	
1	1	0	0	Reserved	TAOS7 (0)	EC7 (0)	RLOOP7 (0)	LLOOP7 (0)	POLN7 (1)	MSK7 (1)	PD7 (1)	

\*Other address is reserved.

\* Initial value is in ( ).

\* "<>" show I/O pin name. Address A0-A3 should be input via AD0-AD3 pins.

**STATUS REGISTER**

Symbol	Description
LOS <sub>x</sub> (x=1 to 7)	Loss of signal alarm for channel x. Read only register. When the loss of signal or the loss of MCLK are detected, LOS <sub>x</sub> goes High.
LOT <sub>Cx</sub> (x=1 to 7)	Loss of TCLK alarm for channel x. Read only register. When the loss of TCLK <sub>x</sub> is detected, LOT <sub>Cx</sub> goes High.
LOMC	Loss of MCLK alarm. Read only register. When the loss of MCLK is detected, LOMC and LOS <sub>x</sub> go High.

**MASK CONTROL REGISTER**

Symbol	Description
MLOS <sub>x</sub> (x=1 to 7)	Mask loss of signal alarm for channel x. MLOS <sub>x</sub> is active-high to prevent LOS <sub>x</sub> from setting INT output "high". It is possible to read LOS <sub>x</sub> register regardless of the status of MLOS <sub>x</sub> . Initial value is "high".
MLOT <sub>Cx</sub> (x=1 to 7)	Mask loss of TCLK alarm for channel x. MLOT <sub>Cx</sub> is active-high to prevent LOT <sub>Cx</sub> from setting INT output "high". It is possible to read LOT <sub>Cx</sub> register regardless of the status of MLOT <sub>Cx</sub> . Initial value is "high".
MLOMC	Mask loss of MCLK alarm. MLOMC is active-high to prevent LOMC from setting INT output "high". It is possible to read LOMC register regardless of the status of MLOMC. Initial value is "high". Note) Please refer to "Loss of MCLK theory of operation". (P25)

**CHANNEL CONTROL REGISTER**

Symbol	Description
RLOOP <sub>x</sub> / LLOOP <sub>x</sub>	Loopback mode of channel x is activated through the setting of these register as shown below in Table 1.
POLN <sub>x</sub>	TIP <sub>x</sub> /RING <sub>x</sub> output polarity is controlled by this register as shown below in Table 2. Initial value is "high".
PD <sub>x</sub>	PD <sub>x</sub> is active-high to set the corresponding transceiver in power down mode. TTIP <sub>x</sub> and TRING <sub>x</sub> go "low". LOS <sub>x</sub> goes "high" in power down mode. Initial value is "high".
MSK <sub>x</sub>	MSK <sub>x</sub> is active-high to prevent LOS <sub>x</sub> or LOT <sub>Cx</sub> from setting INT output "high". Initial value is "high".
RDEN	RDEN is active-high to prevent RCLK, RPOS, and RNEG output from forcing to "low" or "high" by the detection of Loss of signal. Initial value is "low".
TAOS <sub>x</sub>	TAOS is active-high to output all one's signal from TTIP <sub>x</sub> and TRING <sub>x</sub> . All one's signal synchronized with TCLK. When TCLK is lost, the signal synchronized with MCLK.
EC <sub>x</sub>	Application is selected by this register in Table 3. Initial value is low.

**Table 1. Loopback mode Select**

RLOOPx	LLOOPx	Function
0	0	Normal (Initial value)
0	1	Local Loop back
1	0	Remote Loop back
1	1	Inhibited

**Table 2. TIPx/RINGx Polarity Control**

POLNx	POSx/NEGx	TIPx/RINGx
1	0	space
	1	mark
0	0	mark
	1	space

**Table 3 Equalizer Control**

ECx	Application
0	E1-Coax(75Ω) (Initial value)
1	E1-Twisted Pair(120Ω)

**OUTPUT CONTROL**

\* : don't care

LOS: LOSx output and LOSx register

**Reset, Loss of MCLK, Power down**

RESET	MCLK	PD	TAOS	Loopback		POLN	RDEN	TCLK	Receive Signal	TTIP TRING	RCLK	RPOS RNEG	LOS
				Local	Remote								
0	*	*	*	*	*	*	*	*	*	0	0	0	1
1	loss	*	*	*	*	1	*	*	*	0	0	0	1
1	loss	*	*	*	*	0	*	*	*	0	0	1	1
1	clocked	1	*	*	*	1	*	*	*	0	0	0	1
1	clocked	1	*	*	*	0	*	*	*	0	0	1	1

**Normal Operation(RESET=1, MCLK:clocked, PD=0)**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
	Local	Remote								
0	0	0	1	*	Clocked	in	TPOS TNEG	RCLK	RTIP RRING	0
0	0	0	1	0	Clocked	loss	TPOS TNEG	0	0	1
0	0	0	1	*	Loss	in	0	RCLK	RTIP RRING	0
0	0	0	1	0	Loss	loss	0	0	0	1
0	0	0	1	1	Clocked	loss	TPOS TNEG	RCLK	RTIP RRING	1
0	0	0	1	1	Loss	loss	0	RCLK	RTIP RRING	1
0	0	0	0	*	Clocked	in	TPOS TNEG	RCLK	RTIP RRING	0
0	0	0	0	0	Clocked	loss	TPOS TNEG	0	1	1
0	0	0	0	*	Loss	in	0	ORCLK	RTIP RRING	0
0	0	0	0	0	Loss	loss	0	0	1	1
0	0	0	0	1	clocked	loss	TPOS TNEG	RCLK	RTIP RRING	1
0	0	0	0	1	loss	loss	0	RCLK	RTIP RRING	1

**Normal Operation( $\overline{\text{RESET}}=1$ , MCLK:clocked, PD=0)**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
	Local	Remote								
1	0	0	1	*	clocked	in	All Mark	RCLK	RTIP RRING	0
1	0	0	1	0	clocked	loss	All Mark	0	0	1
1	0	0	1	*	loss	in	All Mark	RCLK	RTIP RRING	0
1	0	0	1	0	loss	loss	All Mark	0	0	1
1	0	0	1	1	clocked	loss	All Mark	RCLK	RTIP RRING	1
1	0	0	1	1	loss	loss	All Mark	RCLK	RTIP RRING	1
1	0	0	0	*	clocked	in	All Mark	RCLK	RTIP RRING	0
1	0	0	0	0	clocked	loss	All Mark	0	1	1
1	0	0	0	*	loss	in	All Mark	RCLK	RTIP RRING	0
1	0	0	0	0	loss	loss	All Mark	0	1	1
1	0	0	0	1	clocked	loss	All Mark	RCLK	RTIP RRING	1
1	0	0	0	1	loss	loss	All Mark	RCLK	RTIP RRING	1

**Remote Loopback(RESET=1, MCLK:clocked, PD=0)**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
	Local	Remote								
0	0	1	1	*	*	in	RTIP RRING	RCLK	RTIP RRING	0
0	0	1	1	0	*	loss	RTIP RRING	0	0	1
0	0	1	1	1	*	loss	RTIP RRING	RCLK	RTIP RRING	1
0	0	1	0	*	*	in	RTIP RRING	RCLK	RTIP RRING	0
0	0	1	0	0	*	loss	RTIP RRING	0	1	1
0	0	1	0	1	*	loss	RTIP RRING	RCLK	RTIP RRING	1

**Remote Loopback(RESET=1, MCLK:clocked, PD=0)**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS RNEG	LOS
	Local	Remote								
1	0	1	1	*	*	in	All Mark	RCLK	RTIP RRING	0
1	0	1	1	0	*	loss	All Mark	0	0	1
1	0	1	1	1	*	loss	All Mark	RCLK	RTIP RRING	1
1	0	1	0	*	*	in	All Mark	RCLK	RTIP RRING	0
1	0	1	0	0	*	loss	All Mark	0	1	1
1	0	1	0	1	*	loss	All Mark	RCLK	RTIP RRING	1

**Local Loopback( $\overline{\text{RESET}}=1, \text{MCLK:clocked}, \text{PD}=0$ )**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS	LOS
	Local	Remote							RNEG	
0	1	0	1	*	clocked	in	TPOS TNEG	TCLK (Note)	TPOS TNEG	0
0	1	0	1	*	clocked	loss	TPOS TNEG	TCLK (Note)	TPOS TNEG	1
0	1	0	1	*	loss	in	0	0	0	0
0	1	0	1	*	loss	loss	0	0	0	1
0	1	0	0	*	clocked	in	TPOS TNEG	TCLK (Note)	TPOS TNEG	0
0	1	0	0	*	clocked	loss	TPOS TNEG	TCLK (Note)	TPOS TNEG	1
0	1	0	0	*	loss	in	0	0	1	0
0	1	0	0	*	loss	loss	0	0	1	1

Note) The phase satisfy receive output timing.

**Local Loopback( $\overline{\text{RESET}}=1, \text{MCLK:clocked}, \text{PD}=0$ )**

TAOS	Loopback		POLN	RDEN	TCLK	Receive signal	TTIP TRING	RCLK	RPOS	LOS
	Local	Remote							RNEG	
1	1	0	1	*	clocked	in	All Mark	TCLK (Note)	TPOS TNEG	0
1	1	0	1	*	clocked	loss	All Mark	TCLK (Note)	TPOS TNEG	1
1	1	0	1	*	loss	in	All Mark	0	0	0
1	1	0	1	*	loss	loss	All Mark	0	0	1
1	1	0	0	*	clocked	in	All Mark	TCLK (Note)	TPOS TNEG	0
1	1	0	0	*	clocked	loss	All Mark	TCLK (Note)	TPOS TNEG	1
1	1	0	0	*	loss	in	All Mark	0	1	0
1	1	0	0	*	loss	loss	All Mark	0	1	1

Note) The phase satisfy receive output timing.



<b>THEORY OF OPERATION</b>
----------------------------

**Loss of signal**

Loss of signal in channel x is reported by setting LOSx register “high”.

The receiver will indicate loss of signal upon receiving 175 consecutive zeros or detecting input level being below the threshold(ALOS).

LOSx returns to “low” when the received signal returns to 12.5% ones density and not include 100 consecutive zeros.

When Loss of Signal is detected in channel x, LOSx register is set “high” and LOSx pin becomes “high”. When LOSx is set “high”, interrupt will be issued on INT pin if MLOSx is “low”. LOSx pin becomes high regardless of MLOSx status. MLOSx is active-high and masks LOSx interrupt. LOSx register represents the current status of received signal regardless of the status of the MLOSx status.

**Loss of TCLK**

Loss of TCLKx is reported by setting LOTCx “high”. When LOTCx is set “high”, INT output becomes “high” if MLOTCx is “low”. Even if TCLK return to normal quickly, LOTCx remain “high” for 126us. MLOTCx is active-high and masks LOTCx interrupt. LOTCx represents the current status of TCLKx and can be read regardless of the status of the MLOTCx status.

When Loss of TCLKx is detected, TTIPx/TRINGx will be forced to “0”.

**Loss of MCLK**

Loss of MCLK is reported by setting LOMC “high”. When LOMC goes “high”, INT output becomes “high” if MLOMC is “low”. Even if MCLK return to normal quickly, LOMC remain “high” for 126us. MLOMC is active-high and masks LOMC interrupt. LOMC represents the current status of MCLK and can be read regardless of MLOMC status. When the loss of MCLK is detected, LOSx register and LOSx pin goes “high” at the same time. Therefore all MLOSx register must be set to “high” to prevent loss of MCLK from setting INT output.

**INT output**

INT output goes “high” when the alarm is reported to any one of LOSx, LOTCx or LOMC registers. This pin can be masked by MLOSx, MLOTCx or MLOMC registers.

**Local Loopback**

In Local Loopback mode, TPOSx,TNEGx,TCLKx signals are looped back to RPOSx, RNEGx, RCLKx output. RTIPx,RRINGx inputs are ignored but loss of signal detection is active. The transmitter in channel x outputs TTIPx,TRINGx normally.

**Remote Loopback**

In Remote Loopback mode, RTIPx/RRINGx signals are looped back to TTIPx/TRINGx output. The receiver in channel x output RPOSx,RNEGx,RCLKx normally and detect loss of signal. TPOSx,TNEGx,TCLKx inputs are ignored. When TAOSx is “high”, all mark signal is output to TTIPx/TRINGx.

**Interface**

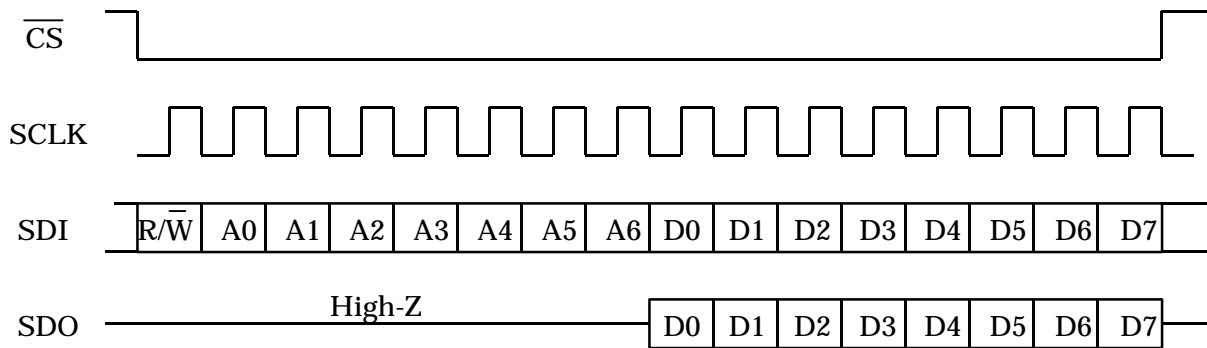
Interface to control/status register is selected by  $\overline{P/S}$  pin. When  $\overline{P/S}$  is set to “low”, parallel interface is selected. When  $\overline{P/S}$  is set to “high”, serial interface is selected.

**Parallel Interface**

Bus type(Intel/Motorola) is selected by BTS pin. When BTS is set to “high”, Motorola mode is selected. When BTS is set to “low”, Intel mode is selected.

**Serial Interface**

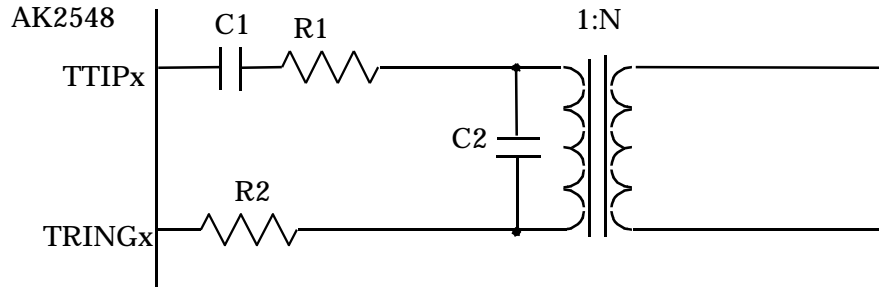
The timing of serial interface is shown below.



$\overline{R/W}=1$ : read  
 $\overline{R/W}=0$ : write

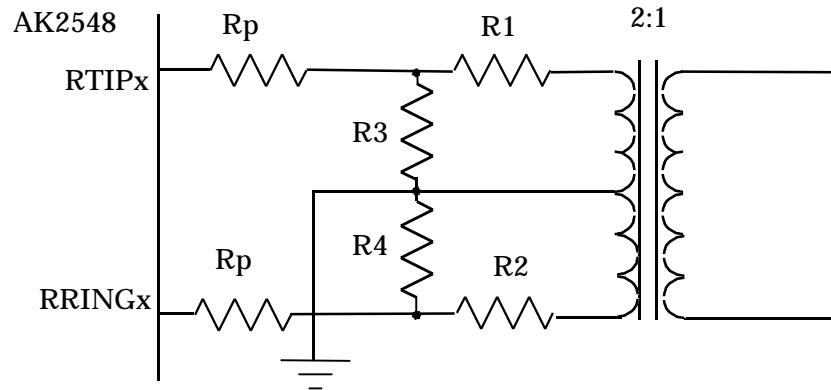
**RECOMMENDED EXTERNAL CIRCUIT**

**Transmit Circuit**



	75Ω	120Ω
Trans Rate	1:2	1:2.2
R1,R2	8.2Ω±1%	9.1Ω±1%
C1	1uF	1uF
C2	470pF	470pF

**Received Circuit**



	75Ω	120Ω
R1,R2	20Ω	82Ω
R3,R4	130Ω	160Ω
Rp	100Ω	

\*Rp is protection resistance against surge.

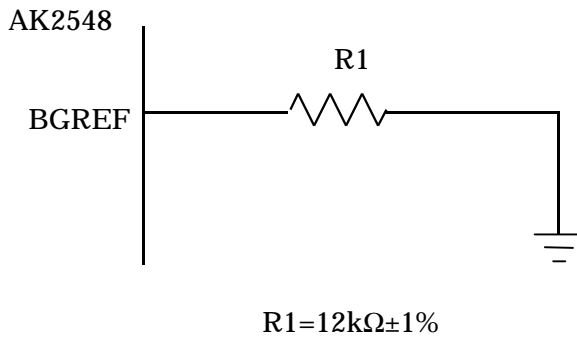
Rp is used for surge current limiting. (ITU-T K.41)

**Recommended Transformer Specification**

	Turns Ratio (Typ)	Primary Inductance (Min)	Leakage Inductance (Max)	Interwinding Capacitance (Max)	DCR (Max)		
					pri	sec	
Tx	75Ω	1:2	720uH	0.3uH	30pF	0.6Ω	1.2Ω
	120Ω	1:2.2	720uH	0.3uH	30pF	0.6Ω	1.3Ω
Rx		1:2	1.2mH	0.3uH	30pF	0.6Ω	1.2Ω

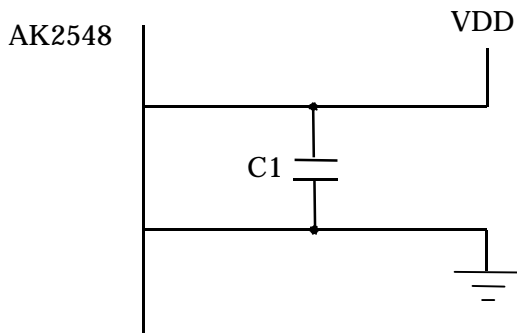
**Reference current circuit**

To determine input reference current, connect  $12\text{k}\Omega \pm 1\%$  resistor.



**Power Supply**

To attenuate the power supply noise, connect capacitors between VDD and VSS respectively. The value of the capacitance AK2548 need depend on the condition of the power supply line. Please decide the value of the capacitance after your evaluation.

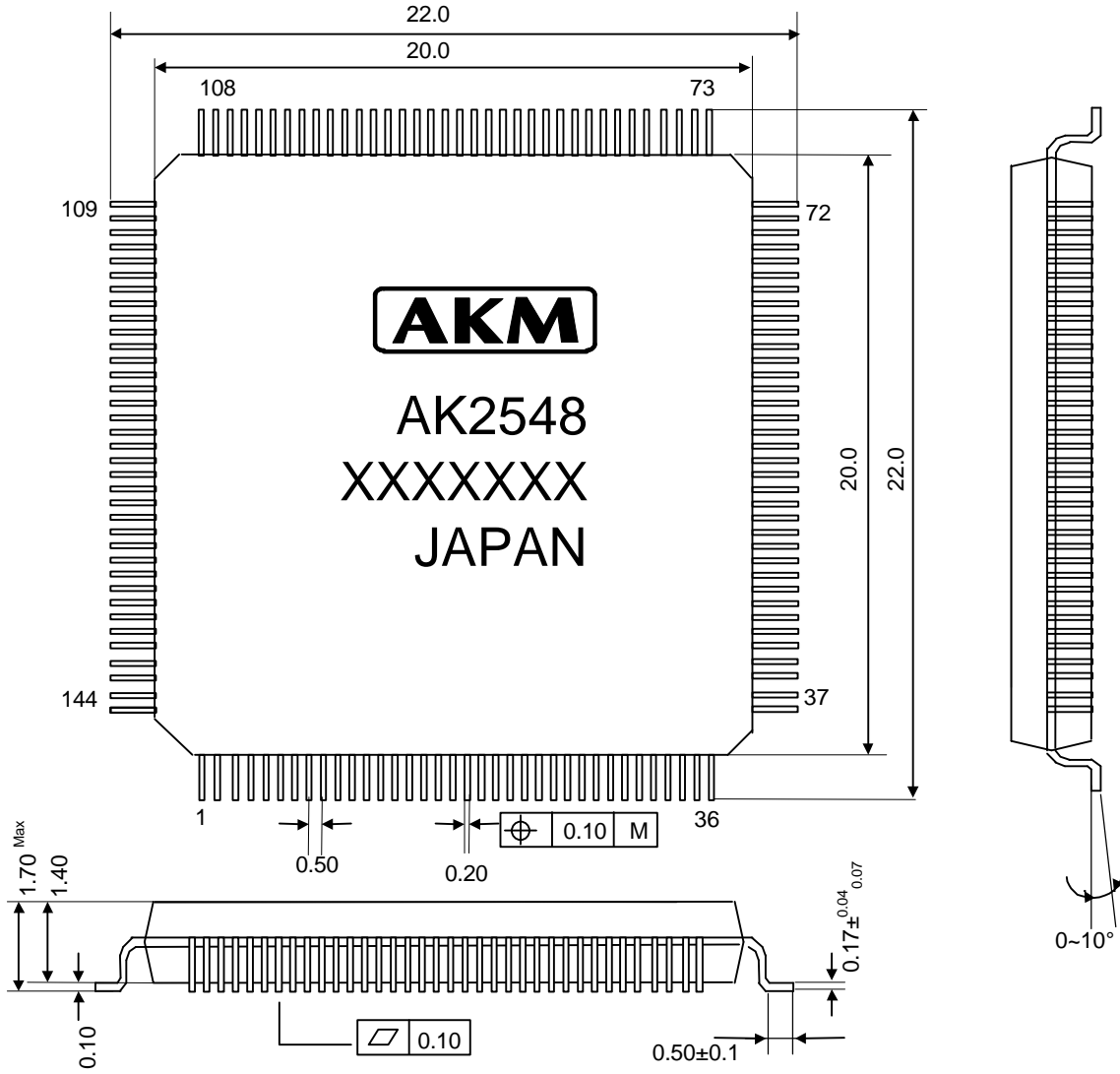


Pin name	C1
RAVDD1-RAVSS1, RAVDD2-RAVSS2, BVDD-BVSS, TAVDD1-TAVSS1, TAVDD2-TAVSS2	1uF
TVDD1-TVSS1, TVDD2-TVSS2, TVDD3-TVSS3, TVDD4-TVSS4, TVDD5-TVSS5, TVDD6-TVSS6, TVDD7-TVSS7, IOVDD1-IOVSS1, IOVDD2-IOVSS2, DVDD1-DVSS1, DVDD2-DVSS2, PVDD-PVSS	0.01uF

PACKAGE

144pin LQFP

OUTPUT DIMENSIONS



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  - (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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