TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

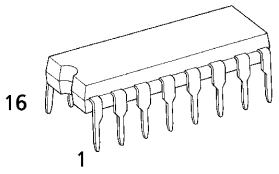
TC74HC191AP, TC74HC191AF

4 – BIT BINARY UP/DOWN COUNTER

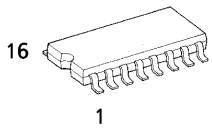
The TC74HC191A are high speed CMOS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC191A is 4 - bit binary up/down counter.
They have a asynchronous load input (LOAD) which is active low.
The direction of counting is determined by the level of DOWN/UP. When D/U is low , the counter counts up ; when D/U is high , it counts down.Counting occurs on the positive going transition of the clock input.
Enable input (ENABLE) and two carry inputs (RIPPLE CLOCK OUT, MAX/MIN) are provided to permit easy cascading of the counters, which facilitates easy implementation of N - bit counters without using external gates.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed····· f_{MAX} = 48MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output drive Capability····· 10 LSTTL Loads
- Symmetrical Output Impedance··· $|I_{OH}| = I_{OL}$ = 4mA (Min.)
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS191

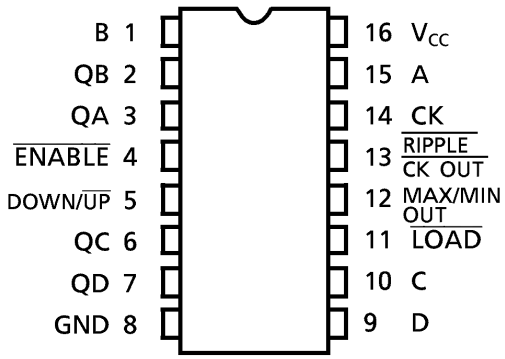


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



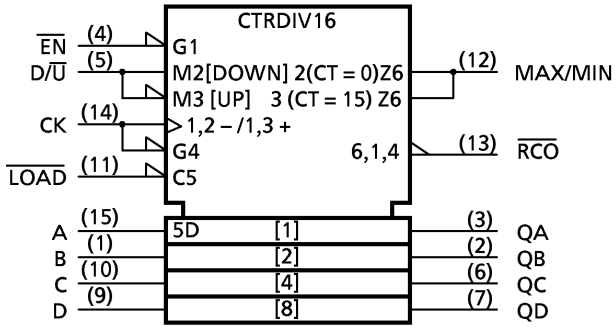
F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

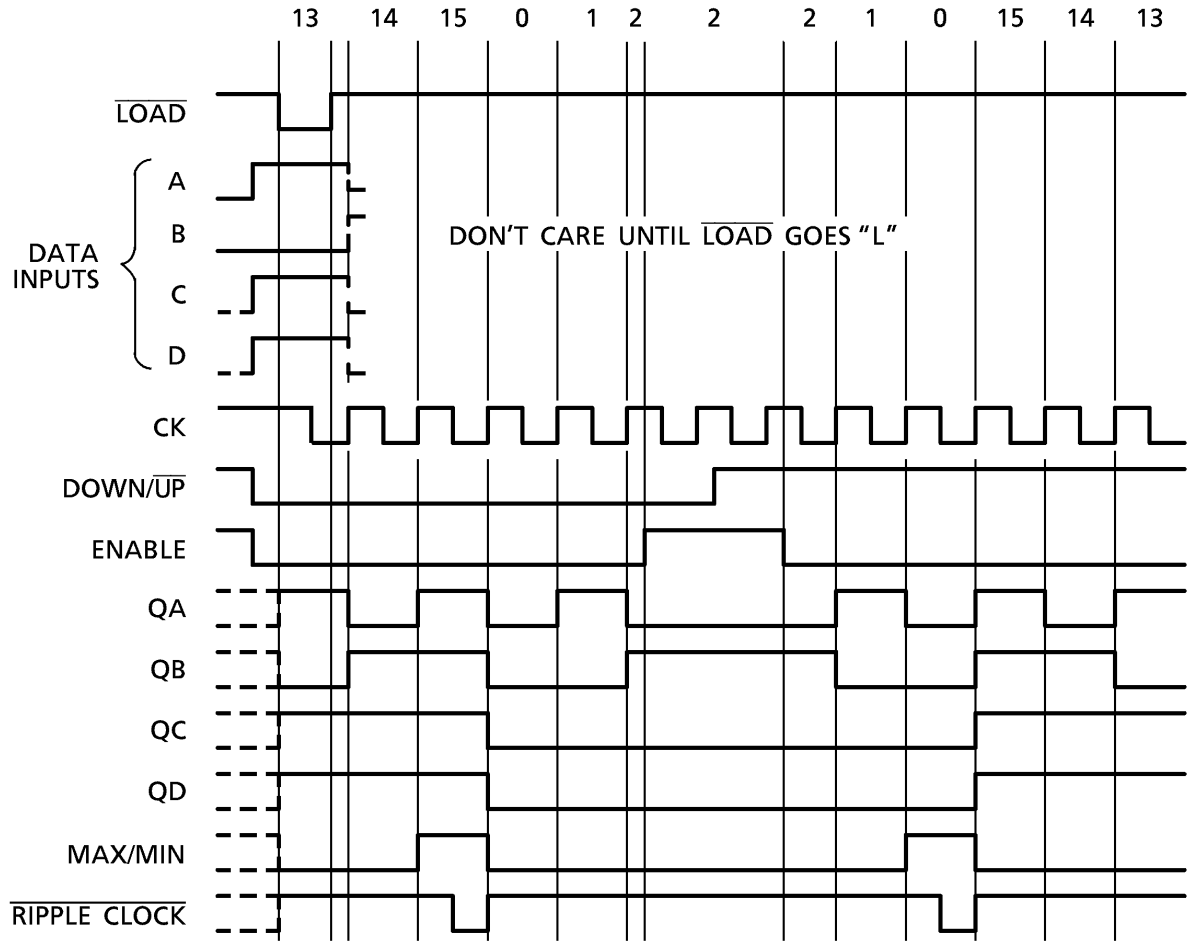


TRUTH TABLE

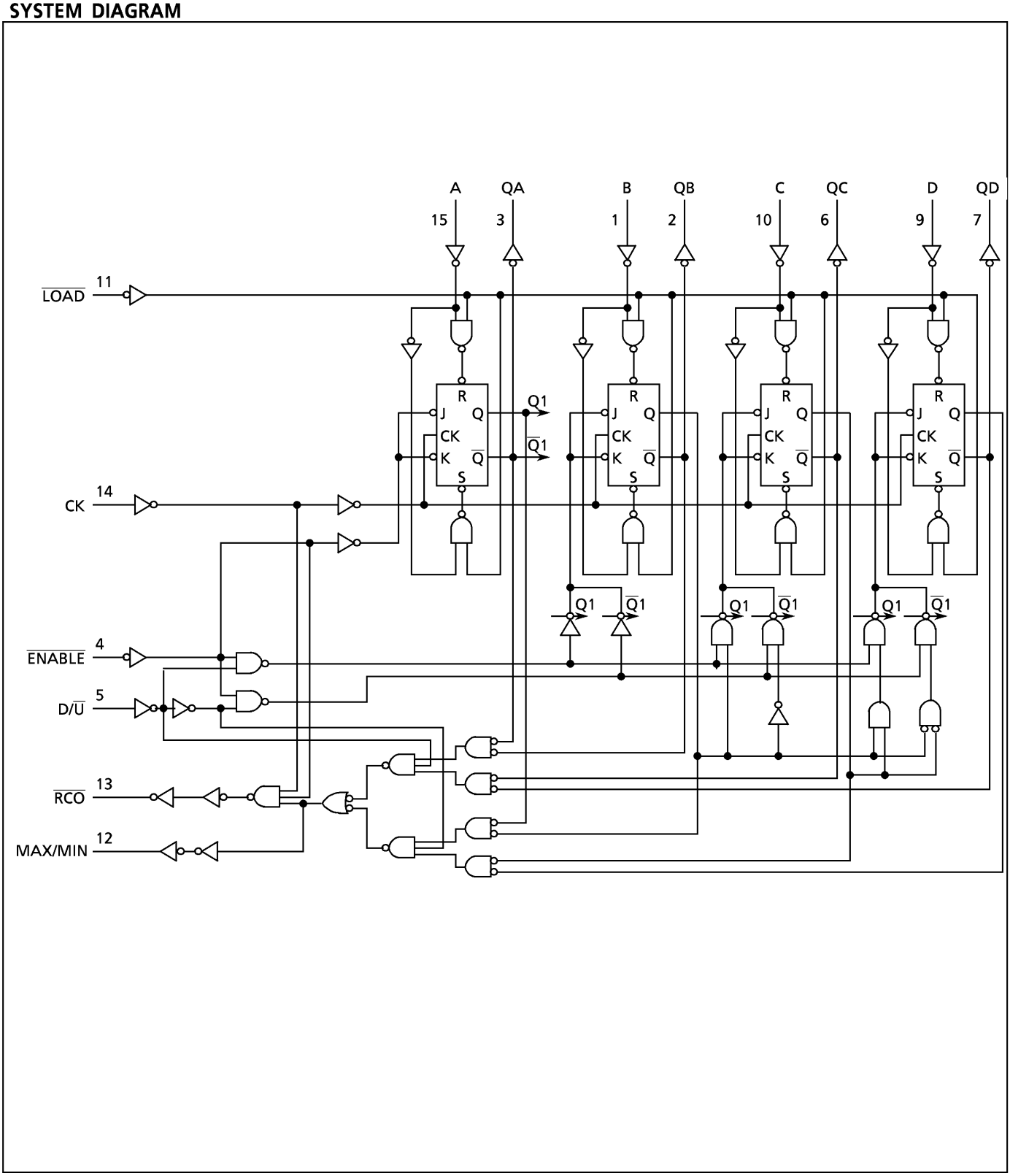
INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	↑	UP COUNT				UP COUNT
H	L	H	↑	DOWN COUNT				DOWN COUNT
H	H	X	↑	NO CHANGE				NO COUNT
H	X	X	↓	NO CHANGE				NO COUNT

NOTE X : DON'T CARE
a ~ d : Inputs Level of A ~ D

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_s		2.0	—	150	190	
			4.5	—	30	38	
			6.0	—	26	33	
Minimum Set−up Time (DATE−$\overline{LOAD}$)	t_s		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Minimum Hold Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (DATE−$\overline{LOAD}$)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time	t_{rem}		2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	5	4	MHz
			4.5	—	25	20	
			6.0	—	29	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		—	18	31	
Propagation Delay Time (CK−$\overline{RCO}$)	t_{pLH} t_{pHL}		—	10	20	
Propagation Delay Time (CK−MAX/MIN)	t_{pLH} t_{pHL}		—	23	42	
Propagation Delay Time ($\overline{LOAD}$−Q)	t_{pLH} t_{pHL}		—	21	35	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		—	17	30	
Propagation Delay Time ($\overline{ENABLE}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		—	11	17	
Propagation Delay Time (D/$\overline{U}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		—	17	31	
Propagation Delay Time (D/$\overline{U}$−MAX/MIN)	t_{pLH} t_{pHL}		—	15	27	
Maximum Clock Frequency	f_{MAX}		27	48	—	MHz

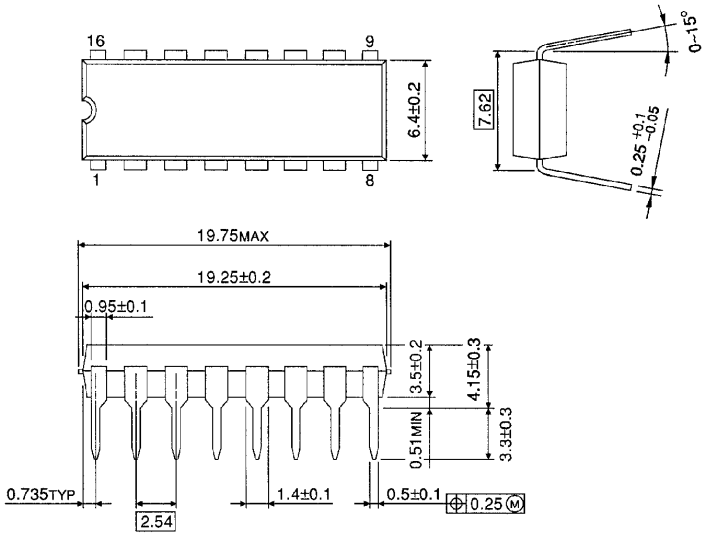
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C MIN.	TYP.	MAX.	Ta = −40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		2.0	—	88	180	—	225	
			4.5	—	22	36	—	45	
			6.0	—	19	31	—	38	
Propagation Delay Time (CK−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	52	120	—	150	
			4.5	—	13	24	—	30	
			6.0	—	11	20	—	26	
Propagation Delay Time (CK−MAX/MIN)	t_{pLH} t_{pHL}		2.0	—	108	240	—	300	
			4.5	—	27	48	—	60	
			6.0	—	23	41	—	51	
Propagation Delay Time (LOAD−Q)	t_{pLH} t_{pHL}		2.0	—	100	205	—	255	
			4.5	—	25	41	—	51	
			6.0	—	22	35	—	43	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		2.0	—	84	175	—	220	
			4.5	—	21	35	—	44	
			6.0	—	18	30	—	37	
Propagation Delay Time ($\overline{ENABLE}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	56	105	—	130	
			4.5	—	14	21	—	26	
			6.0	—	12	18	—	22	
Propagation Delay Time (D/$\overline{U}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	84	180	—	225	
			4.5	—	21	36	—	45	
			6.0	—	18	31	—	38	
Propagation Delay Time (D/$\overline{U}$−MAX/MIN)	t_{pLH} t_{pHL}		2.0	—	72	160	—	200	
			4.5	—	18	32	—	40	
			6.0	—	15	27	—	34	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	—	4	—	MHz
			4.5	25	44	—	20	—	
			6.0	29	52	—	24	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	101	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

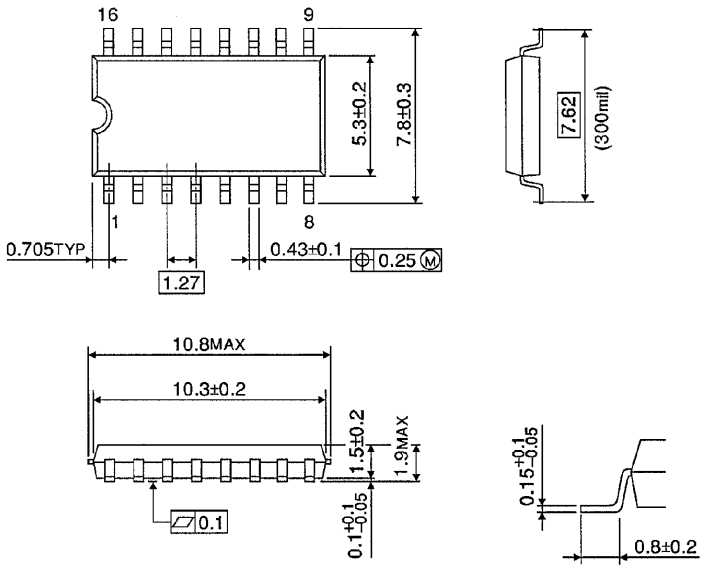
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

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