SL1914

Satellite Tuner Front End LNA with AGC
Preliminary Information

DS5137 ISSUE 1.6 April 1999

Features
- Single chip solution for satellite tuner LNA and AGC
- Provides for 30 dB minimum AGC
- Low DSB NF at maximum gain
- High signal handling at minimum gain
- Provides differential output drive
- ESD protection (Normal ESD handling procedures should be observed)

Applications
- Satellite receiver systems
- Data communications systems
- Master Antennae Distribution Systems

Ordering Information
SL1914A/KG/MP1S
SL1914A/KG/MP1T

Description
The SL1914 is a wideband LNA with AGC designed primarily for application in satellite tuner front ends, offering high signal handling capability with low noise figure compatible with most common tuner input requirements.

The SL1914 is optimised to complement the SL1925, ZIF quadrature downconverter, integrating all the active RF circuitry within the tuner, in a highly compact, efficient solution, and offering a full 1-45 MS/s tuner capability.

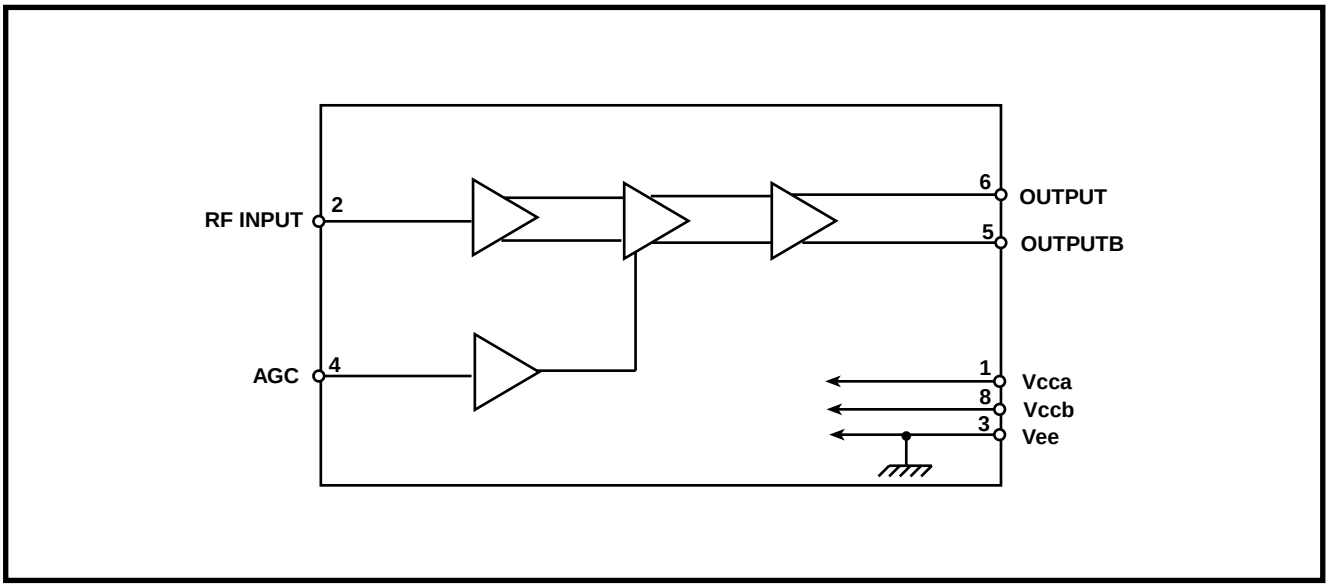
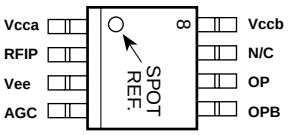


Figure 1 Block Diagram



MP8

Figure 2 Pin Connections

Quick Reference Data

Characteristic		Units
Operating frequency	950 - 2150	MHz
Input DSB NF at max gain	9	dB
Maximum conversion gain	20	dB
Minimum conversion gain	-10	dB
$IPIP3_{2T}$	117	dBµV
$IPIP2_{2T}$	127	dBµV

Table 1

Functional Description

The SL1914 is a bipolar, low noise AGC amplifier designed primarily for application in satellite tuner front ends. It contains a low noise input amplifier, an AGC stage with a minimum of 30dB of gain control and a 75 Ohm output drive. It replaces all active circuitry in conventional architectures.

The typical key performance numbers under nominal load ambient and supply conditions are contained in table headed Quick Reference Data.

Electrical Characteristics

T_{amb}= -20^{o}C to +70^{o}C, V_{ee}= 0V, Vcc = 5V±5%, These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1, 8		110	150	mA	AGC = 4V
Operating range		950		2150	MHz	
Input impedance	2		75		Ω	
IF input return loss	2	8			dB	
Input DSB NF	2		9	11	dB	Maximum gain, AGC = 0.75V
Variation in NF with gain setting				-1	dB/dB	
Conversion gain						Differential power gain into 75Ω
minimum				-10	dB	Vagc = 4V See note 1.
maximum		21			dB	Vagc = 0.75V
					dB	AGC monotonic from Vee to Vcc
Gain variation within channel				+0.5	dB	Maximum channel bandwidth of 54MHz, within range 950 - 2150MHz
Input referred 1 dB gain compression	2	107			dBμV	Minimum specified gain setting
Input referred IP3	2	117			dBμV	Minimum specified gain setting, two tones at 99dBμV
Input referred IP2	2	125			dBμV	Minimum specified gain setting, two tones at 99dBμV
Variation in second and third order intermodulation intercept points with gain setting				-1	dB/dB	
AGC control slope variation	4			4:1		
AGC control input current	4			±350	μA	
Output impedance	5, 6		75		Ω	
Output return loss	5, 6	6			dB	

Note 1: The AGC voltage should not exceed 4V.

Absolute Maximum Ratings

All voltages referred to Vee at 0V.

Characteristics	Min	Max	Unit	Conditions
Supply voltage	-0.3	7	V	
IFIN and IFINB input voltage		117	dBμV	Transient condition only
All I/O port DC offset	-0.3	VCC+0.3	V	Except AGC (pin 4)
AGC input DC offset	-0.3	4	V	
Storage temperature	-55	150	°C	
Junction temperature		150	°C	
Package thermal resistance, chip to case		39.8	°C/W	
Package thermal resistance, chip to ambient		120	°C/W	
Power consumption at 5.25V		790	mW	
ESD protection	2		kV	Mil std-883 latest revision method 3015 class 1

Marker	Freq (MHz)	Z real Ω	Z imag Ω
1	950	77	-6
2	1250	80	-34
3	1550	44	-44
4	2150	29	-35

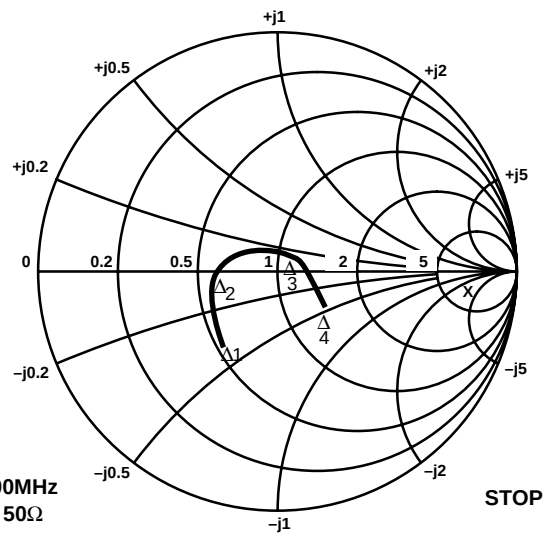
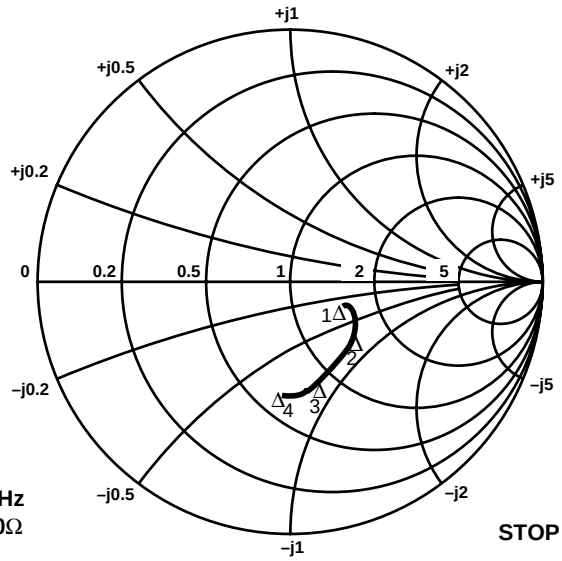


Figure 3 Input impedance (typical)

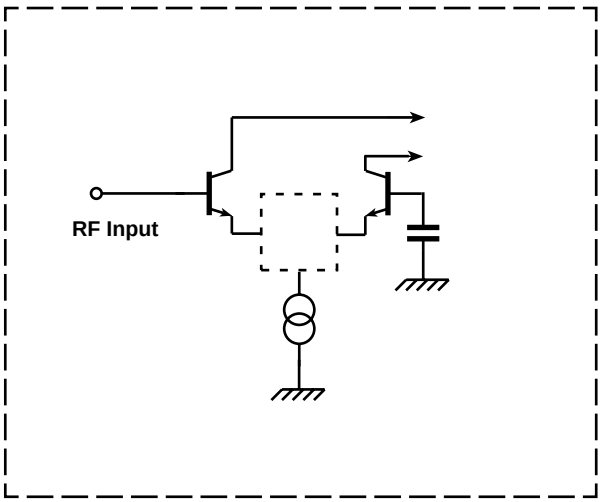
Marker	Freq (MHz)	Z real Ω	Z imag Ω
1	950	34	-16
2	1250	35	2
3	1550	58	68
4	2150	84	-30



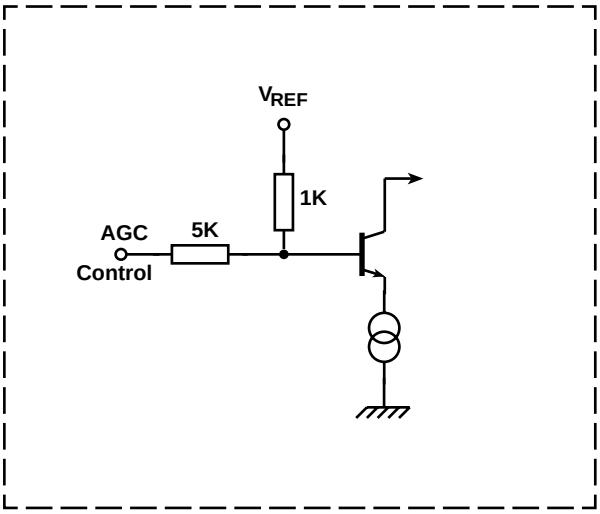
START 950.000 000MHz
NORMALISED TO 50Ω

STOP 2 150.000 000 MHz

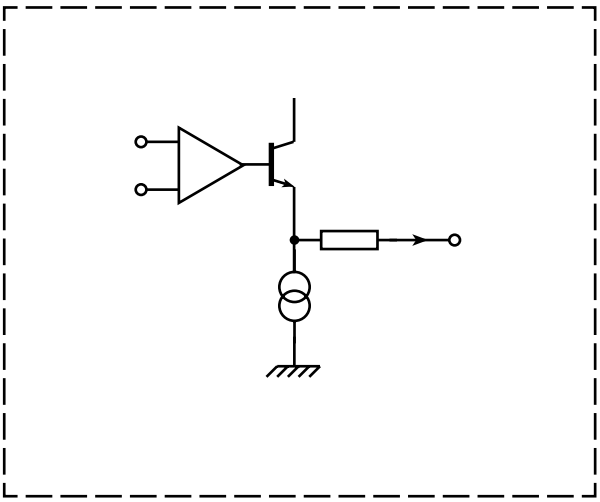
Figure 4 Output impedance (typical)



RF Input (pin 2)



AGC Input (pin 4)



RF outputs (pins 5, 6)

Figure 6 Input/Output interface circuit

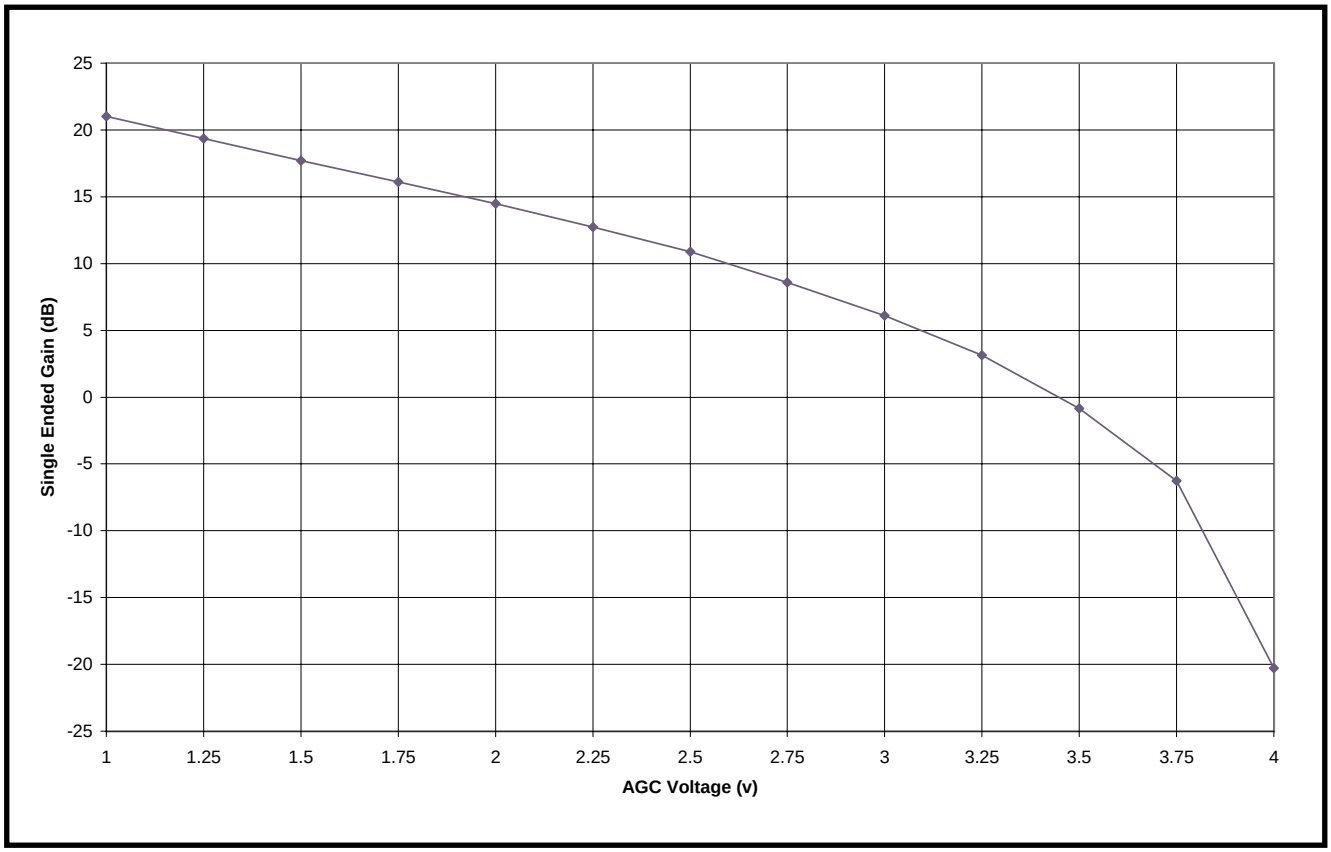
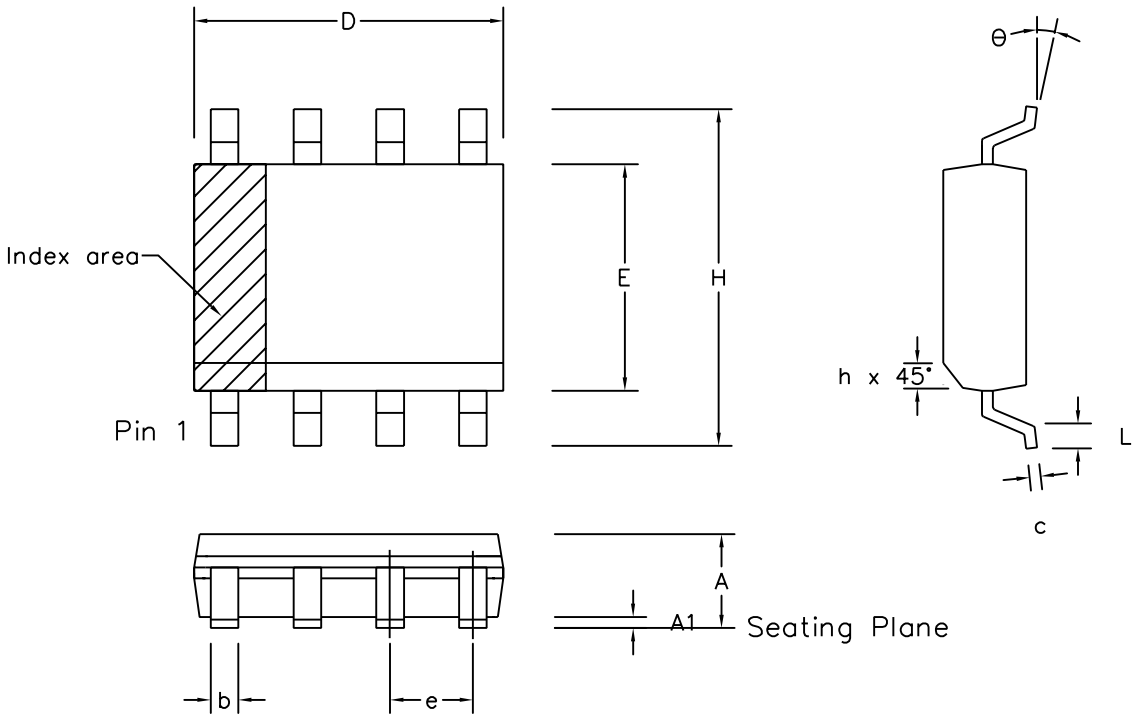


Figure 5 gain variation with AGC voltage (typical)



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010

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