

3V, 1.8GHz TO 2.8GHz LINEAR POWER AMPLIFIER

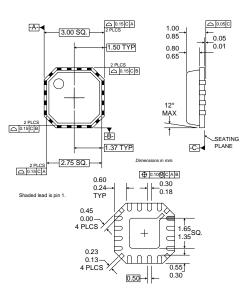
Typical Applications

- IEEE802.11B WLAN Applications
- IEEE802.11G WLAN Applications
- 2.5 GHz ISM Band Applications

Product Description

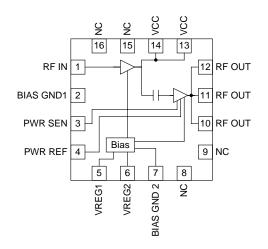
The RF5117C is a linear, medium-power, high-efficiency amplifier IC designed specifically for battery-powered WLAN applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz WLAN and other spread-spectrum transmitters. The device is provided in a 3mmx3mm, 16-pin, leadless chip carrier with a backside ground. The RF5117C is designed to maintain linearity over a wide range of supply voltage and power output.

- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Optimum Technology Matching® Applied

•		• • • •
🗌 Si BJT	🗹 GaAs HBT	GaAs MESFET
Si Bi-CMOS	SiGe HBT	Si CMOS
InGaP/HBT	GaN HEMT	SiGe Bi-CMOS



Functional Block Diagram

Package Style: QFN, 16-Pin, 3x3

Features

- Single 3.3V Power Supply
- +30dBm Saturated Output Power
- 26dB Small Signal Gain
- High Linearity
- 1800 MHz to 2800 MHz Frequency Range
- +17dBm P_O, 11G, <3% EVM

Ordering Information

RF5117C 3V, 1.8GHz to 2.8GHz Linear Power Amplifier RF5117C PCBA Fully Assembled Evaluation Board

 RF Micro Devices, Inc.
 Tel (336) 664 1233

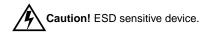
 7628 Thorndike Road
 Fax (336) 664 0454

 Greensboro, NC 27409, USA
 http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
	-0.5 to +6.0	
Supply Voltage		V _{DC}
Power Control Voltage (V _{REG})	-0.5 to 3.5	V
DC Supply Current	600	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC Level 2	

Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.



RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Deremeter	Specification		11	Condition		
Parameter	Min.	Min. Typ. Max.		Unit	Condition	
Overall					T=25 ℃, V _{CC} =3.0V, V _{REG} =2.7V, Freq=2450MHz, circuit per evaluation board schematic.	
Frequency Range		1800 to 2800		MHz		
Maximum Linear Output Power					With 802.11B modulation (11Mbit/s) and meeting 802.11B spectral mask.	
VCC=3.0V		22		dBm		
VCC=5.0V		27		dBm		
Linear Efficiency		25		%		
Error Vector Magnitude (EVM)		2.5		%	P _O =17dBm, EVM increases over 11g, 54MBPS signal input	
Small Signal Gain	24	26	28.5	dB	P _{IN} =-7dBm	
Reverse Isolation	30			dB		
Second Harmonic		-35		dBc		
802.11B Adjacent Channel Power		-38	-32	dBc	$P_{OUT}=21 dBm, V_{CC}=3.0 V$	
Alternate Channel Power		-56	-52	dBc	P _{OUT} =21dBm, V _{CC} =3.0V	
Isolation	35	45		dB	In "OFF" state, P _{IN} =-5.0dBm	
Input Impedance		50		Ω	With external matching	
Input VSWR		2:1			With external matching	
Power Down						
V _{REG} "ON"	2.1	2.7	3.0	V	Voltage supplied to control input; device is "ON"	
V _{REG} "OFF"		0	0.5	V	Voltage supplied to control input; device is "OFF"	
Power Supply						
Operating Voltage		3.0 to 5.0		V		
Current Consumption		500		mA	At max output power	
		200	220	mA	P _{OUT} =21dBm, V _{CC} =3.0V	
		110		mA	Idle current, V _{CC} =3.0V, V _{REG} =2.7V	
V _{REG} Current (Total)		5	10	mA	V _{CC} =3.0V	
		10	15	mA	V _{CC} =5.0V	

Pin	Function	Description	Interface Schematic
1	RF IN	RF input. Matching network with DC block required, see evaluation board schematic for details.	RF IN O
2	BIAS GND1	Ground for first stage bias circuit. Not connected.	See pin 5.
3	PWR SEN	The PWR SEN and PWR REF pins can be used in conjunction with an external feedback path to provide an RF power control function for the RF5117C. The power control function is based on sampling the RF drive to the final stage of the RF5117C.	ORF OUT
4	PWR REF	Same as pin 3.	See pin 3.
5	VREG1	This pin requires a regulated supply to maintain nominal bias current.	VREG1 O- BIAS VREG2 O- BIAS BIAS GND1 GND2
6	VREG2	Same as pin 5.	See pin 5.
7	BIAS GND2	Ground for second stage bias circuit. For best performance connect to ground with a 10nH inductor.	See pin 5.
8	NC	Not connected.	
9	NC	Not connected.	
10	RF OUT	RF output and bias for the output stage. The power supply for the out- put transistor needs to be supplied to this pin. This can be done through a quarter-wave length microstrip line that is RF grounded at the other end, or through an RF inductor that supports the required DC cur- rents.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	See pin 10.
13	VCC	Interstage match and bias for first stage output. Connect interstage matching capacitor to this pad with a short trace. Connect low-fre- quency bypass capacitors to this pin with a long trace. See evaluation board layout for details.	See pin 1.
14	VCC	Same as pin 13.	See pin 1.
15	NC	Not connected.	
16	NC	Not connected.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device will be required.	

Theory of Operation and Application Information

The RF5117C is a two-stage device with a nominal gain of 26dB in the 2.4GHz to 2.5GHz ISM band. The RF5117C is designed primarily for IEEE802.11B/11G WLAN applications where the available supply voltage and current are limited. This amplifier will operate to (and below) the lowest expected voltage made available by a typical PCMCIA slot in a laptop PC, and will maintain required linearity at decreased supply voltages.

The RF5117C requires only a single positive supply of 3.0V nominal (or greater) to operate to full specifications. Power control is provided through two bias control input pins (V_{REG1} and V_{REG2}), but in most applications these are tied together and used as a single control input.

There is some external matching on the input and output of the part, thus allowing the part to be used in other applications outside the 2.4GHz to 2.5GHz ISM band (such as MMDS). Both the input and the output of the device need a series DC-blocking capacitor. In some cases, a capacitor used as a matching component can also serve as the blocking cap. The circuit used on the evaluation board is optimized for 3.0V nominal applications.

For best results, the PA circuit layout from the evaluation board should be copied as closely as possible, particularly the ground layout and ground vias. Other configurations may also work, but the design process is much easier and quicker if the layout is copied from the RF5117C evaluation board. Gerber files of our designs can be provided upon request.

The RF5117C is not a difficult part to implement, but care in circuit layout and component selection is always advisable when designing circuits to operate at 2.5GHz. The most critical passive components in the circuit are the input, interstage and output matching components (C1, C5, and C11). In these cases, high-Q capacitors suitable for RF applications are used on our evaluation board (a BOM is available on request). High-Q parts are not required in every design, but it is very strongly recommended that the original design be implemented with the same or similar parts used on our evaluation board. Then, less costly components can be substituted in their place, making it easy to test the impact of cheaper components on performance. General RFMD experience has indicated that the slightly higher cost of better quality passive components is more than offset by the significant improvements in production yields in large-volume manufacturing. Using less costly components will typically result in a 1 to 2dB degradation in gain.

The interstage matching capacitor, C11, along with the combined inductance of the internal bond wire, the short length of circuit board trace, and the parasitic inductance of this capacitor, tunes the peak of the small-signal gain response. The trace length between C11 and pins 13 and 14 should be kept as short as possible.

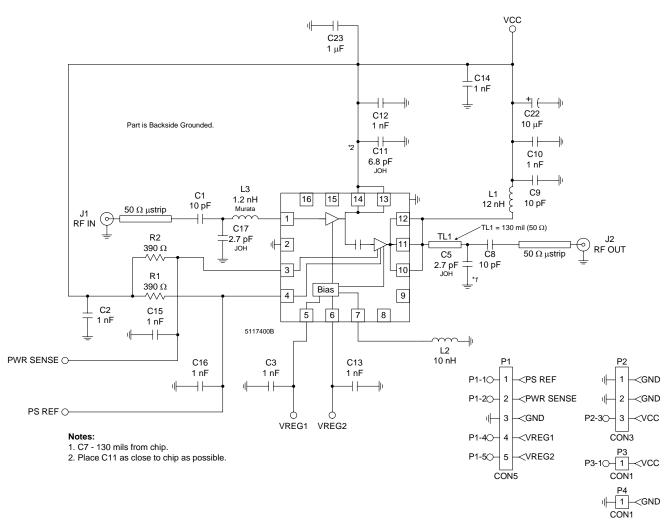
In practice, V_{CC} and the supply for the output stage bias will be tied to the same supply. It is important to isolate C11 from other RF and low-frequency bypass capacitors on this supply line. This can be accomplished using a suitably long transmission line which is RF shorted on the other end. Ideally the length of this line will be a quarter wavelength, but it only needs to be long enough so that the effects of other supply bypass capacitors on the interstage match are minimized. If board space is a concern, this isolation can also be accomplished with an RF choke inductor or ferrite bead. Additionally, a higher-value capacitor than shown on the application schematic can be used if bypass capacitors must be closer. A Smith Chart can be used to provide initial guidance for value selection and parts placement. Be aware of the self-resonant frequency (SRF) of higher-valued capacitors. The SRF must be above the frequency of operation.

The output matching capacitor is C5, located 130mils from the IC (this distance should be duplicated as closely as possible). Due to variations in FR-4 characteristics and PCB manufacturer process variations, some benefit will be obtained from small adjustments to these transmission line lengths when the evaluation board layout is duplicated on another design. Prior to full rate manufacturing, the board layout of early prototypes should include some additional exposed ground areas around C5 to optimize this part of the circuit. A Smith Chart can help determine the desired value and transmission line length, which can be similarly adjusted on the board prior to production.

The RF5117C can be used with an IEEE802.11g modulation with a few modifications. Pin 2 should not be connected to ground and a $4.7 k\Omega$ resistor should be placed on the V_{REG1} line. This is done on the evaluation board by cutting the V_{REG1} trace and placing the resistor on the open line. All other components should not be modified and the IEEE802.11g schematic should be followed as closely as possible.

Power sensing is implemented with the PWR SEN and PWR REF lines. The outputs of these pins are transistor collectors and need to be pulled up to the supply through a resistor. PWR REF provides an output current proportional to the output stage bias current, and PWR SEN provides an output current proportional to the total (RF and bias) current of the output stage. The pull-up resistors convert these currents to voltages, and the voltage difference between these two pins is proportional to the RF current. See the graph, " V_{REF} - V_{SENSE} versus P_{OUT} ", for the response of this signal. This difference signal can be fed to a power control circuit elsewhere in the end product, or it can be processed at the PA with additional circuitry and used to adjust the V_{REG} voltage(s) to implement automatic level control. Contact RFMD Sales or Applications Engineering for additional data and guidance in using this feature.

The RF5117C has primarily been characterized with a voltage on V_{REG1} and V_{REG2} of 2.7 V_{DC} . However, the RF5117C will operate from a wide range of control voltages. If you prefer to use a control voltage that is significantly different than 2.7 V_{DC} , contact RFMD Sales or Applications Engineering for additional data and guidance.



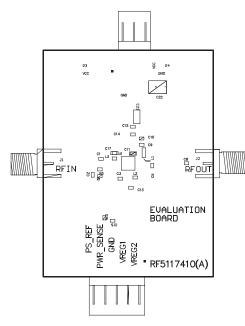
Evaluation Board Schematic - IEEE802.11b 2400MHz to 2483MHz

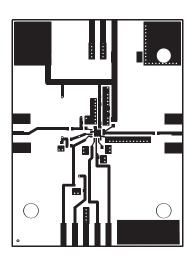
++ıŀ C23 VCC 1 μF \bigcirc ⊥C14 ⊤1 nF + (-41 -11 C22 C12 Place C11 as close 10 μF Part is Backside Grounded to chip as possible 1 nF 41 *3 Ċ11 C10 6.8 pF 1 nF JOH ++L3 L1 { 12 nH { C9 C1 1.2 nH 16 15 13 14 +10 pF 10 pF 50 Ω µstrip Murata J1 41 1 12 -TL1 = 130 mil (50 Ω) C17 TL1 R2 2.7 рF _{ЈОН} J2 2 *2-11 $390 \ \Omega$ **RF OUT** 50 Ω µstrip C5 Ċ8 \sim 2.7 pF _{ЈОН} 10 pF 10 3 Т R1 *1 390 O Bias 4 \sim 9 5 C2 C15 6 7 8 1 nF 1 nF 5117400B \mathbb{H} \dashv _ 4 L2 PWR SENSE O-10 nH C16 СЗ C13 P1 1 nF 1 nF 1 nF P1-10-1 -< PS REF <GND ⊪ ╟ ++-11-4 P1-20-2 - PWR SENSE -<GND R3 1 2 $_{*4} \gtrsim 4.3 \text{ k}\Omega$ PS REF () 3 -<vcc ᆘ 3 -<GND P2-30-Notes: 1. C7 - 130 mils from chip. Q Ć P1-40-4 -</KEG1 CON3 2. Pin 2 cut from ground. 3. C11 must be placed as close to chip as possible. VREG1 VREG2 P3 P3-10-1-<VCC P1-50- 5 -</ 4. The V_{REG} trace is cut and a 4.7 k Ω resistor is placed on the trace. CON5 CON1 Ρ4 CON1

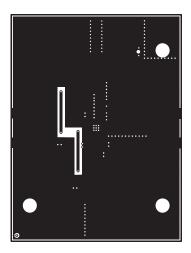
Evaluation Board Schematic - IEEE802.11g 2400MHz to 2483MHz

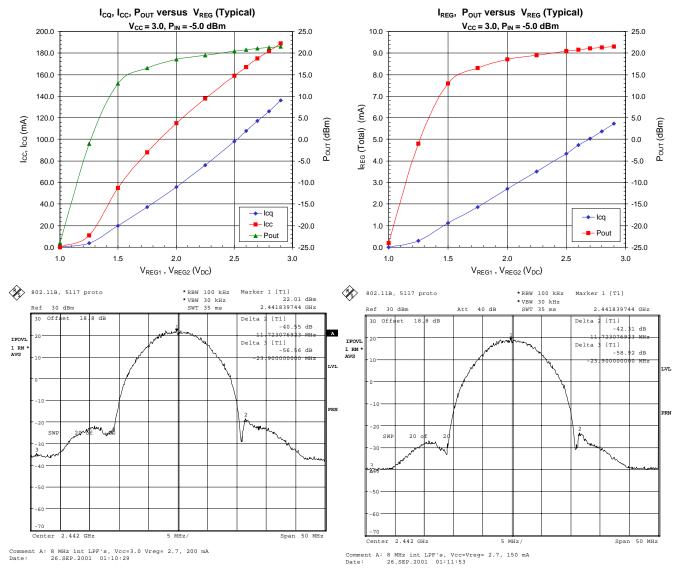
Evaluation Board Layout Board Size 1.5" x 2.0"

Board Thickness 0.031", Board Material FR-4, Multi-Layer

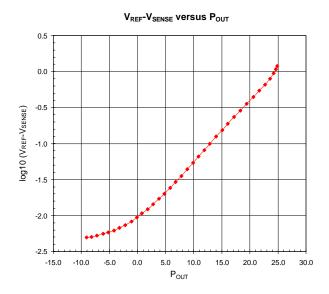


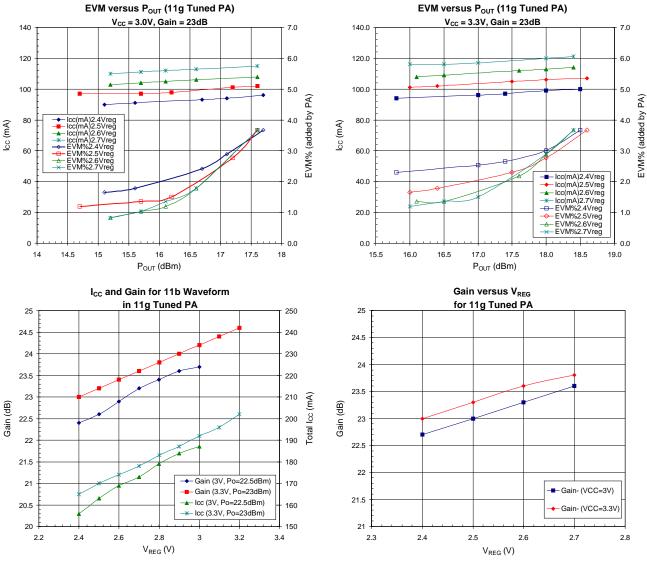






Spectral Plot: V_{CC} =3.0V, V_{REG1} = V_{REG2} =2.7VSpectral Plot: V_{CC} =2.7V, V_{REG1} = V_{REG2} =2.7V P_{OUT} =22.05dBm, P_{IN} =-4.1dBm, I_{CC} ~200mAP_{OUT}=19.05dBm, P_{IN} =-6.8dBm, I_{CC} ~150mA





Evaluation Board with 11g Tuning