MP8830

Triple 10-bit High Speed
Analog-to-Digital Converter with
Digitally Controlled References

FEATURES

- **3 Independent 10-bit ADCs**
- **Simultaneous Sampling @ 1.25 MSPS**
- **Independent Digitally Controlled References**
- **9-bit Positive Reference and 6-bit Negative Reference Adjustment per Sample**
- **Low Power: 500mW (typ)**
- **Internal Track and Hold**
- **Single 5 V Supply**
- **Fast Mode for OCR**
- **A_{IN} Input Range: 1.3 V to 2.6 V p-p**
- **Black Level Clamp**
- **Latch-Up Free**
- **ESD Protection: 2000 V Minimum**

BENEFITS

- **Pixel-to-Pixel Correction**
- **Improves Effective Resolution over Software Correction Schemes**
- **Reduced DSP/Processor Demands**
- **Reduction of Parts Count and System Cost**

APPLICATIONS

- **Precision CCD Systems**
- **Color and B&W Scanners**
- **Digital Copiers**
- **IR Cameras**

GENERAL DESCRIPTION

The MP8830 is a simultaneous sampling 1.25 MSPS triple 10-bit A/D Converter. It provides pixel-to-pixel correction of CCD or other inputs by updating gain and offset parameters supplied from an external correction memory. Each ADC has a 9-bit DAC driving its positive reference voltage and a 6-bit DAC driving its negative reference to independently adjust the gain and offset of each channel.

The MP8830 uses ADCs with a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance and performs an on-chip sample and hold function. The MP8830 uses proprietary high speed DACs to drive the ADC references which allows reference adjustment on every conversion at a 1.25 MHz rate. An internal clamp is available for DC restoration of A_{IN} black level.

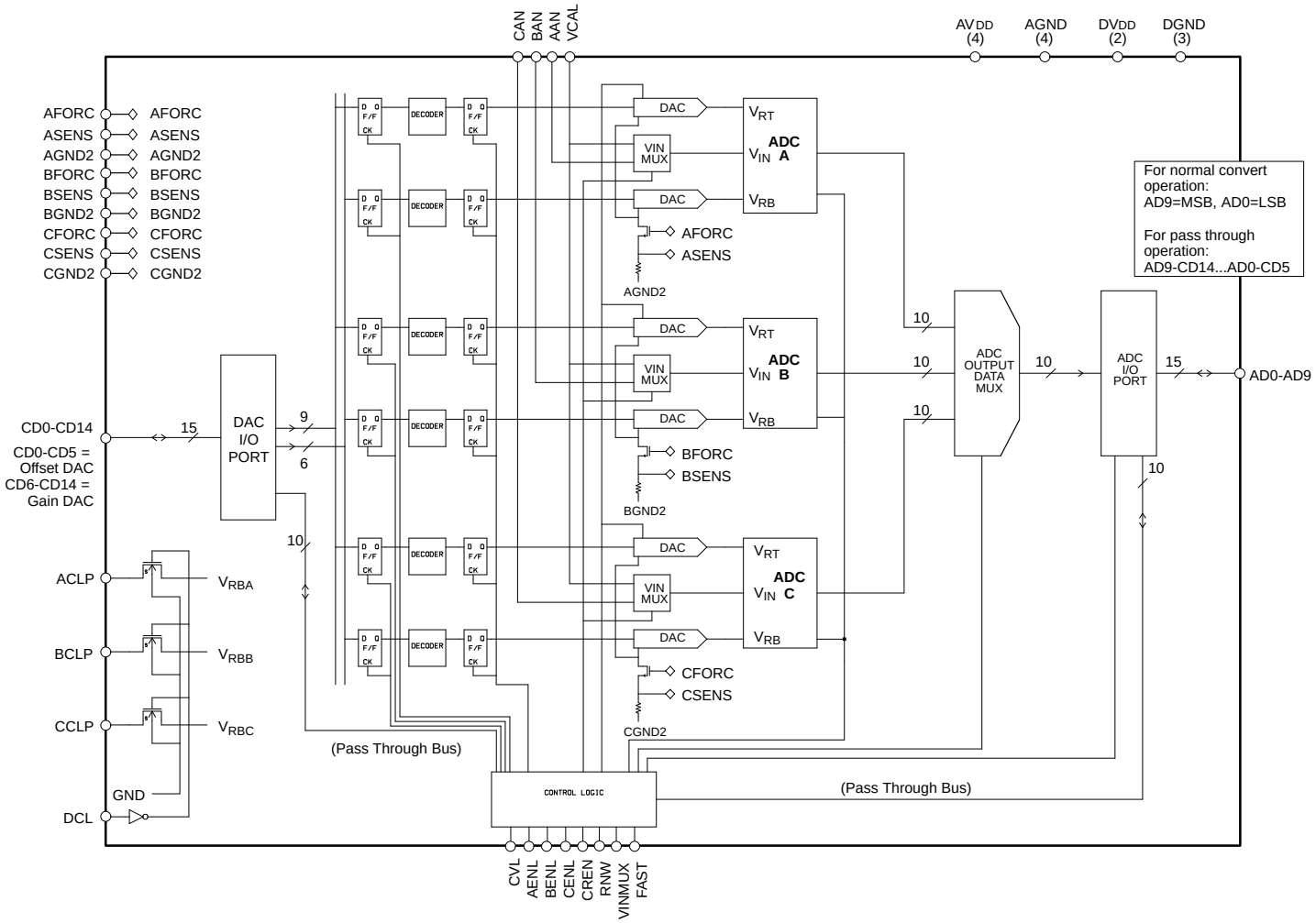
The MP8830 operates from a single 5 V supply and an external 1 V reference, and consumes only 500mW of power (typ).

Specified for operation over the temperature range 0 to 60°C, the MP8830 is available in a 64 lead Plastic Quad Flat Pack (PQFP) package.

ORDERING INFORMATION

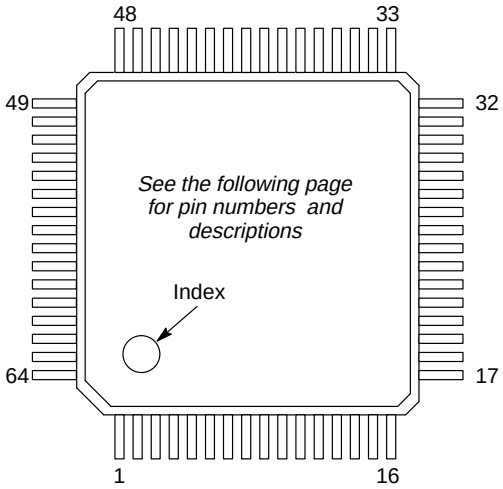
Package Type	Temperature Range	Part No.
PQFP	0 to +60°C	MP8830AE

BLOCK DIAGRAM



PIN CONFIGURATION

See Packaging Section for Package Dimensions



64 Pin PQFP
Q64

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DV_{DD}	Digital Positive Power Supply
2	CD14	DAC Input Pin 14
3	CD13	DAC Input Pin 13
4	CD12	DAC Input Pin 12
5	CD11	DAC Input Pin 11
6	CD10	DAC Input Pin 10
7	CD9	DAC Input Pin 9
8	CD8	DAC Input Pin 8
9	CD7	DAC Input Pin 7
10	CD6	DAC Input Pin 6
11	CD5	DAC Input Pin 5
12	CD4	DAC Input Pin 4
13	CD3	DAC Input Pin 3
14	CD2	DAC Input Pin 2
15	CD1	DAC Input Pin 1
16	CD0	DAC Input Pin 0
17	CV_{DD}	Analog Positive Power Supply
18	CSENS	Sensing Voltage for Biasing the C Channel
19	CFORC	Forcing Voltage for Biasing the C Channel
20	CAN	C Channel Analog Input
21	CGND2	Analog Ground Related to DAC Bias
22	CCLP	Clamp Voltage C
23	CGND1	Analog Negative Power Supply
24	BV_{DD}	Analog Positive Power Supply
25	BSENS	Sensing Voltage for Biasing the B Channel
26	BFORC	Forcing Voltage for Biasing the B Channel
27	BAN	B Channel Analog Input
28	BGND2	Analog Ground Related to DAC Bias
29	BCLP	Clamp Voltage B
30	BGND1	Analog Negative Power Supply
31	AV_{DD}	Analog Positive Power Supply
32	AGND2	Analog Ground Related to DAC Bias

PIN NO.	NAME	DESCRIPTION
33	ASENS	Sensing Voltage for Biasing the A Channel
34	AFORC	Forcing Voltage for Biasing the A Channel
35	AAN	A Channel Analog Input
36	AGND1	Analog Negative Power Supply
37	ACLP	Clamp Voltage A
38	VCAL	Calibration Input Voltage
39	VINMX	Analog Mux Control
40	DGND	Digital Negative Power Supply
41	DCL	Black Level Clamp Control (Active Low)
42	N/C	No Connection
43	DGND	Digital Negative Power Supply
44	DV_{DD}	Digital Positive Power Supply
45	FAST	FAST Mode Enable
46	GND3	Analog Negative Power Supply
47	V_{DD3}	Analog Positive Power Supply
48	CREN	Pass Through Mode Enable
49	RNW	READ not WRITE
50	CENL	Channel C Data Clock
51	BENL	Channel B Data Clock
52	AENL	Channel A Data Clock
53	CVL	Cycle Clock
54	AD9	ADC Data Output 9
55	AD8	ADC Data Output 8
56	AD7	ADC Data Output 7
57	AD6	ADC Data Output 6
58	AD5	ADC Data Output 5
59	AD4	ADC Data Output 4
60	AD3	ADC Data Output 3
61	AD2	ADC Data Output 2
62	AD1	ADC Data Output 1
63	AD0	ADC Data Output 0
64	DGND	Digital Negative Power Supply

Note: All digital signals are active high unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: $AV_{DD} = DV_{DD}$= 5 V, DGND = AGND = 0 V, $V_{REF} = AV_{DD} \times 0.2$ Temperature = 0 to 60°C[1]

A/D Converters						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions/Comments**
Resolution	N	10			Bits	
Differential Non-Linearity	DNL	–1	±0.75	2	LSB	Gain DAC = 000 (hex), offset DAC = 00 (hex). Monotonicity guaranteed.
Differential Non-Linearity	DNL	–1	±0.5	2	LSB	Gain DAC = 1FF (hex), offset DAC = 00 (hex). Monotonicity guaranteed.
Integral Non-Linearity	INL		2	2.75	LSB	Gain DAC = 000 (hex), offset DAC = 00 (hex), Best fit straight line.
Integral Non-Linearity	INL		1.5	2	LSB	Gain DAC = 1FF (hex), offset DAC = 00 (hex), Best fit straight line.
Zero Scale Error	ZSE	–15		9	mV	Measured with offset and gain DACs set to 000. Offset is defined as the difference between the clamp voltage and the analog input voltage which results in the transition of the ADC code from 004 to 005.
Zero Scale Drift[2]	ZSD		50		µV/°C	Measured as the change in the ZSE over temperature. This error does not include the error introduced by the external V_{REF} amplifier or external V_{REF} resistor divider.
DC Input Range	A_{IN}	VCLP –5mV		2.92 V + VCLP –5 mV	V	The digitizing range is set with the Gain DAC and offset DAC. Please note A_{IN} (min) is VCLP – 4 LSB = V_{RB} and A_{IN} (max) is GFS (max) + ZSR (max) + VCLP – 4 LSB.
Data Rate	FS	1.25			MSPS	The conversion rate is determined by the timing diagram and timing specifications. Set by the CVL period.
Analog Input Voltage Change from Sample to Sample[2]	ΔA_{IN}	0		±FS	V	Assuming A_{IN} voltage remains within the specified digitizing range based on the offset and gain DAC codes.
Input Capacitance[2]	C_{IN}			45	pF	Measured with A_{IN} DC = 2.5 V and AENL = low.
Gain DAC						
Resolution	N		9		Bits	
Differential Non-Linearity	DNL	–1		+2.25	LSB	
Integral Non-Linearity	INL			+2	LSB	
Gain DAC Full Scale ($V_{RT} – V_{RB}$)	GFS	2.6	2.68	2.76	V	Gain DAC = 1FF V_{RT} is the top of the ADC reference ladder. Refer to block diagram.
Gain DAC Zero Scale ($V_{RT} – V_{RB}$)	GZS	1.22	1.26	1.3	V	Gain DAC = 000 V_{RB} is the bottom of the ADC reference ladder. Refer to block diagram.
Maximum Gain Change per Cycle[2]	MGC			50	% FSR	After the specified maximum change in gain DAC setting, the ADC should output the same code ±1 LSB for all of the following conversions assuming the analog input remains fixed, i.e. DC.
Settling Time (MGC)[2]	ts-gd		200		ns	

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comments
Offset DAC						
Resolution	N		6		Bits	
Differential Non-Linearity	DNL	–0.5		0.5	LSB	
Integral Non-Linearity	INL			1	LSB	
V_{RB} Range	ZSR	152	158	164	mV	This is measured as the voltage difference at the clamp pin of the selected channel when the offset DAC changed from 000 (hex) to 3F (hex) with the gain DAC at 1FF (hex). Refer to V_{RT} and V_{RB} EQNs in the theory of operation section.
Maximum Offset Change per Cycle[2]	MOC			100	% FSR	After the specified maximum change in offset DAC setting, the ADC should output the same code ±1 LSB for all of the following conversions assuming the analog input remains fixed, i.e. DC.
Full Scale Settling Time[2]	ts-od		200		ns	For a 00 (hex) to 3F (hex) change of offset DAC code.
Black Level Clamp Switch						
On Resistance	R_{ON}		100	150	Ω	Effective R_{IN} at clamp pin.
Input Leakage	IL_{CLP}			25	nA	Offset DAC at 00 (hex) (worst case condition).
Clamp Switching Charge Injection[2]	Q_{CLP}			50	pC	Offset DAC at 00 (hex) (worst case condition).
Voltage at Clamp Pin	V_{CLP}	170	180	190	mV	Offset by 4 LSB from bottom tap of ADC ladder. Gain = 000 (H). Offset DAC = 00.
Reference Voltage Requirements (See Theory of Operation)						
Reference Voltage	V_{REF}	0.93	1	1.07	V	All linearity specifications assume the reference voltage = AV_{DD} X (0.2).
		0.5		1.15	V	Functional.
Calibration Voltage	VCAL	AGND		AV_{DD}	V	
Sense Pins Input Resistance (ASENS, BSENS, CSENS)	RINS		560		Ω	RINS is measured from the sense pin to AGND2, BGND2, CGND2 with the power turned off and test voltage less than 250 mV.
Power Supplies (Note: All GND pins are substrate)						
Analog Positive Supply	AV_{DD}	4.75	5	5.25	V	Bypass power supply pins.
Digital Positive Supply	DV_{DD}	AV_{DD}	AV_{DD}	AV_{DD}	V	Bypass power supply pins.
Analog Negative Supply	AGND	0	0	0	V	
Digital Negative Supply	DGND	0	0	0	V	
Power Supply Rejection	PSRR			–60	dB	f=1 KHz.
Supply Current	I_{DD}		100	130	mA	During specified operation.
Digital Characteristics						
Digital Input High Voltage for Control Pins	V_{IH}	3.5			V	All digital input pins other than DAC data inputs.
Digital Input Low Voltage for Control Pins	V_{IL}			1.5	V	All digital input pins other than DAC data inputs.
Digital Input High Voltage for DAC Input Pins	V_{IH}	2.4			V	DAC data inputs, CD0-CD14
Digital Input Low Voltage for DAC Input Pins	V_{IL}			0.4	V	DAC data inputs, CD0-CD14
V_{OL}	V_{OL}			0.5	V	@ I_{OL} = 4 mA
V_{OH}	V_{OH}	4.5				@ I_{OH} = 4 mA
Digital Input Leakage Current	I_{IN}	–10		10	µA	

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions/Comments
3-State Leakage	I_{OZ}	–10		10	µA	In pass-through mode
Digital Timing Specifications[2]						For testing, rise time = fall time = 10 ns. Output loading = 60 pF except for AD0-AD9 for which loading is 40 pF. Rise and fall times faster than 5 ns should be avoided.
AENL, BENL, CENL Pulse Width	t_1	125			ns	
D/A Data Hold Time	t_2	20			ns	
BENL Rising Edge to CENL Rising Edge	t_3	270			ns	
AENL Rising Edge to CVL Falling Edge	t_4	30			ns	
D/A Data Setup Time	t_5	20			ns	
Analog Input Hold Time	t_6	20			ns	Measured as part of analog feedthrough test. Note, $t_{tapmax} < t_{4min} + t_{6min}$.
CVL Rising Edge to AENL Rising Edge	t_7	230			ns	
A/D Data Enable Time	t_8			40	ns	CVL to Channel A data. BENL to Channel B data. CENL to Channel C data.
CENL Rising Edge to CVL Rising Edge	t_9	40			ns	
Analog Input Settled to 0.1%	t_{10}	50			ns	Assumes the sample is taken at the rising edge of AENL.
A/D Data Hold Time	t_{11}	20			ns	
Aperture Delay	t_{AP}		20	40	ns	Analog sampling window delay from CVL rising (↑) edge (start) or AENL rising (↑) edge (end).
CVL Falling Edge to BENL Rising Edge	t_{12}	180			ns	
Delay from CD5-14 to AD0-9 with CREN=1	t_{13}			50	ns	
Delay from AD0-9 to CD5-14 with CREN = 1	t_{14}			50	ns	
Delay from DCL Falling Edge to Clamp on.	t_{15}			40	ns	External analog clamp voltage settling depends on external circuitry.
Delay from DCL Rising Edge to Clamp off.	t_{16}			40	ns	External analog clamp voltage settling depends on external circuitry.
Time for AD0-9 and CD5-14 to switch from normal operation to pass through mode or vise versa (i.e. bus contention).	t_{17}	0		40	ns	User should stop driving the bus before changing the mode and data will not be valid for 40 ns after a change of mode.
Digital Quiet Time	t_{18}	15			ns	This quiet time is necessary to reduce digital crosstalk during the critical sampling time. The accuracy of each conversion may be corrupted due to digital noise on the board during this period.
Digital Quiet Time	t_{19}	40			ns	This quiet time is necessary to reduce digital crosstalk during the critical sampling time. The accuracy of each conversion may be corrupted due to digital noise on the board during this period.

Notes
1 Production testing performanced at 25°C.
2 Not production tested.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted) [1, 2]

AV_{DD} to GND . . . . . 6 V
DV_{DD} to GND . . . . . 6 V
$AV_{DD} – DV_{DD}$ . . . . . 150 mV DC
All Inputs . . . . . V_{DD} +0.5 to GND –0.5 V
Storage Temperature . . . . . –65°C to 150°C
Lead Temperature . . . . . 300°C

ESD Rating . . . . . 2000 V on all pins.

Package Power Dissipation Rating @ 75°C
PQFP . . . . . 1100 mW
Derates above 75°C . . . . . 15 mW/°C
T_{JMAX} . . . . . 150°C

NOTES:
1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All logic inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

TRUTH TABLE

Function	CVL	AENL	BENL	CENL	CREN	RNW	VINMX	FAST	DCL
Start A_{IN} tracking	↑	1	1	1	0	X	0	X	X
Sample A_{IN}	1	↑	1	1	0	X	0	X	X
MSB convert	0	1	0	1	0	X	0	X	X
LSB convert	0	1	1	0	0	X	0	X	X
Output A ADC data from previous sample	↑	1	1	1	0	X	0	X	X
Output B ADC data from previous sample	X	1	↓	1	0	X	0	X	X
Output C ADC data from previous sample	X	1	1	↓	0	X	0	X	X
Load channel A data to first A DAC register	X	↓	1	1	0	X	0	X	X
Load channel B data to first B DAC register	X	1	↓	1	0	X	0	X	X
Load channel C data to first C DAC register	X	1	1	↓	0	X	0	X	X
Update second register for all DACs	↑	1	1	1	0	X	0	X	X
Turn on all black level clamp switches	X	X	X	X	X	X	X	X	0
Pass-through mode: ADC port in, DAC port out	X	X	X	X	1	0	X	X	X
Pass-through mode: DAC port in, ADC port out	X	X	X	X	1	1	X	X	X
ADC inputs connect to VCAL	X	X	X	X	X	X	1	X	X
Put ADCs in 4-bit mode	X	X	X	X	X	X	X	1	X

TIMING DIAGRAMS

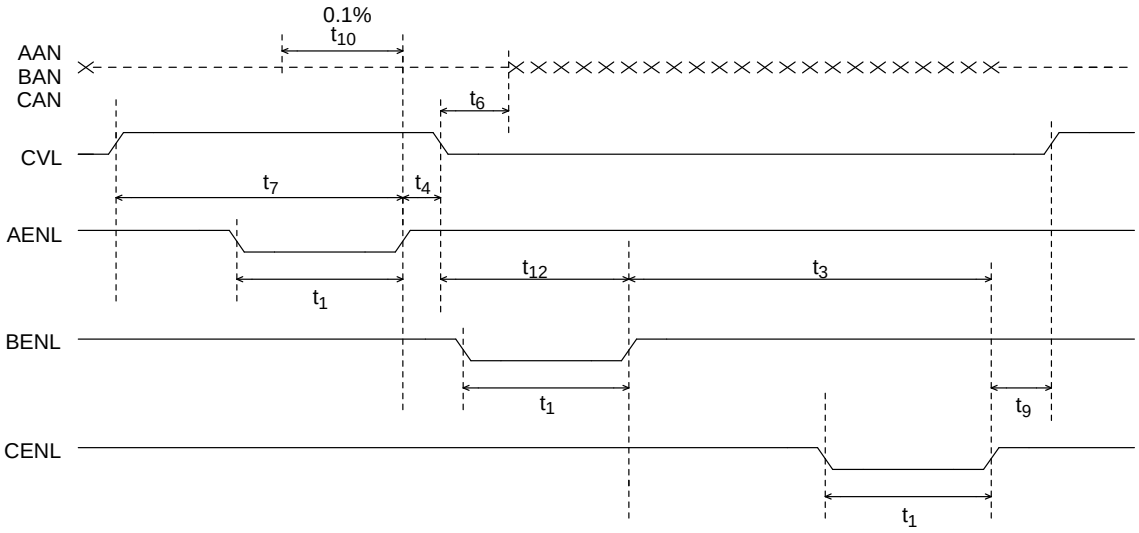


Figure 1. Clock Timing for Convert Mode

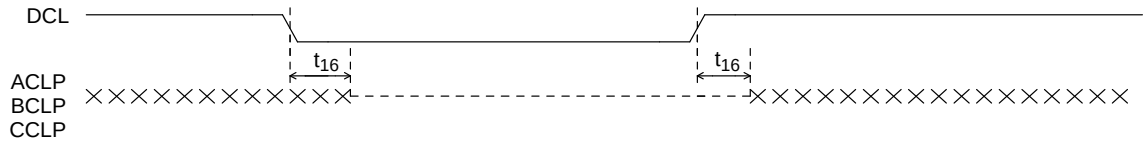


Figure 2. DC Clamp Operation

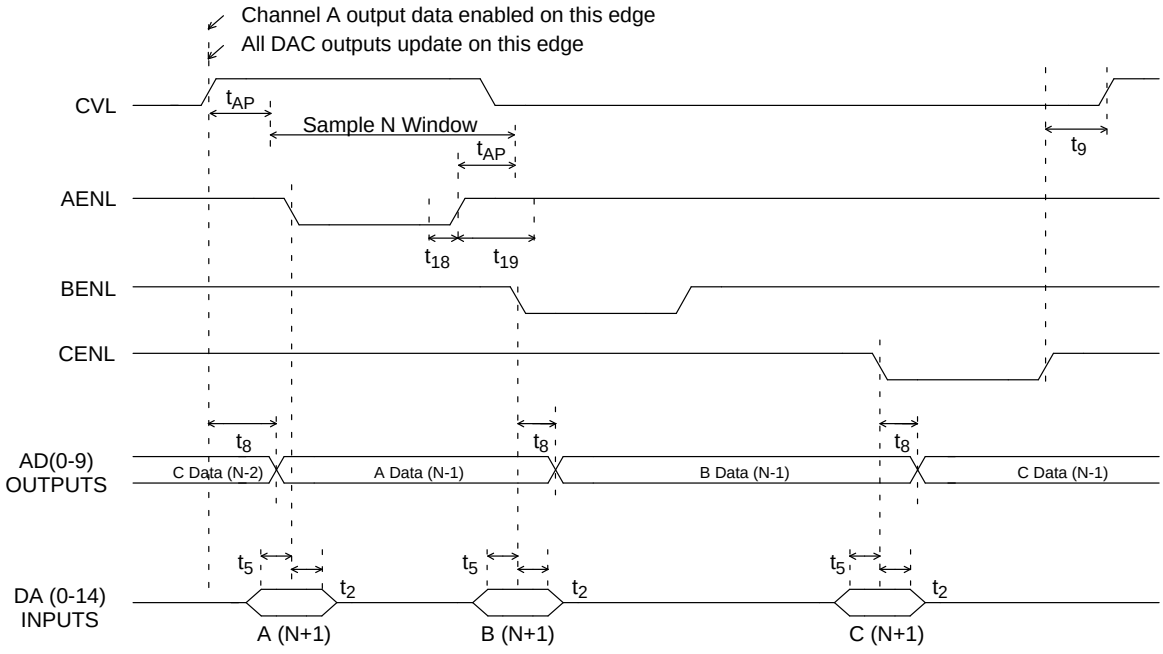
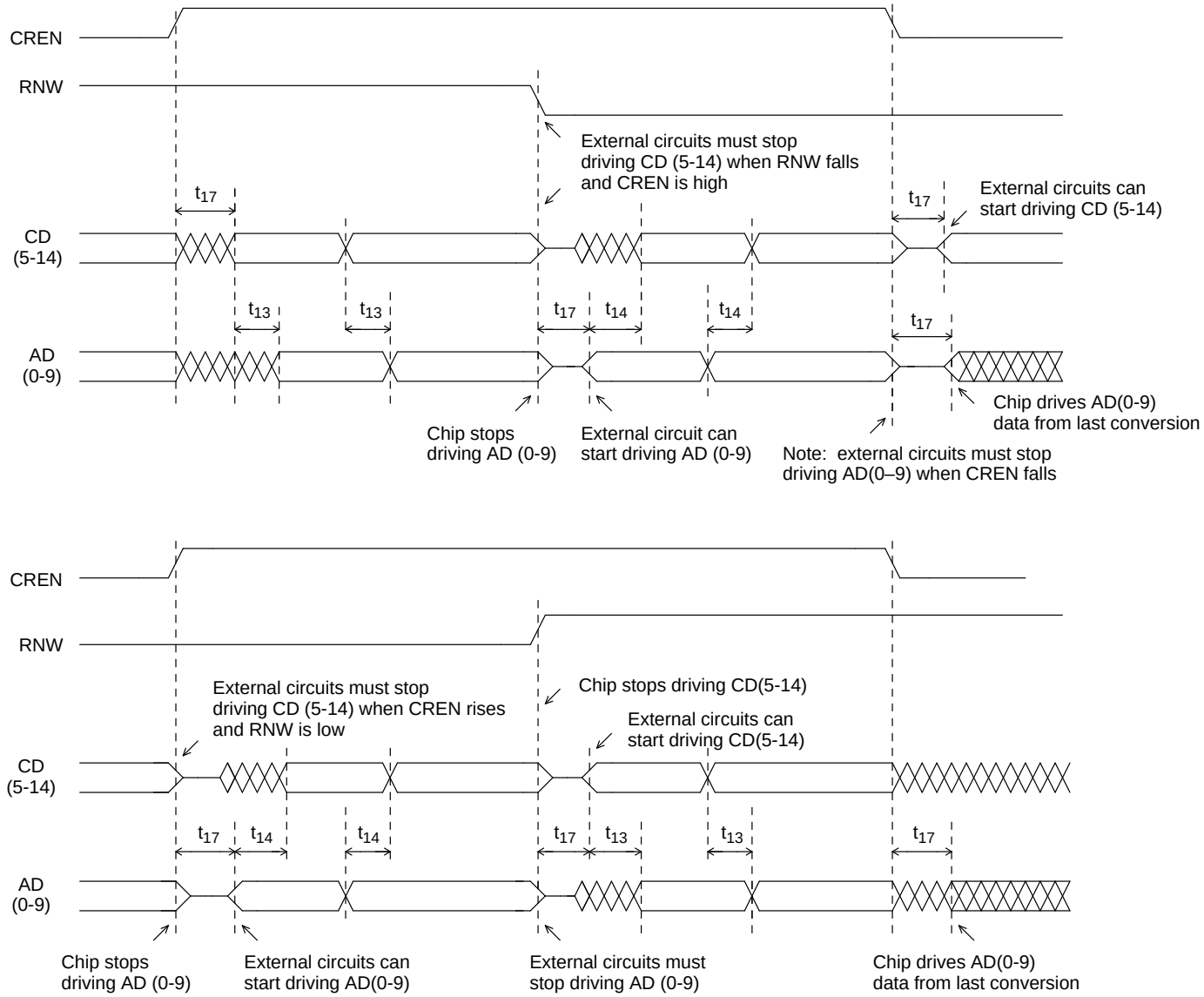


Figure 3. DAC Input and ADC Output Timing for Normal Convert Operation (CREN = 0)

Pass Through Mode

1. AENL, BENL & CENL should be held high during pass-through mode. ADCs and DACs will not work properly during pass-through.
2. Pass-through mode enable. When CREN is high, pass-through mode between the ADC and DAC ports is enabled. RNW controls the direction of pass-through operation.
3. READ not WRITE signal. RNW controls the direction of the pass-through operation when CREN is high, and has no impact when CREN is low. When RNW is high, data passes from the DAC port to the ADC port. When RNW is low, data passes from the ADC port to the DAC port. Note the port connections are: CD5; AD0; CD6; AD1;...;CD14; AD9.



T_{13} Pass through delay from CD(5-14) to AD(0-9)

T_{14} Pass through delay from AD(0-9) to CD(5-14)

T17 Pass through set up time

Figure 4. Timing for Pass Through Mode Operation

THEORY OF OPERATION

The MP8830 is composed of three ADC converters with dynamic gain and offset control along with their associated analog and digital support circuitry. The three converters are intended to be used in a simultaneous sampling configuration. The only external circuits required are a reference and reference buffer amp.

The ADC gain and offset DAC inputs, ADC output data, and the A_{IN} sampling time are related to the four clock inputs, CVL, AENL, BENL and CENL.

In applications which require rejecting a bias level from the analog input, a zero clamp is provided for each channel. With the addition of a buffer input amp and blocking capacitor, this function rejects the bias present during DCL = 0 time on the analog input.

ADC calibration or test can be performed using the built-in VCAL / A_{IN} MUX which will switch the ADC A_{IN} from the channel input voltage, AAN, BAN, CAN to VCAL.

A fast mode is provided, where only the four ADC MSBs are produced while the remaining data is set to 00(hex).

To simplify board layout, a data pass-through configuration is provided to allow bi-directional communication between the ADC data port and the 10 MSBs of the DAC I/O port.

ADC System Overall Sequence

The following section describes the events which take place during one conversion cycle (*Figures 1-4*). Assume at power up, or in the previous cycle, that the values for the gains and offsets needed for this sample set have been loaded into the first DAC registers. This data is loaded into the second registers for all three channels *on the rising edge of CVL*. A_{IN} tracking for all channels is also started after t_{AP} delay. Note that the AENL, BENL and CENL were at "1" states.

At the *falling edge of AENL*, the channel A gain and offset data for the next cycle is loaded into the channel A first DAC register. The analog input sample for all three channels is taken at the *rising edge of AENL* after t_{AP} delay.

At the *falling edge of BENL*, the channel B gain and offset data for the next cycle is loaded into the channel B first DAC register. The MSB comparators are also enabled at this time. At *the rising edge of BENL*, the MSB value is latched, and the range for the LSBs is selected. Note that the gain and offset DAC must be settled by this time in order for the MSB value to be correct (t_7 + t_4 + t_1 ensure this.)

At *the falling edge of CENL*, the channel C gain and offset data for the next cycle is loaded into the channel C first DAC register. The LSB comparators are also enabled at this time. At *the rising edge of CENL*, the LSB value is latched.

During the time (t_9) when CENL =1 and CVL = 0, the MSB data is corrected (if necessary) and then propagated along with the LSB data to the ADC outputs. On the rising edge of CVL, channel A data is enabled at the output port.

Since the actual ADC samples are taken at the rising edge of AENL after t_{AP} delay, this period of time is the most sensitive to transition noise from digital components. Keep all transitions outside of the t_{18}, t_{19} digital quiet time window around the AENL rising edge. Since the ADC output bus will change states at the rising edge of CVL, the time from CVL rising to AENL rising is important. The delay from CVL rising to channel A valid on the ADC bus is t_8. This requires that AENL rising edge must not occur until at least t_8 after CVL rising.

CVL Functions

CVL rising edge performs three functions. The first is to update the gain and offset DACs from their respective first registers simultaneously. The second function is to initiate the sample window. The third function is to latch the results of the previous conversions into the ADC output register.

The A channel ADC data is presented at the ADC data port after CVL rising edge. CVL falling edge does not change any internal state.

DAC Data Port Operation

DAC data is loaded first into an input register and then loaded into the DAC register.

The input register allows sequential loading of the next conversion settings for all the channels through the 15-bit DAC data bus while the ADC data is being clocked out of the ADC data port. The second register allows for simultaneous updating of all channels at the beginning of the analog sample period. This timing gives the ADC reference levels adequate time to settle before being used to convert the sampled A_{IN}. Note that the DAC data must be presented at each cycle, since there is no provision for holding DAC data after each cycle.

At power up, the DAC states should be set for the first sample's required gain and offset settings. This is accomplished by setting CVL = 1, and cycling each of the AENL, BENL, and CENL clocks from their 1 to 0 to 1 states sequentially with each channel's respective data present at the DAC data port.

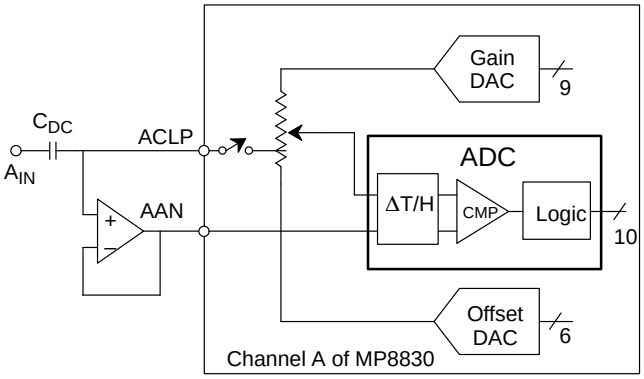


Figure 5. Simplified Diagram Channel A Example

Black Level Switch Operation

The MP8830 is equipped with a black level setting switch. The function of the black level setting switch is to store the DC offset value of the ADC as well as the common mode value of A_{IN} across the external C_{DC}-hold capacitor. This is a cost effective method to store the black level of A_{IN} or the offset of the system. Note that the ACLP, BCLP, and CCLP level is DC shifted to accommodate for the distribution of ADC offset.

One terminal of each clamp switch is connected at the ladder tap voltage which corresponds to +4 LSB from the ADC 000(hex) to 001(hex) transition. This 4 LSB offset allows the ADC to measure as low as –4 LSB of the analog input voltage relative to the clamp voltage. To increase the negative input detectable range, clamp with the offset DAC at a code higher than 00(hex).

The second terminal of the clamp switch is connected to a pin with its corresponding channel prefix. For channel A, the pin is named ACLP.

The control of the all the switches is provided by a separate unlatched logic input called DCL. The delay from DCL falling edge to switch on is specified as t_{16}. The actual time required to store the bias voltage depends on the external C value, and bias variation from sample to sample. The equivalent impedance of the clamp is 100Ω typical, spec name of R_{ON}, and must be included in the analysis of the zero sample time considerations.

The black level is a function of the offset DAC, and therefore requires that the value of the offset DAC be loaded into the offset DAC second register before the clamp is turned on. This value can be set from 00(hex) to 3F(hex) corresponding to a clamp level change of ZSR.

The voltage swing at the ACLP, BCLP, CCLP pin after clamp should be limited to the range of AV_{DD} to AGND. This will prevent the stored charge on the holding cap from being changed by the input protection devices.

A 50Ω to 100Ω resistor in series with the ACLP, BCLP, CCLP pin will limit the current induced in the protection and parasitic diodes due to over-voltages induced by the source. Limit this current with the use of external protection diodes.

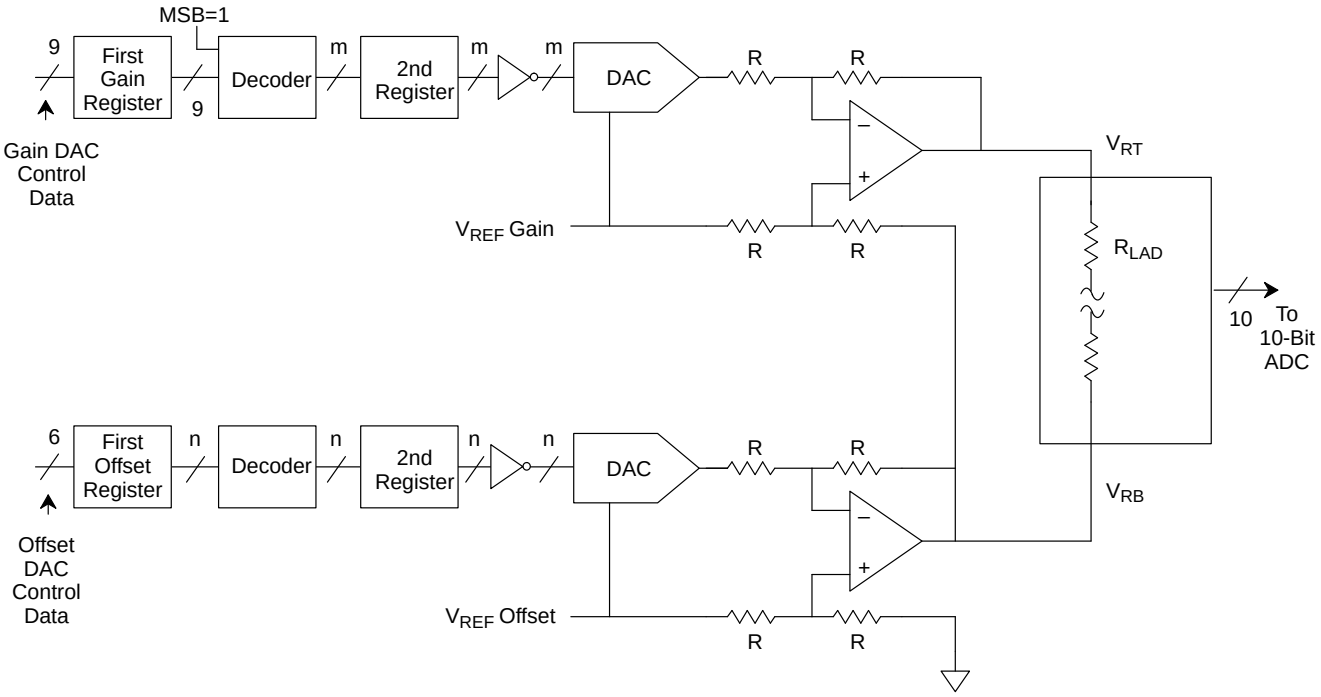


Figure 6. MP8830 Single-Channel Equivalent Circuit

ADC Gain and Offset Control

Each channel of the MP8830 contains a 10-bit ADC, a 10-bit DAC with MSB = 1 (9 active bits) driving the positive reference, and a 6-bit DAC driving the negative reference of the ADCs ladder network.

The relationship between the ADC gain and offset and the DAC data can be expressed mathematically.

Assign the terms V_{RT} and V_{RB} to represent the voltages for the ADC full scale and black levels. DgainA and DoffsetA represent the digital value for the gain and offset parameters set by the DACs for channel A.

V_{RT} and V_{RB} are defined by the equation:

$$V_{RT} = \left\{(1 + \frac{DgainA}{2^9}) * 1.3\right\} * V_{REF} + V_{RB}$$

$$V_{RB} = \left\{(1 + \frac{DoffsetA}{2^6}) * 0.16\right\} * V_{REF}$$

$$V_{RT} - V_{RB} = \left\{(1 + \frac{DgainA}{2^9}) * 1.3\right\} * V_{REF}$$

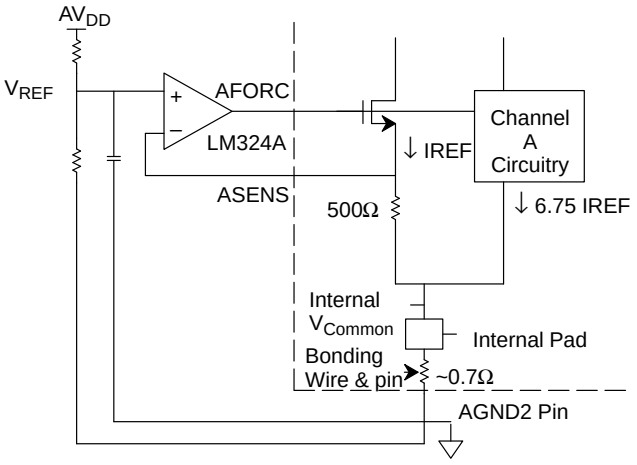


Figure 7. Driving the AFORC and ASENS Pins (Channel A Example)

Channel Bias Circuitry

The gain DAC and the offset DAC for each channel have a combined bias generator for setting their full scale range. An external op amp is required and is connected per *Figure 7.* The V_{REF} range for each channel can be either the same or different depending on the application and nominal channel gain required. A higher V_{REF} provides lower channel gain.

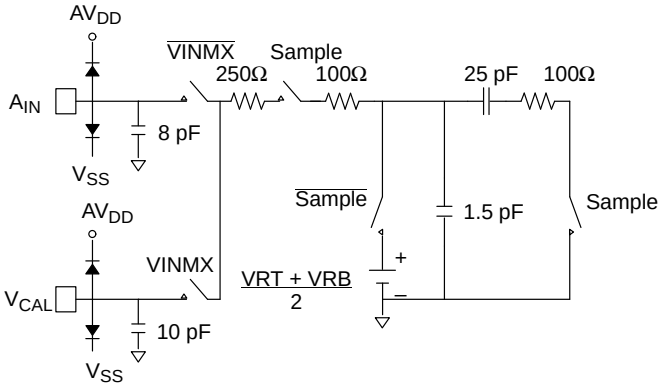


Figure 8. ADC Input Equivalent Circuit

ADC Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. *Figure 8.* shows an equivalent input circuit.

VCAL and VINMX

VCAL voltage is connected through an analog mux to all 3 channel inputs at VINMX=1. VCAL can then be used to normalize all three ADC input voltage to output states. It can be used for testing as well as building calibration tables for all three channels.

Supply and Grounds

AGND1, BGND1, CGND1, and GND3 should be connected under the package to make their common impedance as low as possible. AGND2, BGND2, CGND2 should also be connected to this ground.

Use a single supply to drive all of the V_{DD} pins. AV_{DD}, BV_{DD}, CV_{DD}, V_{DD3} should be connected to a common supply plane which forms a supply / ground plane with the analog ground plane. In addition, local decoupling (preferably 0.1 uFchip type) should be connected between each analog V_{DD} pin and its closest analog ground.

A decoupling capacitor (preferably 0.1 uFchip type) should be connected across pin 1 and 64 and between pin 44 and 43. A DV_{DD} to DGND supply/ground plane should also be provided.

PIN OUT DEFINITIONS

Pin #	Pin Name	Function
1, 44	DV_{DD}(2)	Digital positive power supplies. 5 V. Should be decoupled to digital GND plane. The two DV_{DD} pins both connect to the ESD ring as well as the control logic, data port logic, and the internal ADC output data bus drivers.
43, 64	DGND (2)	Digital negative power supplies. 0 V. The two DGND pins both connect to the ESD ring as well as the control logic and data port logic.
31 24 17 47	AV_{DD}, BV_{DD}, CV_{DD}, V_{DD3}	Analog positive power supplies. 5 V. Should be star connected to the analog supply post or direct connection to analog supply plane. Decouple to AGND, BGND, CGND. $V_{DD}3$ powers the ADC internal logic only.
36 30 23 46	AGND1, BGND1, CGND1, GND3	Analog negative power supplies. 0 V. Should be star connected to analog ground post or direct connection to the analog ground plane. These GNDs power the analog sections of the ADC and the circuitry in the DACs. GND3 pin connects to the internal ADC data bus and the ADC internal logic.
32 28 21	AGND2, BGND2, CGND2	Analog grounds related to DAC bias are the common voltage for the reference. The ADC ladder resistor terminates to this pin as well as the internal bias resistor used for setting the DAC reference. These pins should be used as the reference ground voltage for all analog measurements.
52	AENL	Channel A data clock, active low. A DAC data loaded into first register bank on the falling edge of AENL.
51	BENL	Channel B data clock, active low. B DAC data loaded into the first register on the falling edge of BENL. B ADC data loaded to the ADC output port on falling edge (and should be read on the rising edge).
50	CENL	Channel C data clock, active low. C DAC data loaded into the first register on the falling edge of CENL. C ADC data loaded to the ADC output port on falling edge (and should be read on the rising edge).
53	CVL	Cycle clock. All DACs loaded on rising edge. Begin sample of analog input on rising edge. A ADC data is loaded to the ADC output port on the rising edge of CVL (and should be read on the rising edge of AENL).
48	CREN	Pass through mode enable. When CREN is high, passthrough mode between the ADC and DAC ports is enabled. RNW controls the direction of pass through operation.
49	RNW	READ not WRITE signal. RNW controls the direction of the pass through operation when CREN is high and has no impact when CREN is low. When RNW is high data passes from the DAC port to the ADC port. When RNW is low, data passes from the ADC port to the DAC port. Note, the port connections are: CD5; AD0; CD6; AD1;.....;CD14; AD9.
39	V_{IN}MX	Analog mux control. V_{IN}MX controls the analog mux on the input of all three ADCs. When V_{IN}MX is high, all ADC inputs are connected to VCAL. When low, each ADC is connected to its particular analog input pin.
45	FAST	Fast mode enable. The FAST pin controls the mode of the ADCs. When low, the part functions as specified for 10-bit resolution. When high, the ADC's resolution becomes 4-bit and the LSBs are forced low. The clock rate can be increased in this mode to 3 MHz.
37	ACLP	Clamp voltage A. Black level clamp pin for the A channel.
29	BCLP	Clamp voltage B. Black level clamp pin for the B channel.
22	CCLP	Clamp voltage C. Black level clamp pin for the C channel.
41	DCL	Black level clamp control (active low). Black level clamp enable for all pins. All Black level clamps are turned on when DCL is low.
35	AAN	A channel analog input.
27	BAN	B channel analog input.
20	CAN	C channel analog input.
38	VCAL	Calibration input voltage.

34	AFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the A channel.
33	ASENS	Sensing voltage for biasing the internal DACs. This is the source of the N-channel biasing transistor and the top terminal of the internal biasing resistor for the A channel.
26	BFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the B channel.
25	BSENS	Sensing voltage for biasing the internal DACs. This is the source of the N-Channel biasing transistor and the top terminal of the internal biasing resistor for the B channel.
19	CFORC	Forcing voltage for biasing the internal DACs. This is the gate of the N-Channel biasing transistor for the C channel.
18	CSENS	Sensing voltage for biasing the internal DACs. This is the source of the N-Channel biasing transistor and the top terminal of the internal biasing resistor for the C channel.
54-63	AD9-AD0	ADC data output pins. AD9 is the MSB.
2-16	CD14-CD0	DAC input pins. CD14-CD6 are the Gain DAC MSB to LSB. CD5-CD0 are the offset DAC MSB to LSB.
42	N/C	No connection.
40	DGND	Digital Ground.

Note: All digital signals are active high unless otherwise noted.

APPLICATION NOTES FOR CCD SYSTEMS

A typical CCD digitizing configuration is shown in *Figure 9.*, which incorporates global gain and offset adjustment as well as pixel-to-pixel variation correction. The MP8830 can greatly simplify this type of system by replacing the ADCs, the pixel correction DACs, and the global offset DACs as shown in *Figure 10.* One main advantage of the MP8830 is the way the offset and span for each pixel are controlled. In the traditional application, the offset and span settings interact requiring addtional computations for each pixel adjustment. With the MP8830, the offset and span settings can be calibrated separately simplifying the computations necessary.

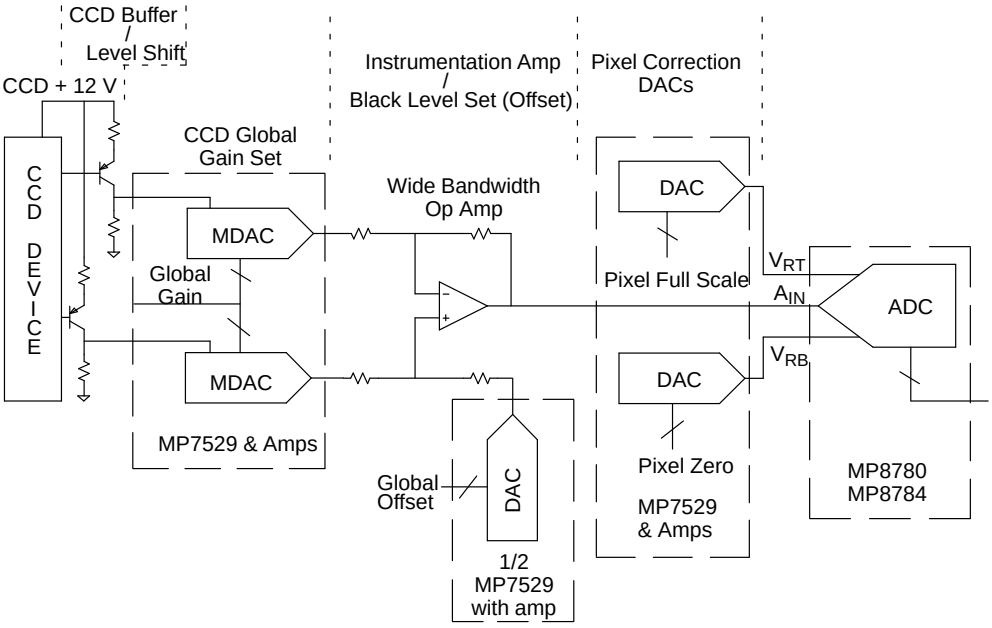


Figure 9. Common Configuration for CCD Digitizer 1 Channel Shown

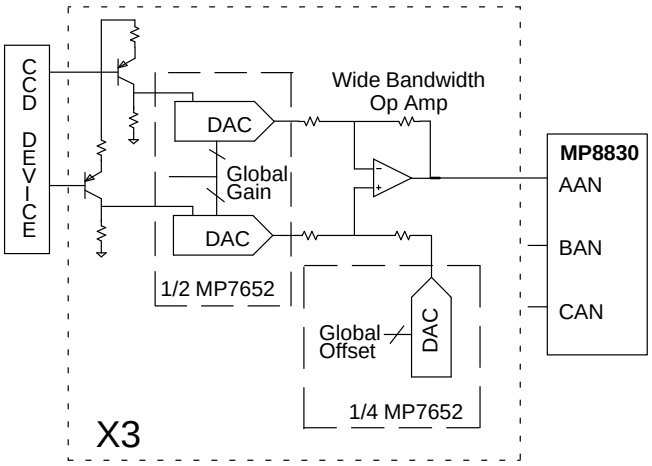


Figure 10. Common Configuration for CCD Digitizer with MP8830 1 Channel Shown

The configuration shown in *Figure 10.* incorporates all of the building blocks present in previous generations. As shown, the MP7652 allows for a serial data path for the global adjustment DACs. The MP7643 allows for a parallel data path. The clamp function would not normally be used in this configuration.

As shown in *Figure 11.,* by using the clamp pin, the global offset (black level) can be AC coupled to the ADC in order to simplify the offset calibration and eliminate thermal and power supply induced errors.

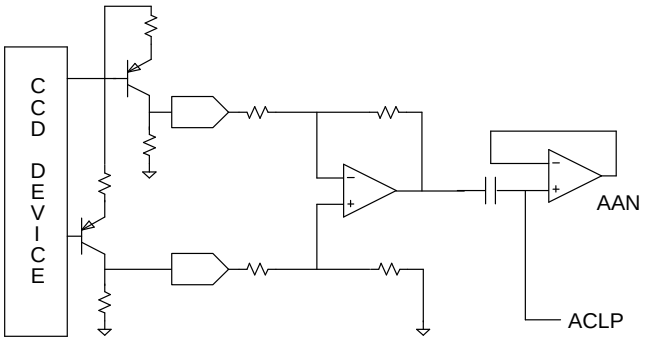


Figure 11. Configuration for CCD Digitizer using Black Level Clamp Channel A Shown

The amount of adjustment range available with the standard configuration may allow for the use of only one V_{REF} buffer amp by connecting the A, B, CFRC pins together on the MP8830 and using the ASENS pin as the feedback point to the buffer. BSENS and CSENS are open in this case. See *Figure 12.*

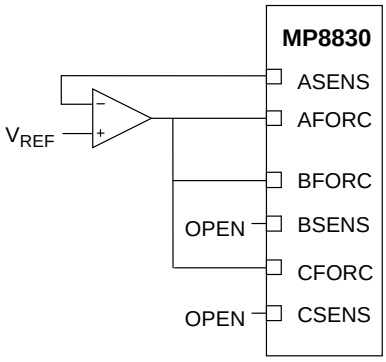


Figure 12. Simplified Reference Buffer Amp Configuration

Additional gain adjustment is possible by varying the channel V_{REF} voltage during calibration. *Figure 13.* shows a general drawing for this approach. By using the MP7643, the buffer amplifiers can be eliminated as shown in *Figure 14.*

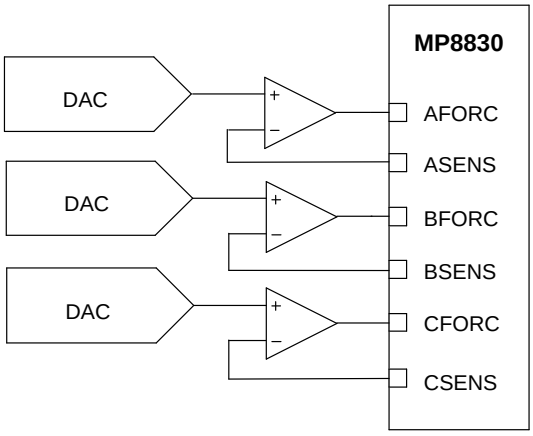


Figure 13. 3/8 of MP7670

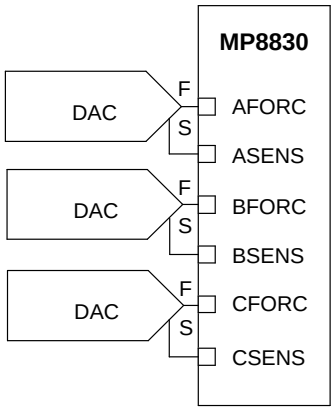
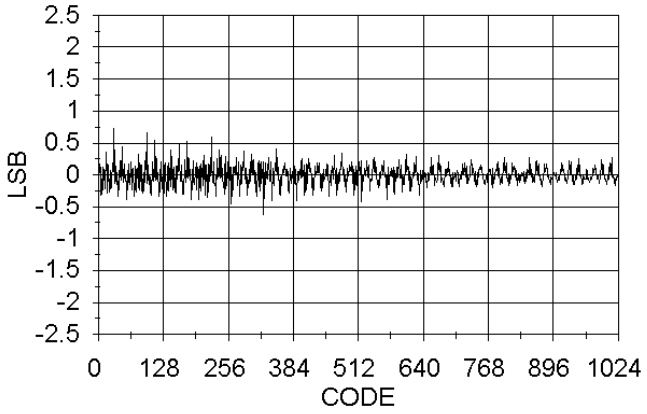
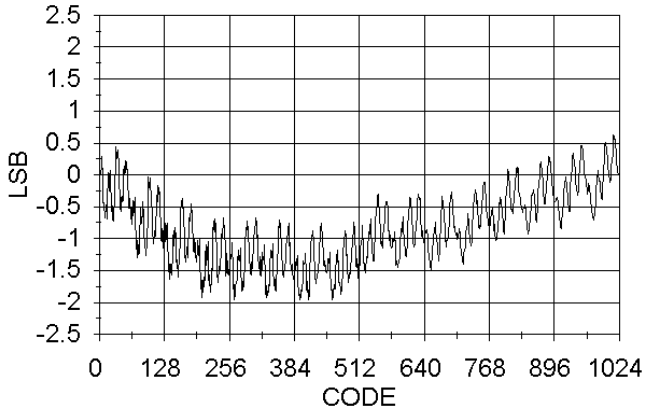


Figure 14. 3/4 of MP7643

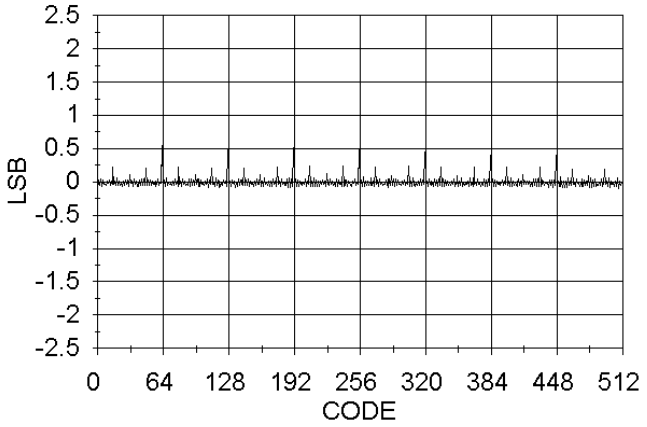
PERFORMANCE CHARACTERISTICS



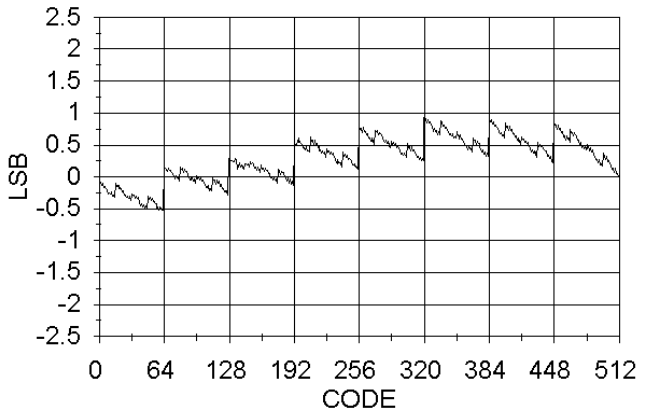
Graph 1. ADC DNL Error Plot
Channel A



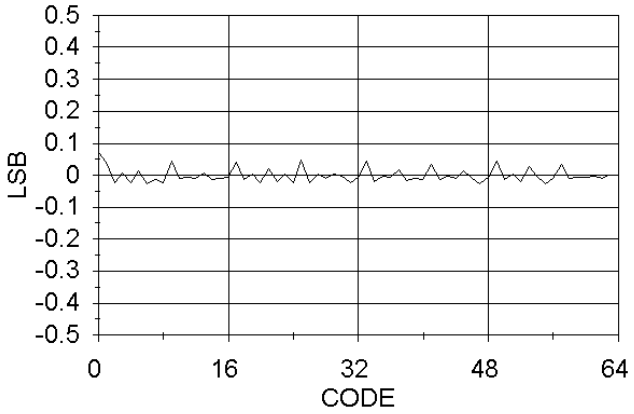
Graph 2. ADC INL Error Plot
Channel A



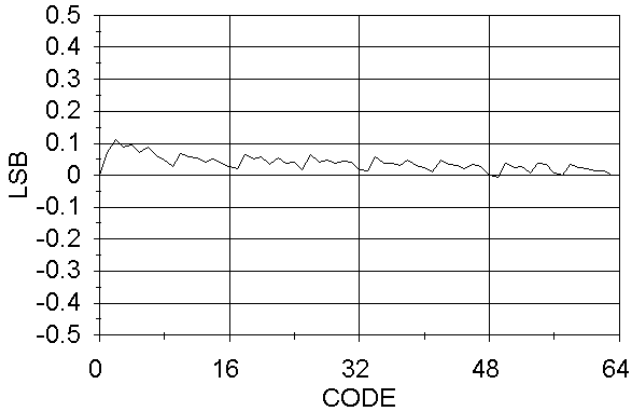
Graph 3. Gain DAC DNL Error Plot
Channel A



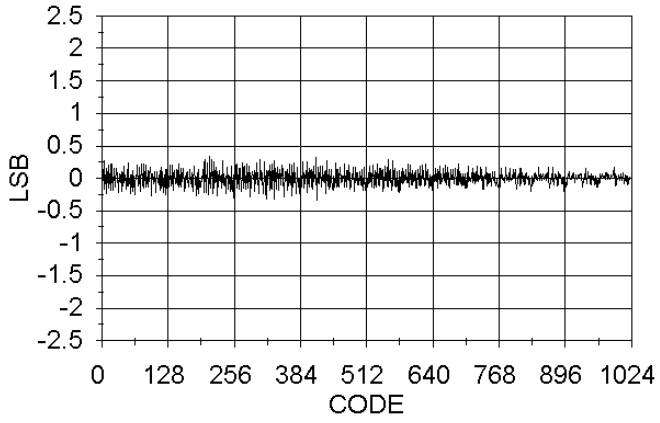
Graph 4. Gain DAC INL Error Plot
Channel A



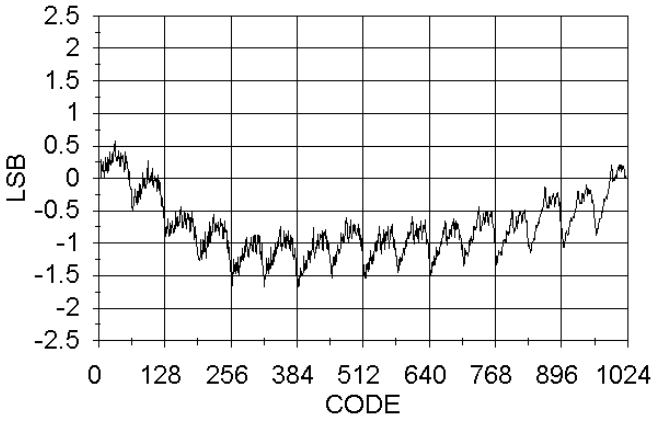
Graph 5. Offset DAC DNL Error Plot
Channel A



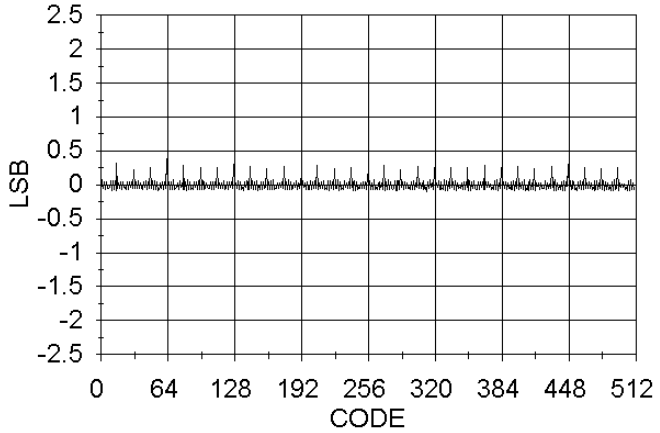
Graph 6. Offset DAC INL Error Plot
Channel A



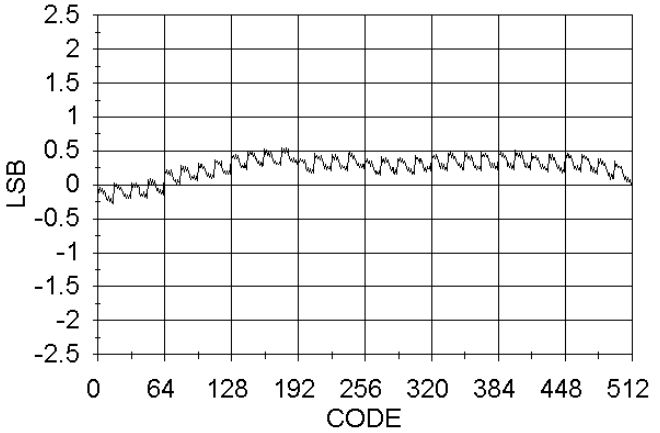
Graph 7. ADC DNL Error Plot
Channel B



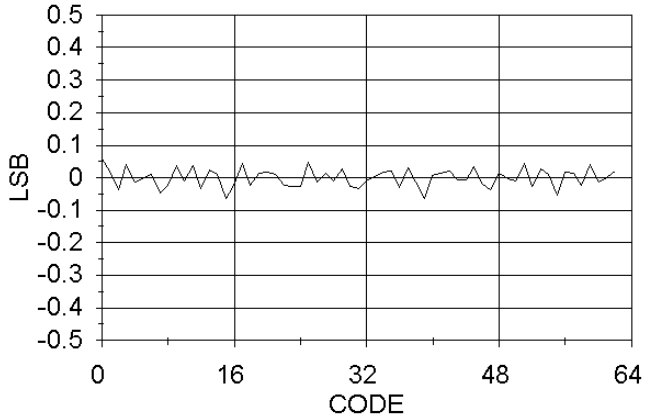
Graph 8. ADC INL Error Plot
Channel B



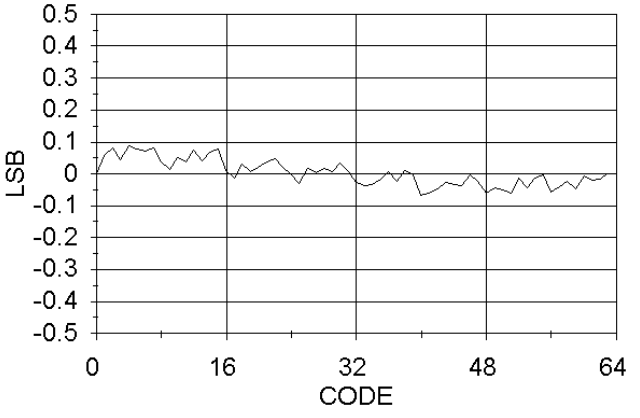
Graph 9. Gain DAC DNL Error Plot
Channel B



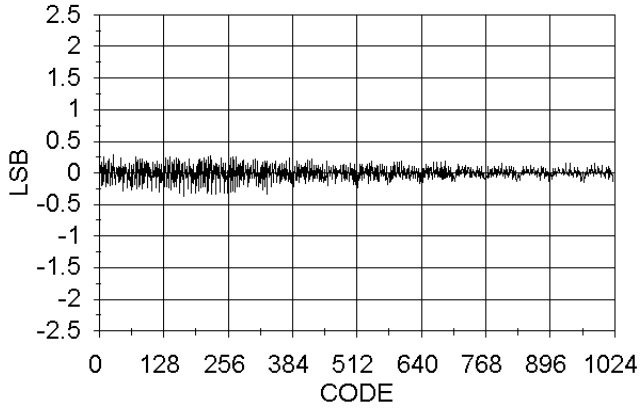
Graph 10. Gain DAC INL Error Plot
Channel B



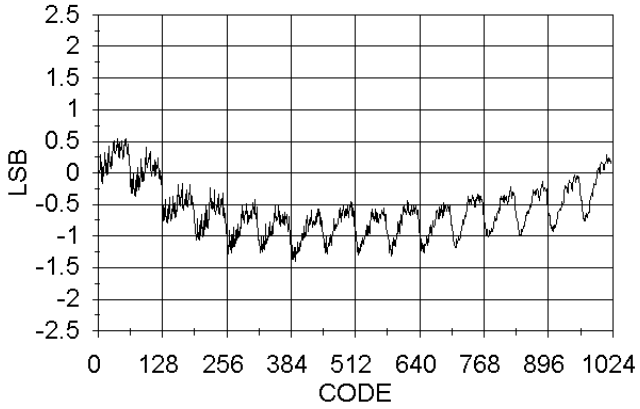
Graph 11. Offset DAC DNL Error Plot
Channel B



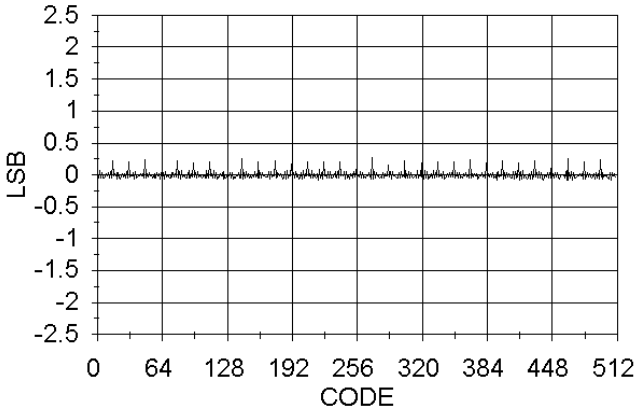
Graph 12. Offset DAC INL Error Plot
Channel B



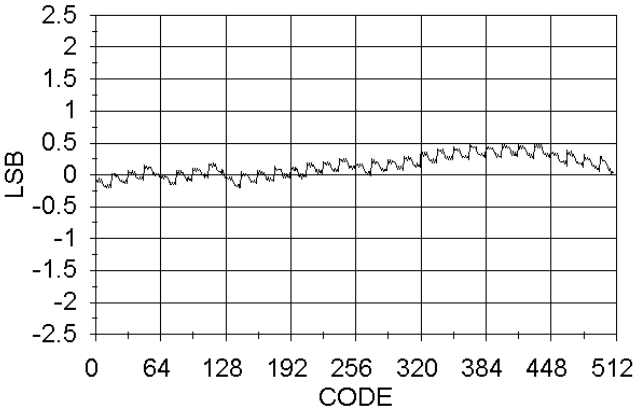
Graph 13. ADC DNL Error Plot
Channel C



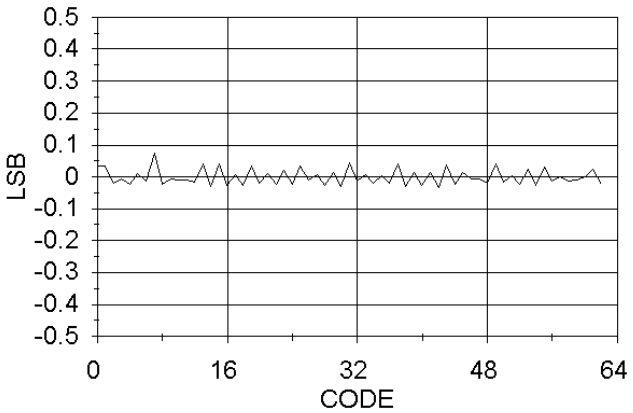
Graph 14. ADC INL Error Plot
Channel C



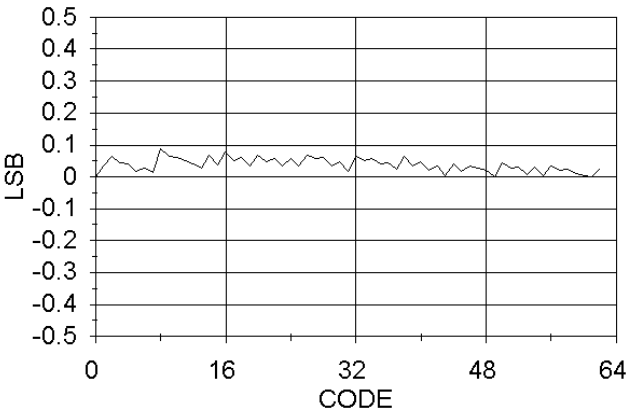
Graph 15. Gain DAC DNL Error Plot
Channel C



Graph 16. Gain DAC INL Error Plot
Channel C

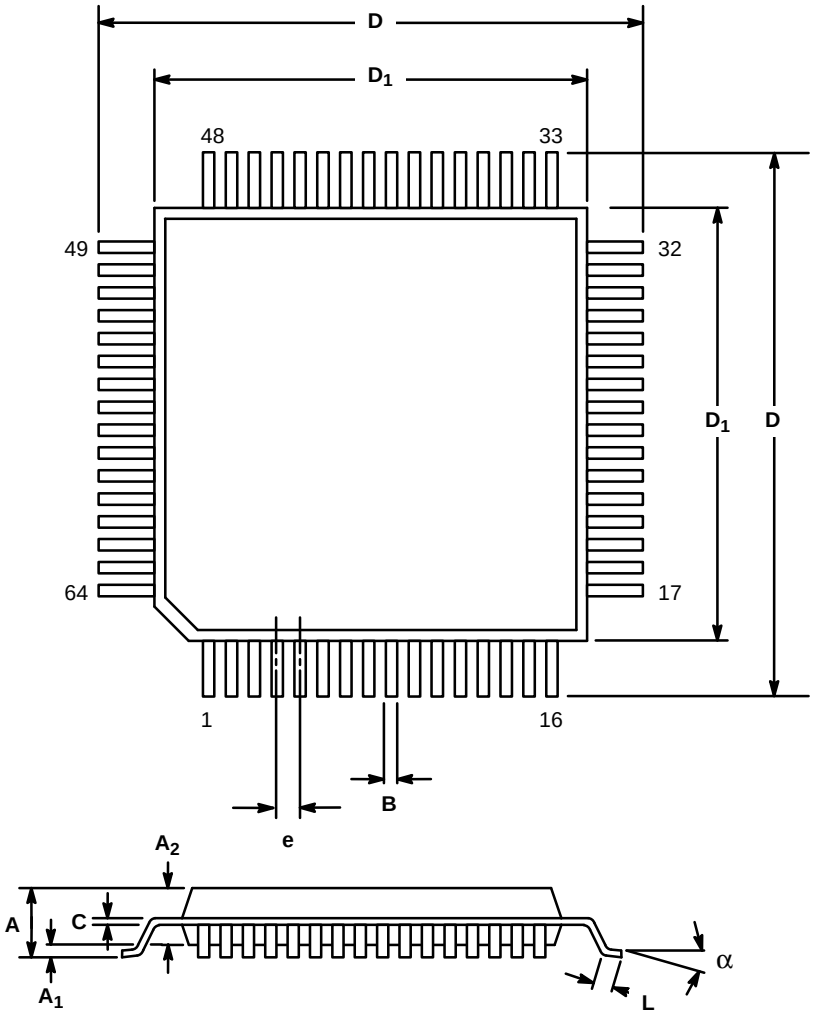


Graph 17. Offset DAC DNL Error Plot
Channel C



Graph 18. Offset DAC INL Error Plot
Channel C

64 LEAD PLASTIC QUAD FLAT PACK
(14mm x 14mm PQFP, METRIC)
Q64



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	3.15	—	0.124
A_1	0.25	—	0.01	—
A_2	2.6	2.8	0.102	0.110
B	0.3	0.4	0.012	0.016
C	0.13	0.23	0.005	0.009
D	16.95	17.45	0.667	0.687
D_1	13.9	14.1	0.547	0.555
e	0.80 BSC		0.0315 BSC	
L	0.65	1.03	0.026	0.040
α	0°	7°	0°	7°
Coplanarity = 4 mil max.				

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