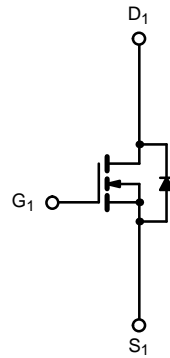
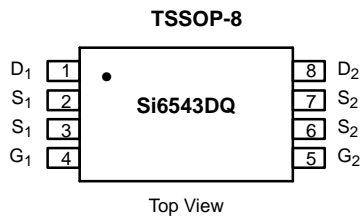


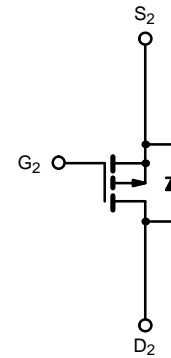


## Dual N- and P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
N-Channel	30	0.065 @ V <sub>GS</sub> = 10 V	±3.9
		0.095 @ V <sub>GS</sub> = 4.5 V	±3.1
P-Channel	-30	0.085 @ V <sub>GS</sub> = -10 V	±2.5
		0.19 @ V <sub>GS</sub> = -4.5 V	±1.8



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V <sub>DS</sub>	30	-30	V
Gate-Source Voltage		V <sub>GS</sub>	±20	±20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	T <sub>A</sub> = 25°C	I <sub>D</sub>	±3.9	±2.5	A
	T <sub>A</sub> = 70°C		±3.1	±2.1	
Pulsed Drain Current		I <sub>DM</sub>	±20	±20	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	1.25	-1.25	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.0		W
	T <sub>A</sub> = 70°C		0.64		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	125	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1.0		V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V	N-Ch		±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	N-Ch		1	μA	
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V	P-Ch		-1		
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch		25		
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch		-25		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	N-Ch	15		A	
		V <sub>DS</sub> ≥ -5 V, V <sub>GS</sub> = -10 V	P-Ch	-15			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.9 A	N-Ch		0.043	0.065	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = 2.5 A	P-Ch		0.066	0.085	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.1 A	N-Ch		0.075	0.095	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = 1.8 A	P-Ch		0.125	0.19	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.9 A	N-Ch		7	S	
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.5 A	P-Ch		5		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.25 A, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V
		I <sub>S</sub> = -1.25 A, V <sub>GS</sub> = 0 V	P-Ch		0.8	-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.9 A P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.5 A	N-Ch		9.8	15	nC
Gate-Source Charge	Q <sub>gs</sub>		P-Ch		8.7	15	
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		2.1		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	N-Ch		9	15	ns
			P-Ch		7	15	
Rise Time	t <sub>r</sub>		N-Ch		6	18	
			P-Ch		9	18	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		18	27	
			P-Ch		14	27	
Fall Time	t <sub>f</sub>		N-Ch		6	15	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.25 A, di/dt = 100 A/μs	N-Ch		48	80	
		I <sub>F</sub> = -1.25 A, di/dt = 100 A/μs	P-Ch		46	80	

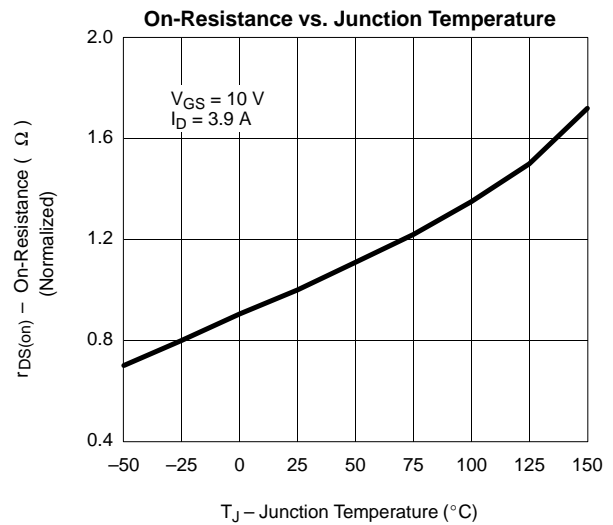
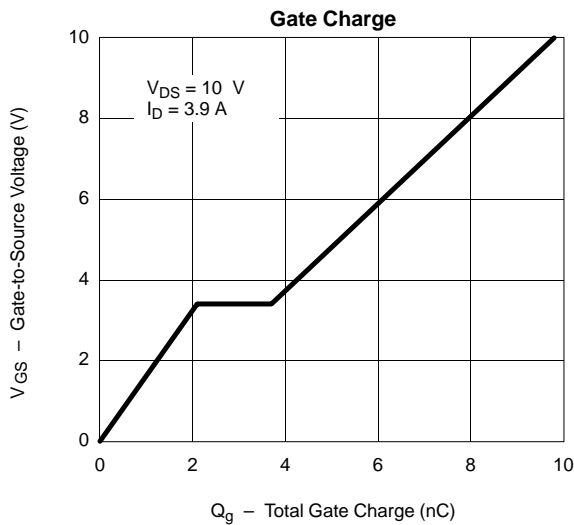
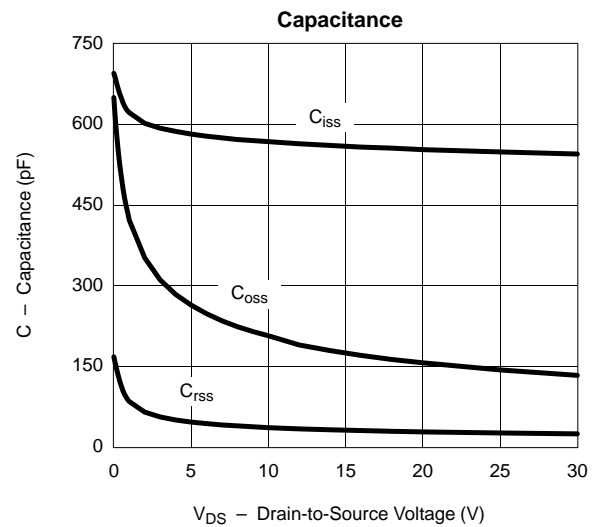
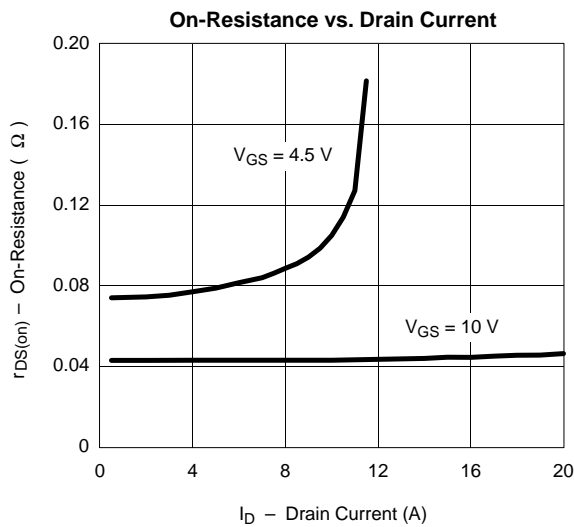
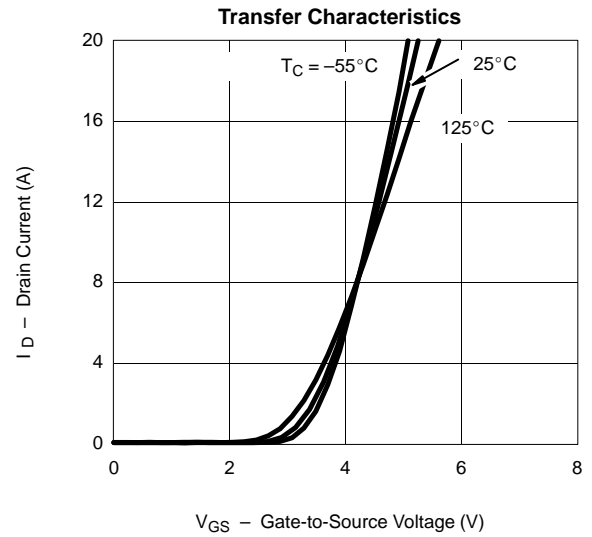
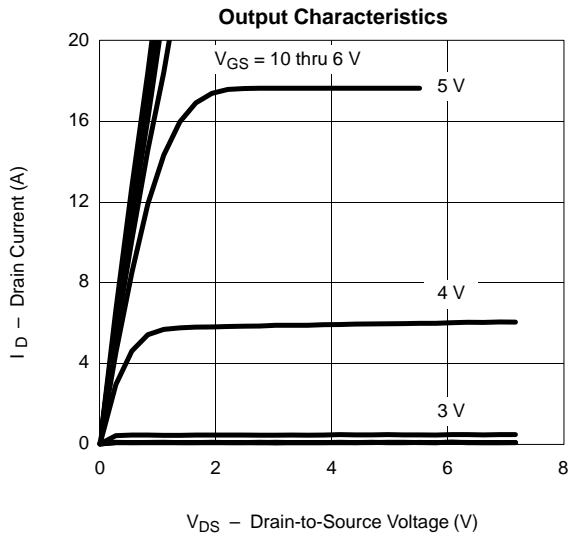
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

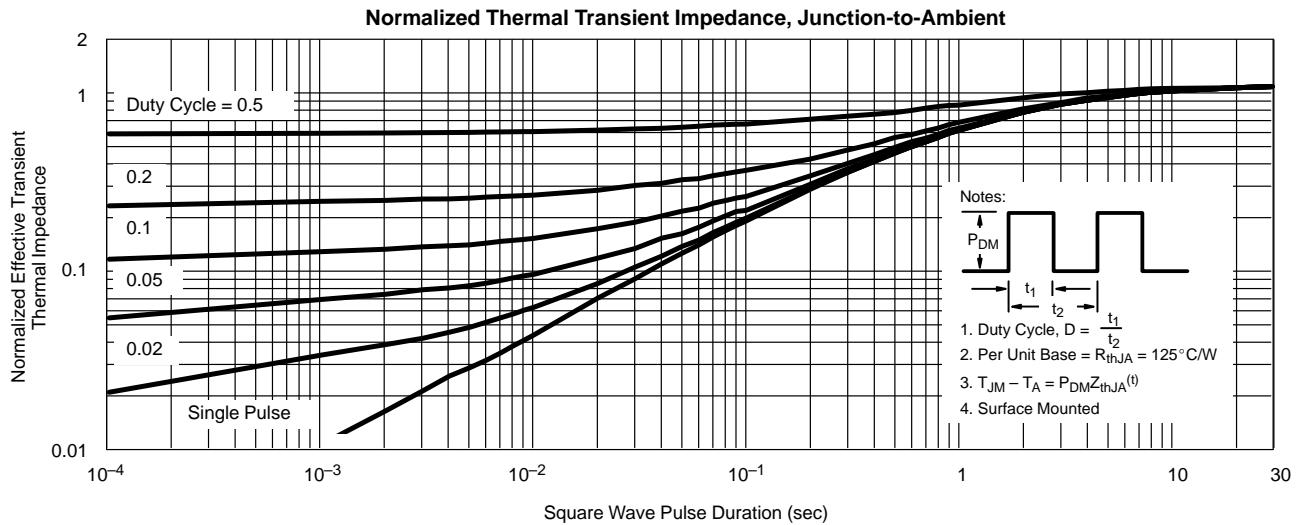
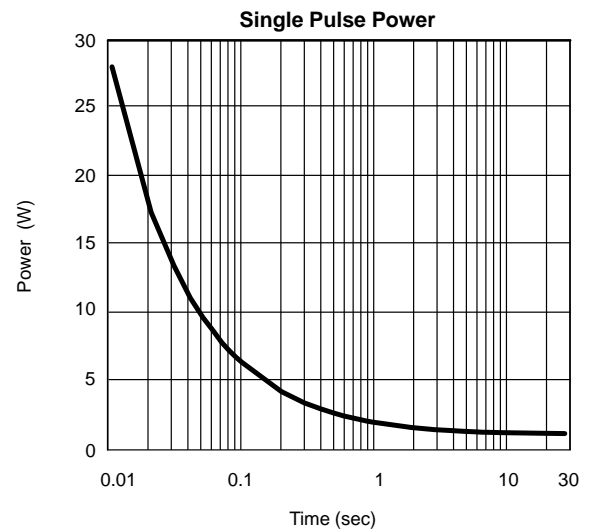
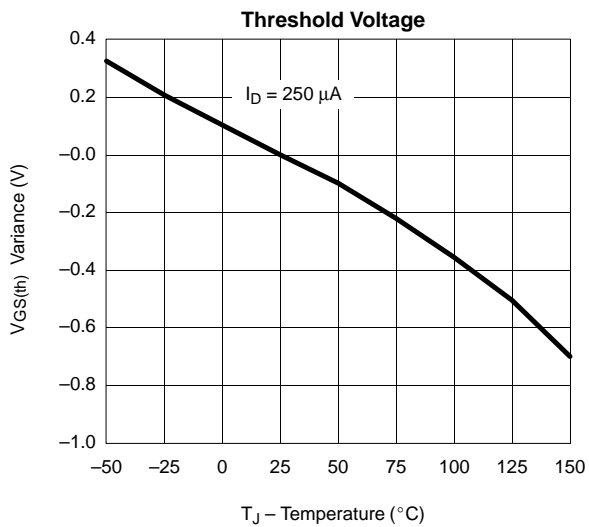
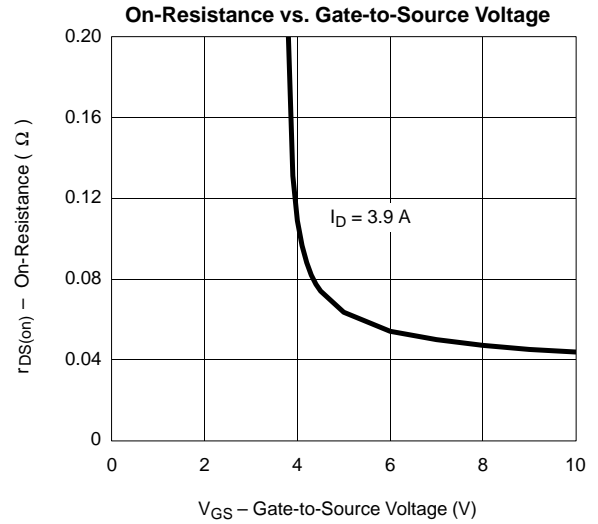
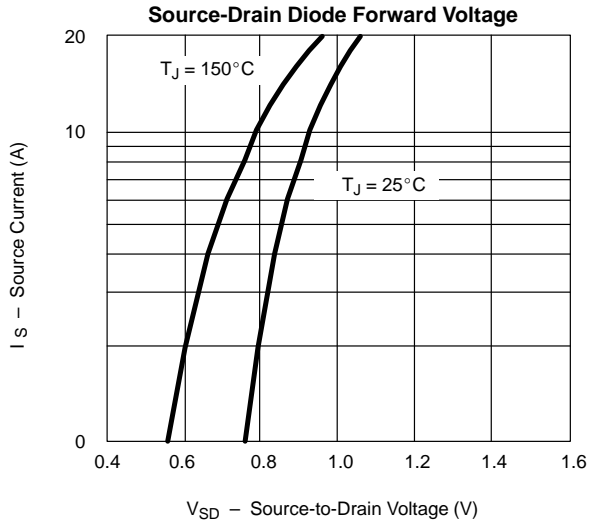


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



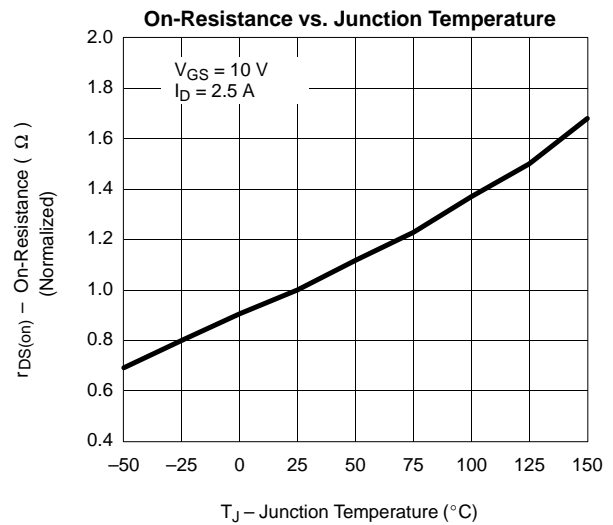
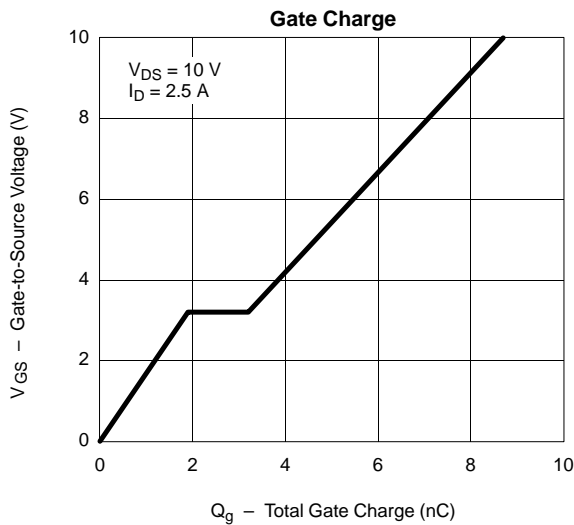
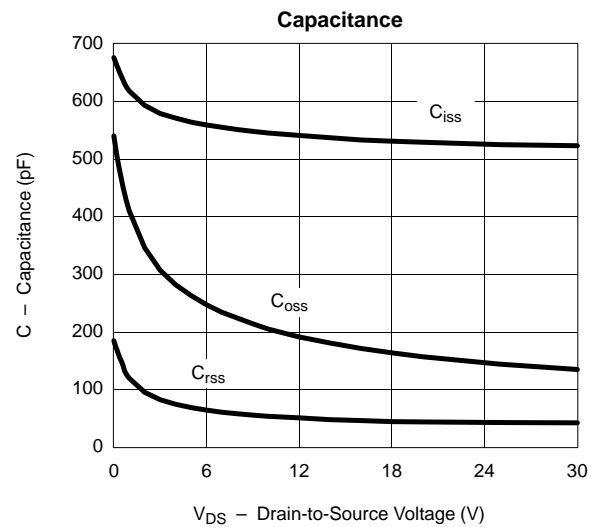
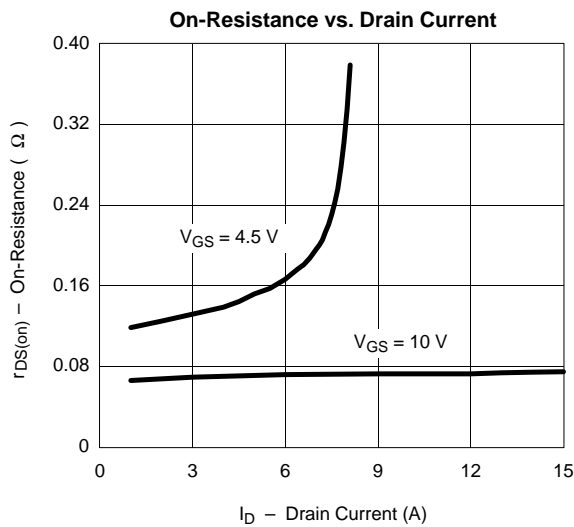
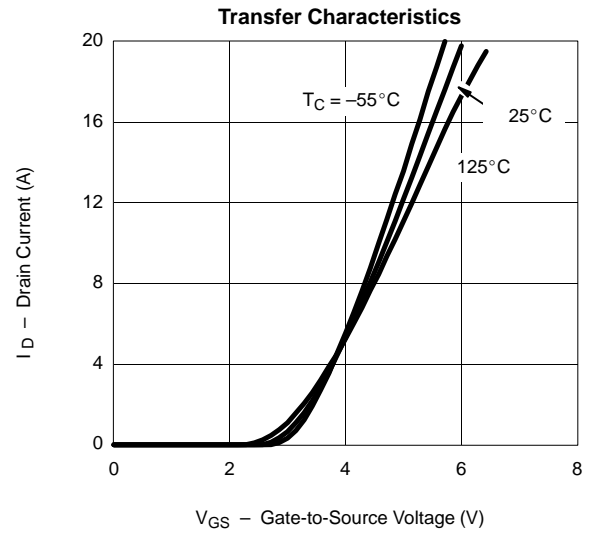
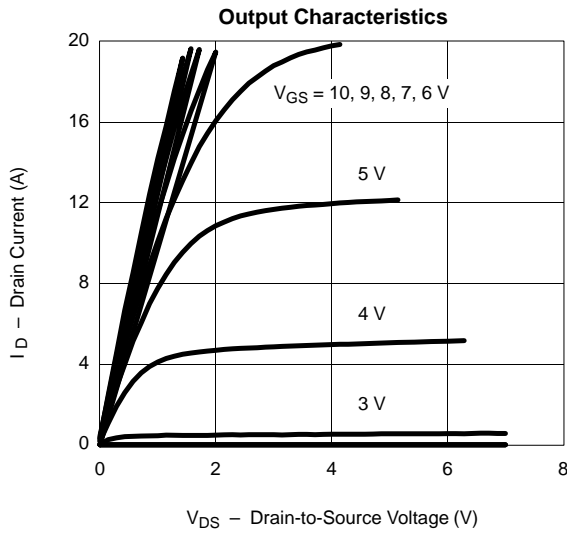
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL**





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL**

