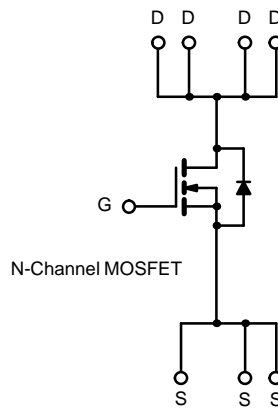
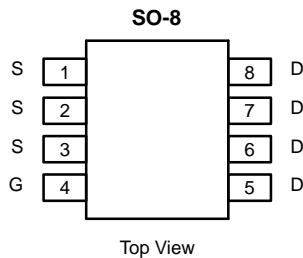




N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0075 @ $V_{GS} = 10$ V	15
	0.010 @ $V_{GS} = 4.5$ V	13

TrenchFET[®]
Power MOSFETs
High-Efficiency
PWM Optimized



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	15	11.0	A
	$T_A = 70^\circ\text{C}$		13	9.0	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	50		
Continuous Source Current (Diode Conduction) ^a		I_S	2.7	1.40	W
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.10	1.56	
	$T_A = 70^\circ\text{C}$		2	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	33	40	$^\circ\text{C/W}$
	Steady State		68	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	16	21	

Notes
a. Surface Mounted on FR4 Board.



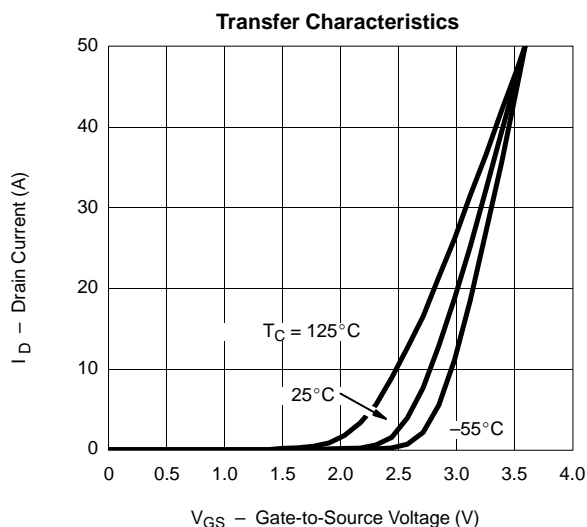
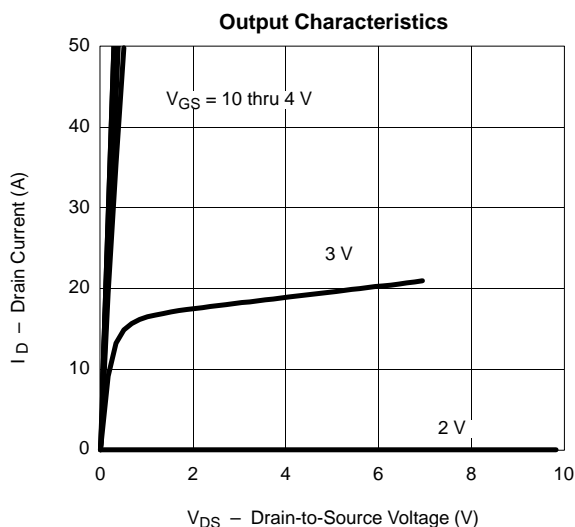
MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$		0.0062	0.0075	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 13 \text{ A}$		0.0083	0.010	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 15 \text{ A}$		42		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.73	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 5.0 \text{ V}, I_D = 15 \text{ A}$		27	35	nC
Gate-Source Charge	Q_{gs}			10.2		
Gate-Drain Charge	Q_{gd}			11.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		16	25	ns
Rise Time	t_r			9	20	
Turn-Off Delay Time	$t_{d(off)}$			60	100	
Fall Time	t_f			37	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	80	

Notes

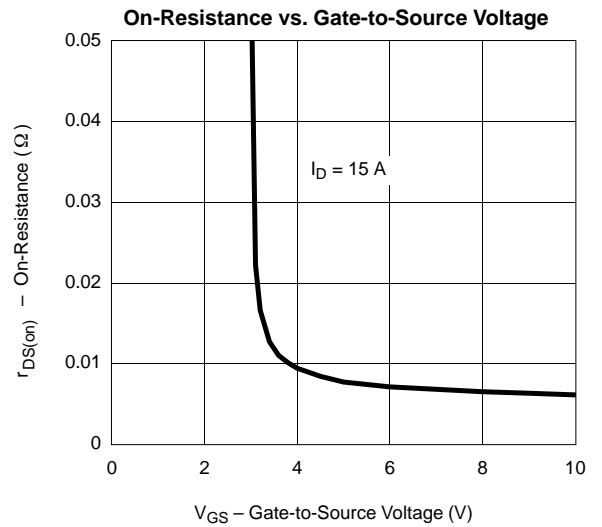
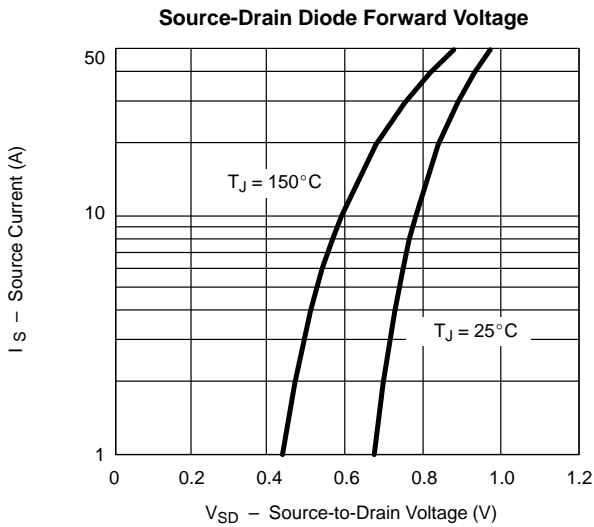
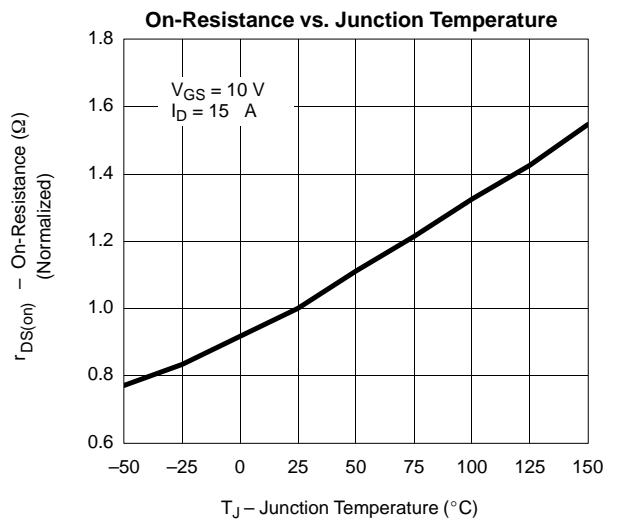
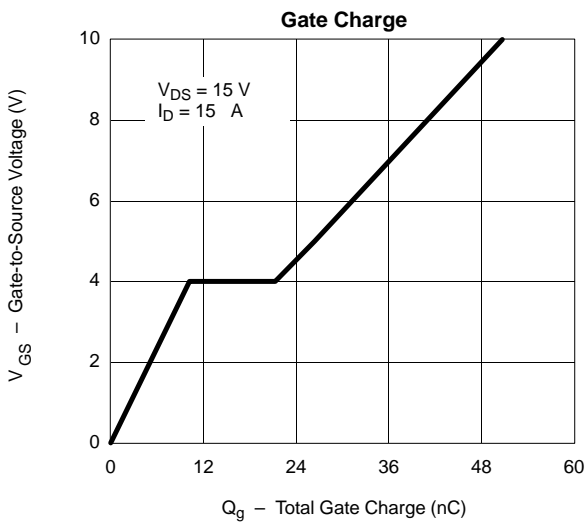
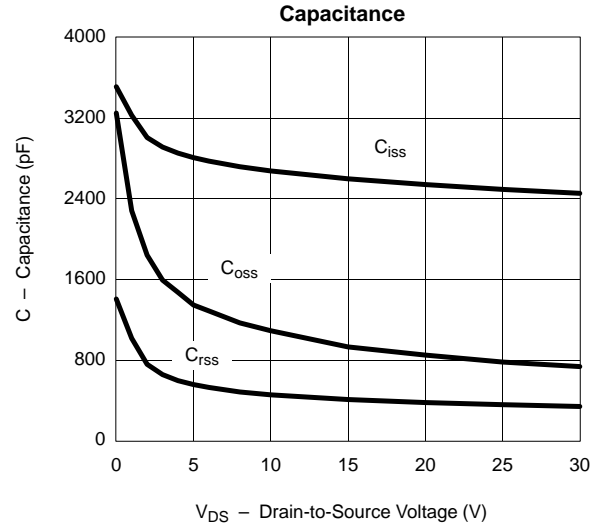
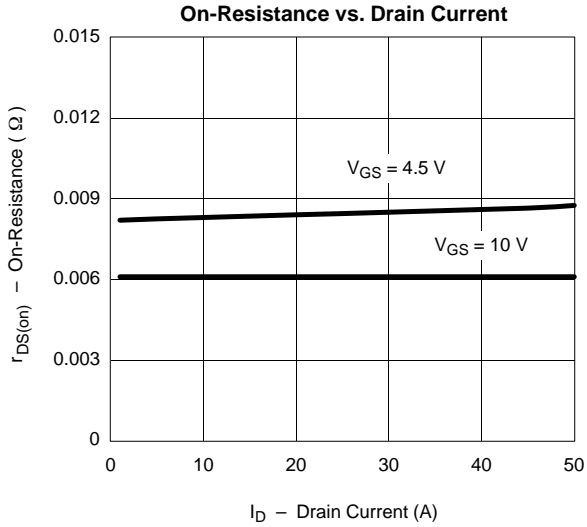
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

