SONY

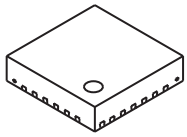
CXG1166ER

High Power 3 × 5 Antenna Switch MMIC with Integrated Control Logic

Description

The CXG1166ER is a high power antenna switch MMIC for PDC handsets. There are two modes which are TDMA mode and Packet mode. The CXG1166ER is suited to connect Tx/Rx/Duplexer to one of 4 antennas. This switch has on-chip logic circuit for operation with 4 CMOS inputs. The Sony Junction-gate PHEMT (JPHEMT) process is used for low insertion loss and low voltage operation.

24 pin VQFN (Plastic)



Features

- Low insertion loss: 0.7dB @1.44GHz
- Low loss bypass mode in TDMA
- High linearity: Harmonic < – 60dBc
- CMOS compatible input control
- Small package: 24-pin VQFN (3.3mm × 3.3mm)

Applications

3 × 5 antenna switch for digital cellular such as PDC handsets

Structure

GaAs Junction-gate PHEMT

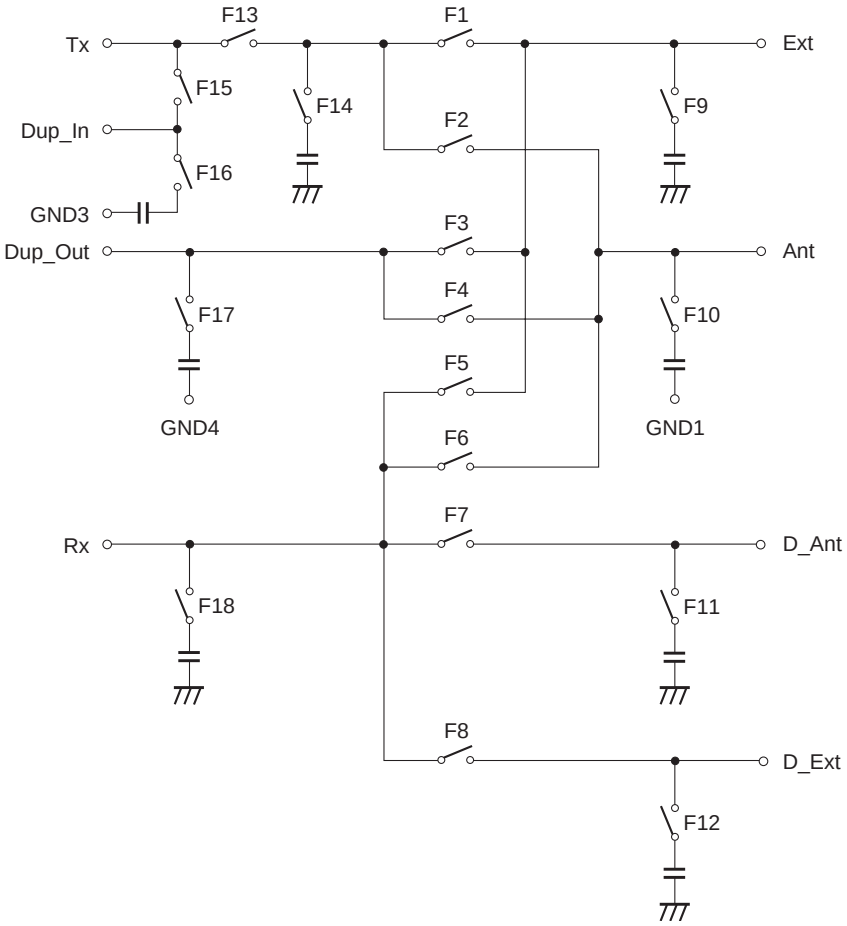
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

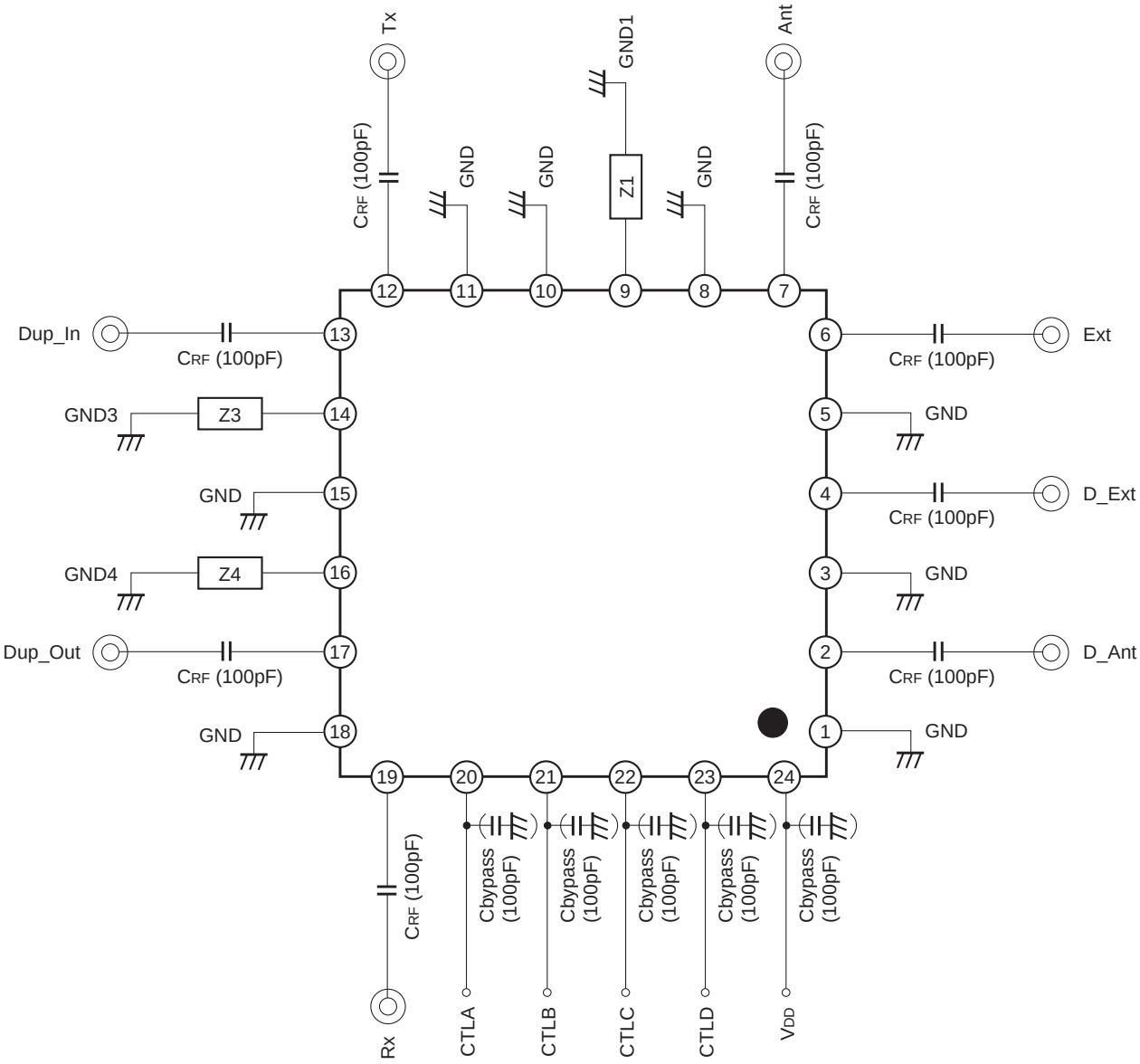
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04503-PS

Block Diagram



Pin Configuration/Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF decoupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

A: Rx/Tx
B: Main/diversity
C: External/antenna
D: TDMA/28.8k

State	On Pass	A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18
1	Tx – Ext	H	—	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H
2	Tx – Ant	H	—	H	L	L	H	L	L	L	L	L	L	H	L	H	H	H	L	L	H	H	H
3	Rx – Ext	L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	L	H	L	H	H	L
4	Rx – Ant	L	L	H	L	L	L	L	L	L	H	L	L	H	L	H	H	L	H	L	H	H	L
5	Rx – D_Ext	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	L	L	H	L	H	H	L
6	Rx – D_Ant	L	H	H	L	L	L	L	L	L	L	H	L	H	H	L	H	L	H	L	H	H	L
7	Dup_Out – Ant Rx – Ant	—	L	H	H	L	L	L	H	L	H	L	L	H	L	H	H	L	H	H	L	L	L
8	Dup_Out – Ant Rx – D_Ant	—	H	H	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H	H	L	L	L
9	Dup_Out – Ext Rx – Ext	—	L	L	H	L	L	H	L	H	L	L	L	L	H	H	H	L	H	H	L	L	L
10	Dup_Out – Ext Rx – D_Ext	—	H	L	H	L	L	H	L	L	L	L	H	L	H	H	L	L	H	H	L	L	L

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.7	3.0	3.5	V
Vctl (H)	2.2	3.0	3.5	V
Vctl (L)	0		0.4	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx – Ext	*1	—	0.75	1.0	dB
		Tx – Ant	*1	—	0.7	0.95	dB
		Tx – Dup_In	*1	—	0.25	0.5	dB
		Rx – Ext	*2	—	0.65	0.9	dB
		Rx – Ant	*2	—	0.65	0.9	dB
		Rx – D_Ext	*2	—	0.45	0.7	dB
		Rx – D_Ant	*2	—	0.45	0.7	dB
		Dup_Out – Ext	*1, *4	—	0.75	1.0	dB
		Rx – Ext	*2, *5	—	0.8	1.05	dB
		Dup_Out – Ant	*1, *4	—	0.9	1.15	dB
		Rx – Ant	*2, *5	—	0.95	1.2	dB
		Dup_Out – Ext	*1, *4	—	0.45	0.7	dB
		Rx – D_Ext	*2, *5	—	0.5	0.75	dB
		Dup_Out – Ant	*1, *4	—	0.45	0.7	dB
		Rx – D_Ant	*2, *5	—	0.5	0.75	dB
Isolation	ISO.	Tx – Ext	*1	24	30	—	dB
		Tx – Ant	*1	24	30	—	dB
		Tx – Dup_In	*1	19	25	—	dB
		Rx – Ext	*2	24	30	—	dB
		Rx – Ant	*2	24	30	—	dB
		Rx – D_Ext	*2	24	30	—	dB
		Rx – D_Ant	*2	24	30	—	dB
		Dup_Out – Ext	*1, *4	29	35	—	dB
		Rx – Ext	*2, *5	29	35	—	dB
		Dup_Out – Ant	*1, *4	29	35	—	dB
		Rx – Ant	*2, *5	29	35	—	dB
		Dup_Out – Ext	*1, *4	24	30	—	dB
		Rx – D_Ext	*2, *5	24	30	—	dB
		Dup_Out – Ant	*1, *4	24	30	—	dB
		Rx – D_Ant	*2, *5	24	30	—	dB
		Tx – Rx	*1	43	50	—	dB

*1 Pin = 29.5dBm, 0/3V control, V_{DD} = 2.7V to 3.5V, 1,429MHz to 1,453MHz

*2 Pin = 10dBm, 0/3V control, V_{DD} = 2.7V to 3.5V, 1,477MHz to 1,501MHz

*3 π/4-shifted DQPSK, Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 1,429MHz to 1,453MHz,
ACP (±50kHz) < – 70dBc, ACP (±100kHz) < – 75dBc, 2nd harmonics < – 75dBc, 3rd harmonics < – 75dBc

*4 Rx terminal end is OPEN (Pattern cut).

*5 Dup_Out terminal end is OPEN (Pattern cut).

(Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Harmonics	2fo	Tx – Ext	*3	—	–70	–60	dBc
		Tx – Ant	*3	—	–70	–60	dBc
		Tx – Dup_In	*3	—	–75	–60	dBc
		Dup_Out – Ext (Main)	*3, *4	—	–75	–60	dBc
		Dup_Out – Ext (Div)	*3, *4	—	–70	–60	dBc
		Dup_Out – Ant (Main)	*3, *4	—	–70	–60	dBc
		Dup_Out – Ant (Div)	*3, *4	—	–70	–60	dBc
	3fo	Tx – Ext	*3	—	–67	–60	dBc
		Tx – Ant	*3	—	–67	–60	dBc
		Tx – Dup_In	*3	—	–70	–60	dBc
		Dup_Out – Ext (Main)	*3, *4	—	–67	–60	dBc
		Dup_Out – Ext (Div)	*3, *4	—	–67	–60	dBc
		Dup_Out – Ant (Main)	*3, *4	—	–67	–60	dBc
		Dup_Out – Ant (Div)	*3, *4	—	–67	–60	dBc
ACP	±50kHz	Tx – Ext	*3	—	–70	–57	dBc
		Tx – Ant	*3	—	–70	–57	dBc
		Tx – Dup_In	*3	—	–70	–57	dBc
		Dup_Out – Ext (Main)	*3, *4	—	–70	–57	dBc
		Dup_Out – Ext (Div)	*3, *4	—	–70	–57	dBc
		Dup_Out – Ant (Main)	*3, *4	—	–70	–57	dBc
		Dup_Out – Ant (Div)	*3, *4	—	–70	–57	dBc
	±100kHz	Tx – Ext	*3	—	–73	–65	dBc
		Tx – Ant	*3	—	–73	–65	dBc
		Tx – Dup_In	*3	—	–73	–65	dBc
		Dup_Out – Ext (Main)	*3, *4	—	–73	–65	dBc
		Dup_Out – Ext (Div)	*3, *4	—	–73	–65	dBc
		Dup_Out – Ant (Main)	*3, *4	—	–73	–65	dBc
		Dup_Out – Ant (Div)	*3, *4	—	–73	–65	dBc
Bias current	I_{DD}		V_{DD} = 3.0V		235	350	µA
Control current	Ictl		Vctl (H) = 3.0V		15	30	µA

*1 Pin = 29.5dBm, 0/3V control, V_{DD} = 2.7V to 3.5V, 1,429MHz to 1,453MHz

*2 Pin = 10dBm, 0/3V control, V_{DD} = 2.7V to 3.5V, 1,477MHz to 1,501MHz

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*4 Rx terminal end is OPEN (Pattern cut).

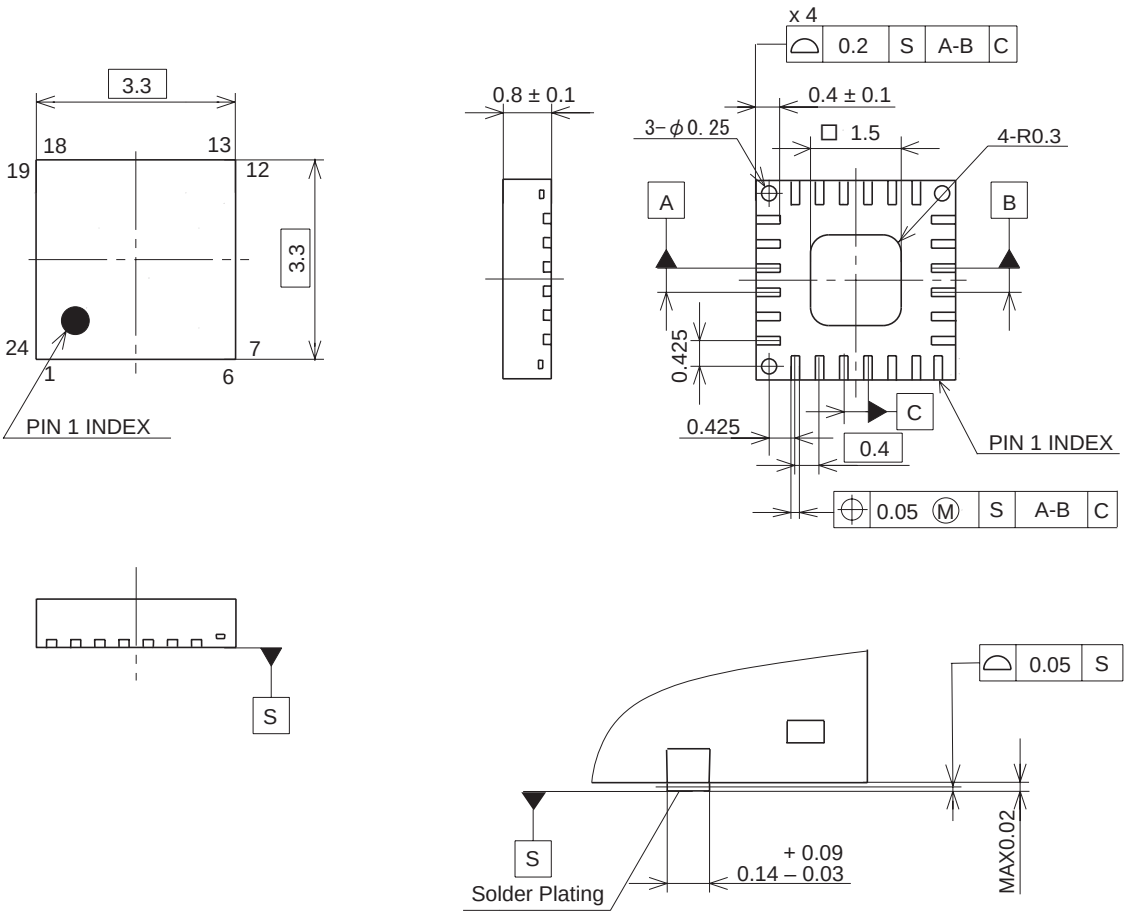
*5 Dup_Out terminal end is OPEN (Pattern cut).

Pin Description

Pin No.	Symbol	Description
2	D_Ant	RF signal output (Use it, connecting capacity.) (100pF is recommended.)
4	D_Ext	RF signal output (Use it, connecting capacity.) (100pF is recommended.)
6	Ext	RF signal output (Use it, connecting capacity.) (100pF is recommended.)
7	Ant	RF signal output (Use it, connecting capacity.) (100pF is recommended.)
12	Tx	RF signal input (Use it, connecting capacity.) (100pF is recommended.)
13	Dup_In	RF signal output (Use it, connecting capacity.) (100pF is recommended.)
17	Dup_Out	RF signal input (Use it, connecting capacity.) (100pF is recommended.)
19	Rx	RF signal input (Use it, connecting capacity.) (100pF is recommended.)
20	CTLA	Logic control A
21	CTLB	Logic control B
22	CTLC	Logic control C
23	CTLD	Logic control D
24	V_{DD}	Power supply input
1, 3, 5, 8, 9, 10, 11, 14, 15, 16, 18	GND	GND

Package Outline Unit: mm

24PIN VQFN（PLASTIC）



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	VQFN-24P-05
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm