GENERAL DESCRIPTION

The XRT79L71 is a single channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controller and Line Interface Unit with Jitter Attenuator that is designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L71 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of ATM or HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control. Industry standard UTOPIA II and POS-PHY interface are also provided.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- HDLC Controller that provides the mapping/extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola, PowerPC, and Mips µPs
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 208 STBI PBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.

ATM/PPP PROTOCOL PROCESSOR

TRANSMIT CELL PROCESSING

- Extracts ATM cells
- Supports ATM cell payload scrambling
- Maps ATM cells into E3 or DS3 frame
- PLCP frame and mapping of ATM cell streams

RECEIVE CELL PROCESSING

- Extraction of ATM cells from PLCP frame or directly from E3 or DS3 frame
- Termination of PLCP frame
- Supports payload cell de-scrambling

TRANSMIT PACKET PROCESSING

- Inserts PPP packets into data stream
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

UTOPIA/ SYSTEM INTERFACE

- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- Compliant with ATM Forum UTOPIA II interface
- Programmable FIFO size for both Transmit and Receive direction
- Compliant to POS-PHY Level 2 interface

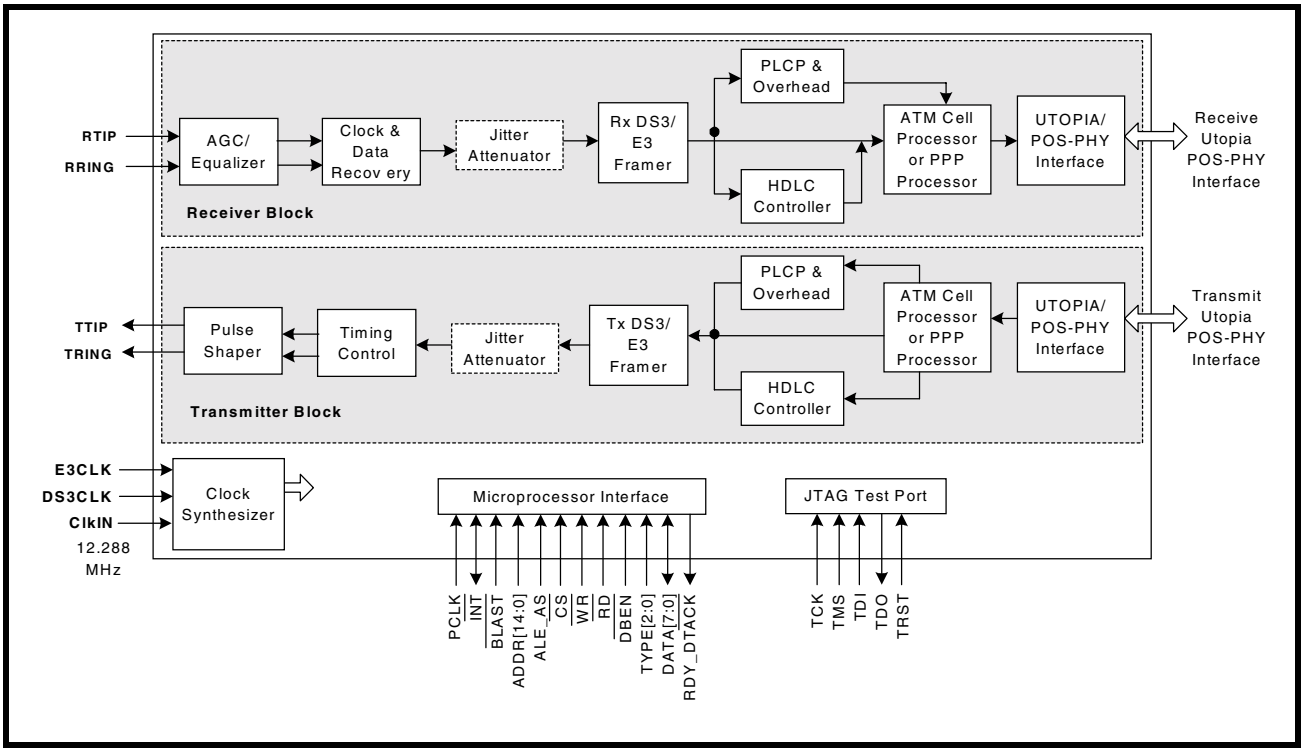
SERIAL INTERFACE

- Serial clock and data interface for accessing DS3/ E3 framer
- Serial clock and data interface for accessing cell/ packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs
- Digital, ATM, WAN and LAN Switches

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L71



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40°C to +85°C

TABLE 1: PIN OUT OF THE XRT79L71 (TOP VIEW)

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	TXUADDR_1	TXUADDR_3	TXUCLKO	TXPEOP	TXUCLK	RXMOD	RXUADDR_4	RXUADDR_0	RXUCLAV	RXUDATA_1	RXUDATA_2	RXUDATA_5	RXUDATA_9	RXUDATA_13	RXGFCMSB	RXGFCCLK
2	TXUADDR_0	TXUADDR_2	TXUADDR_4	RXPDVAL	TXPER	RXPERR	RXUCLKO	RXUADDR_1	RXUSOC	RXUDATA_0	RXUDATA_4	RXUDATA_8	RXUDATA_12	TXGFCCLK	RXPRED	RXPLOF
3	TXUDATA_0	TXUPRTY	TXUSOC	TXUCLAV	TXMOD	RXUCLK	RXPEOP	RXUADDR_2	RXUPRTY	RXUDATA_3	RXUDATA_7	RXUDATA_11	RXUDATA_15	RXGFC	TXPOHCLK	TXPOHFRAME
4	TXUDAT_3	TXUDATA_2	TXUDATA_1	TXUDATA_10	TXUEN_L	TSX_TSOF	RSX_RSOF	RXUADDR_3	RXUEN_L	RXUDATA_6	RXUDATA_10	RXUDATA_14	RXCP	RXPOHFRAME	RXNIB_3	RXNIB_2
5	TXUDATA_7	TXUDATA_6	TXUDATA_5	TXUDATA_4									RXPOOF	RXNIB_0	RXOUTCLK	RXSER
6	TXUDATA_12	TXUDATA_11	TXUDATA_9	TXUDATA_8									RXNIB_1	RXOHIND	RXFRAME	RXCLK
7	GPIO_0	TXUDATA_15	TXUDATA_14	TXUDATA_13			VDD	GND	GND	VDD			RXLOS	RXOH	RXOHENABLE	RXOHCLK
8	DMO_0	GPIO_3	GPIO_2	GPIO_1			VDD	GND	GND	VDD			TXNIB_1	TXNOB_2	TXNOB_3	RXOHFRAME
9	TCK	TMS	TDI	TDO			VDD	GND	GND	VDD			TXNIBCLK	TXSER	TXOHIND	TXNIB_0
10	TRING	TRST	MTIP	TXDGND			VDD	GND	GND	VDD			TXOHINS	TXINCLK	TXFRAME	TXNIBFRAME
11	TTIP	NC	MRING	TXDVDD									PDATA	TXOH	TXOHFRAME	TXFRAMEREF
12	TXAVDD	REFAVDD	REFAGND	TXAGND									PDATA_4	PDATA_1	TXOHCLK	TXOHENABLE
13	RXAVDD	RRING	ANAIO1	OVDD	OGND	GPI_2	GPO_2	PDBEN_L	DA_SEL	DPADDR_7	DPADDR_3	PADDR_6	PINT_L	PDATA_5	PDATA_2	TXAISEN
14	RXAGND	RTIP	ANAIO2	VDD	RESET_L	GPI_1	GPO_1	PTYPE_2	VDD	DPADDR_6	DPADDR_2	PADDR_5	PCS_L	PRDY_L	PDATA_6	PDATA_3
15	JAGND	TXON	ICTB	GND	TESTMODE	GPI_0	GPO_0	PTYPE_1	GND	DPADDR_5	DPADDR_1	PADDR_4	PADDR_1	PRD_L	PBLAST_L	PDATA_7
16	JAAVDD	CLKVDD	DS3CLK	CLKGND	E3CLK	NIBBLEINTF	CLKOUT	PTYPE_0	PCLK	DPADDR_4	DPADDR_0	PADDR_3	PADDR_2	PADDR_0	PWR_L	PAS_L

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PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
MICROPROCESSOR INTERFACE			
F16 F15 F14 F13 G16 G15 G14 G13 C16 D15 D16 E16 E15 E14 E13	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14	I	**Address Bus Input pins Microprocessor Interface:** These pins are used to select the on-chip Framer/UNI registers and RAM space for READ and WRITE Operations with the Microprocessor.
D11 C12 B13 A14 D12 C13 B14 A15	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Bi-Directional Data Bus pins Microprocessor Interface:** These pins are used to drive and receive data over the bi-directional data bus.
A16	ALE/AS	I	**Address Latch Enable/Address Strobe:** This input pin is used to latch the address present at the Microprocessor Interface Address Bus pins (A[6:0]) into the Framer/UNI Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. This input pin is active-high, in the Intel Mode and active low in the Motorola Mode.
D14	$\overline{CS}$	I	**Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the UNI/Framer on-chip registers and RAM locations.
D13	$\overline{INT}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer/UNI device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.
C15	$\overline{RD}$/$\overline{DS}$/	I	**READ Strobe Intel Mode:** If the Microprocessor Interface is operating in the Intel Mode, then this input pin will function as the $\overline{RD}$ (READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the Framer/UNI will place the contents of the addressed register within the Framer/UNI IC on the Microprocessor Bi-directional Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe Motorola Mode:** If the Microprocessor Interface is operating in the Motorola Mode, then this input will function as the $\overline{DS}$ (Data Strobe) signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
C14	RDY/$\overline{\text{DTACK}}$	O	**READY or DTACK:** This active-low output pin will function as the READY output when the Microprocessor Interface is configured to operate in the Intel Mode; and will function as the DTACK output, when the Microprocessor Interface is running in the Motorola Mode. **Intel Mode - READY output:** When the Framer/UNI negates this output pin (e.g., toggles it "Low") it indicates to the Microprocessor that the current READ or WRITE operation is to be extended until this signal is asserted (e.g., toggled "High"). **Motorola Mode - DTACK Data Transfer Acknowledge Output:** The Framer/UNI will assert this pin in order to inform the Microprocessor that the present READ or WRITE cycle is nearly complete. If the Framer/UNI requires that the current READ or WRITE cycle be extended, then the Framer/UNI will delay its assertion of this signal. The 68000 family of Microprocessors requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
M14	$\overline{\text{RESET}}$	I	**Reset Input:** When this active-low signal is asserted, the Framer/UNI device will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.
H16	µPCLK	I	**Microprocessor Interface Clock Input:** This clock input signal is used for synchronous/burst/DMA data transfer operations. This clock can be running up to 33MHz.
B16	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	**Write Strobe Intel Mode:** If the Microprocessor Interface is configured to operate in the Intel Mode, then this active-low input pin functions as the WR (WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, the Framer/UNI will latch the contents of the bi-directional data (D[7:0]) into the addressed registers or Buffer location within the Framer/UNI IC. **R/W Input Pin Motorola Mode:** When the Microprocessor Interface Section is operating in the Motorola Mode, then this pin is functionally equivalent to the R/W pin. In the Motorola Mode, a READ operation occurs if this pin is at a logic "1". Similarly a WRITE operation occurs if this pin is at a logic "0".

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
J16 J15 J14	PTYPE_0 PTYPE_1 PTYPE_2	I	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0]** / **Microprocessor Interface Mode** 000 — Asynchronous Intel 001 — Asynchronous Motorola 010 — Intel X86 011 — Intel I960, Motorola MPC860 100 — IDT3051/52 (MIPS) 101 — IBM Power PC
J13	$\overline{\text{DBEN}}$	I	**Bi-directional Data Bus Enable Input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to enable the Bi-directional Data Bus. Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.
B15	$\overline{\text{BLAST}}$	I	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate to the Microprocessor Interface block that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin by toggling it "Low" in order to denote that the current READ or WRITE operation within a BURST operation is the last operation of this BURST operation.
H13	Direct_Ad	I	**Direct Address Select pin:** This input pin is used to select the addressing mode for the Microprocessor Interface block. Setting this pin "High" will put the Microprocessor Interface block of the XRT79L71 into Direct Addressing Mode. In Direct Addressing Mode, all 15 address pins (A0 - A14) are used to select the on-chip Framer/UNI registers and RAM space for READ and WRITE Operations with the Microprocessor. ***NOTE:*** *It is recommended to set this pin "High" and access the Microprocessor Interface block using the Direct Addressing Mode.* Setting this pin "Low" will put the Microprocessor Interface block of the XRT79L71 into Indirect Addressing Mode. In Indirect Addressing mode, only the lower 8 address pins (A0 - A7) are used to select the on-chip Framer/UNI registers and RAM space for READ and WRITE Operations with the Microprocessor. Two microprocessor accesses are needed to READ or WRITE to the on-chip Framer/UNI registers and RAM space.

PIN #	NAME	TYPE	DESCRIPTION
TEST AND DIAGNOSTIC			
T9	TCK	I	**Test Clock input, Boundary Scan Clock input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
P9	TDI	I	**Test Data input, Boundary Scan Test Data Input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
N9	TDO	O	**Test Data output:** Boundary Scan Test Data Output:
R9	TMS	I	**Test Mode Select, Boundary Scan Test Mode Select input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
R10	TRST	I	**Test Mode Reset, Boundary Scan Mode Reset Input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
M15	TESTMODE	***	**Factory Test Mode Pin:** Tie this pin to Ground.
P15	$\overline{ICT}$	I	**In-Circuit Test Input Pin:** For normal operation, the user should pull this pin "High". ***NOTE:*** *This input pin is internally pulled "High".*
P13 P14	AnalO1 AnalO2	I/O	**Analog Input/Output Test Pin:** These pins should be pulled "Low" for normal operation.
L15 L14 L13	GPI_0 GPI_1 GPI_2	I	**General Purpose Input Test Pin:** These pins should be pulled "Low" for normal operation.
K15 K14 K13	GPO_0 GPO_1 GPO_2	O	**General Purpose Output Test Pin:** These pins should be left unconnected for normal operation.

PIN #	NAME	TYPE	DESCRIPTION
GENERAL PURPOSE INPUT AND OUTPUT PINS			
T8	DMO	O	**Drive Monitor Output Output Pin:** If this input signal is "High", then it means that the drive monitor circuitry within the XRT79L71 has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit periods. If this input signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT79L71.
T7 N8 P8 R8	GPIO_0 GPIO_1 GPIO_2 GPIO_3	I/O	**General Purpose Input/Output Pins:** Each of these pins can be configured to function as either an input or output pin. If a given pin is configured to function as an input pin, then the state of this input pin can be monitored by reading Bit X within the "XXX" Register (Address Location = 0xXX, 0xXX). If a given pin is configured to function as an output pin, then the state of these output pins can be controlled by writing the appropriate value into Bit X within the "XXX" Register.

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT SYSTEM SIDE INTERFACE PINS			
A13	TxAISEn	I	**Transmit AIS Pattern Input pin:** This input pin is used to command the Transmit DS3/E3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "High" configures the Transmit DS3/E3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "Low" configures the Transmit DS3/E3 Framer block to NOT transmit an AIS pattern to the remote terminal equipment. ***NOTE:*** *For normal operation, or if the user wishes to control the Transmit AIS function, via Software Control; the user should tie this input pin to GND.*
L16	NibbleIntf	I	**Nibble Interface Select Input pin:** This input pin is used to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface blocks to operate in either the Serial or the Nibble-Parallel Mode. **Setting this input pin "High" configures each of these blocks to operate in the Nibble-Parallel Mode.** In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data from the local terminal equipment in a nibble-parallel manner via the TxNib[3:0] input pins. Further, the Receive Payload Data Output Interface block will output inbound payload data to the local terminal equipment in a nibble-parallel via the RxNib[3:0] output pins. **Setting this input pin "Low" configures each of these blocks to operate in the Serial Mode.** In this mode, the Transmit Payload Data Input Interface block will accept the outbound payload data from the local terminal equipment in a serial manner via the TxSer input pin. Further, the Receive Payload Data Output Interface block will output the inbound payload data to the local terminal equipment in a serial manner, via the RxSer output pin. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B10	TxFrame	O	**Transmit End of DS3/E3 Frame Indicator:** This output pin is pulse "High" for one DS3 or E3 clock period, when the Transmit Section of the XRT79L71 is processing the last bit of a given DS3 or E3 frame. The implications of this output pin, for each mode of operation, are described below. **ATM UNI/PPP/High-Speed HDLC Controller Mode:** This output pin serves as an end-of-frame indication to the local terminal equipment. **Clear-Channel Framer Mode:** If the XRT79L71 is configured to operate in the Clear-Channel Framer mode, then this output pin serves to alert the Local Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame. Hence, the Local Terminal Equipment uses this output signal to maintain Framing Alignment with the XRT79L71.
A11	TxFrameRef	I	**Transmit DS3/E3 Framer - Framing Alignment Input pin:** If the the Transmit Section of the XRT79L71 is configured to operate in the Local-Timing/Frame-Slave Mode, then the Transmit DS3/E3 Framer block will use this input signal as the Framing Reference. When the XRT79L71 is configured to operate in this mode any rising edge at this input pin will cause the Transmit DS3/E3 Framer block to begin its creation of a new DS3 or E3 frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 or E3 frame rates to this input pin. Further, it is imperative that this clock signal be synchronized with the 44.736MHz or 34.368MHz clock signal applied to the TxInClk input pin. ***NOTE:*** *This input pin should be tied to GND if it is not to be used as the Transmit DS3/E3 Framer - Framing Reference input signal.*
C10	TxInClk	I	**Transmit DS3/E3 Framer Block - Timing Reference Signal:** If the Transmit Section of the XRT79L71 is configured to operate in the Local-Timing Mode, then it will use this signal as the Timing Reference. If the XRT79L71 is being operating in the DS3 Mode, then the user is expected to apply a high-quality 44.736MHz clock signal to this input pin. Likewise, if the XRT79L71 is being operated in the E3 Mode, then the user is expected to apply a high-quality 34.368MHz clock signal to this input pin. **Note for Clear-Channel Framer Operation:** If the user is operating the XRT79L71 in the Clear-Channel Framer mode, then the user should design the local terminal equipment circuitry, such that outbound DS3 or E3 data will be output, upon the falling edge of TxInClk. The Transmit Payload Data Input Interface within the Transmit Section of the XRT79L71 will sample the data, applied to the TxSer input pin, upon the rising edge of TxInClk. ***NOTE:*** *This input pin should be tied to GND if the XRT79L71 is configured to operate in the Loop-Timing Mode.*

PIN #	NAME	TYPE	DESCRIPTION
C11	TxOH/ TxHDLCDat_5	I	**Transmit Overhead Data Input/Transmit HDLC Controller Data Bit 5 input pin:** The function of This input pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOH:** The Transmit Overhead Data Input Interface accepts overhead via this input pin, and insert this data into the overhead bit positions within the outbound DS3 or E3 frames. If the TxOHIns input pin is pulled "High", then the Transmit Overhead Data Input Interface will sample the overhead data, via this input pin, upon the falling edge of the TxOHClk output signal. Conversely, if the TxOHIns input pin is NOT pulled "High", then the Transmit Overhead Data Input Interface block will be inactive and will not accept any overhead data via the TxOH input pin. **High Speed HDLC Controller Mode - TxHDLCDat_5:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 5 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.
D10	TxOHIns/ TxHDLCDat_4	I	**Transmit Overhead Data Insert Input/Transmit HDLC Controller Data Bit 4 input pin:** The function of this input pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHIns:** This input pin is used to either enable or disable the Transmit Overhead Data Input Interface block. If the Transmit Overhead Data Input Interface block is enabled, then it will accept overhead data from the local terminal equipment via the TxOH input pin; and insert this data into the overhead bit positions within the outbound DS3 or E3 data stream. Conversely, if the Transmit Overhead Data Input Interface block is disabled, then it will NOT accept overhead data from the local terminal equipment.Pulling this input pin "High" enables the Transmit Overhead Data Input Interface block. Pulling this input pin "Low" disables the Transmit Overhead Data Input Interface block. **High-Speed HDLC Controller Mode - TxHDLCDat_4:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 4 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.
B12	TxOHClk	O	**Transmit Overhead Clock Output:** This output pin functions as the Transmit Overhead Data Input Interface clock signal. If the user enables the Transmit Overhead Data Input Interface block by asserting the TxOHIns input pin, then the Transmit Overhead Data Input Interface block will sample and latch the data residing on the TxOH input pin upon the falling edge of this signal. ***NOTE:*** *The Transmit Overhead Data Input Interface block is disabled if the user has configured the XRT79L71 to operate in the High-Speed HDLC Controller Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B11	TxOHFrame/ TxHDLCClk	O	**Transmit Overhead Framing Pulse/Transmit HDLC Controller Clock Output pin:** The function of this output pin depends upon whether or not the XRT79L71 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High-Speed HDLC Controller Mode - TxOHFrame:** This output pin pulses high for one TxOHClk period coincident with the instant the Transmit Overhead Data Input Interface would be accepting the first overhead bit within an outbound DS3 or E3 frame. **High Speed HDLC Controller Mode - TxHDLCClk:** This output pin functions as the demand clock output signal for the Transmit HDLC Controller byte-wide input interface. This clock signal is ultimately derived from either the TxInClk or the RxOutClk signal. Hence, the frequency of this clock signal is nominally one-eight of that of the TxInClk or the RxOutClk signals. The Transmit HDLC Controller block will sample the contents of the Transmit HDLC Controller byte-wide input interface, upon the rising edge of this clock output signal. Therefore, the local terminal equipment should be designed to output data onto the TxHDLCDat[7:0] bus upon the falling edge of this clock output signal.
A12	TxOHEnable/ TxHDLCDat_7	I/O	**Transmit Overhead Enable Output indicator/Transmit HDLC Controller Data Bit 7 Input:** The function of this input pin depends upon whether or not the XRT79L71 is configured to operate in the High Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHEnable:** The XRT79L71 will assert this output pin, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the local terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 data stream, then it is expected to sample the state of this signal, upon the falling edge of TxInClk. Upon sampling the TxOHEnable signal "High", the local terminal equipment should; (1) place the desired value of the overhead bit onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the TxOH signal, upon the rising edge of the very next TxInClk input signal. **High-Speed HDLC Controller Mode - TxHDLCDat_7:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 7 (the MSB) within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.

PIN #	NAME	TYPE	DESCRIPTION
C9	TxSer TxPOH SendMSG	I	**Transmit Payload Data Serial Input/Transmit PLCP Path Overhead Input/ Send HDLC Message Request Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxSer:** If the XRT79L71 is configured to operate in the Clear-Channel Framer mode, then this input pin functions as the Transmit Payload Data Serial Input pin. In this case, the local terminal equipment is expected to apply all outbound data which is intended to be carried via the DS3 or E3 payload bits to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxSer input pin, upon the rising edge of TxInClk. **ATM/PLCP Mode - TxPOH:** If the XRT79L71 is configured to operate in the ATM Mode, and if within the ATM Mode, the chip is also configured to operate in the PLCP Mode, then this input pin functions as the Transmit PLCP Path Overhead Input Pin. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input Pin (and Port) become active whenever the user asserts the TxPOHIns input pin by pulling it "High". In this case, the data, residing upon the TxPOH input pin will be sampled upon the rising edge of the TxPOHClk signal. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - SendMSG:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller Mode, then this input pin functions as the Transmit HDLC Controller Input Interface enable input pin. If the user asserts this input pin by pulling it "High" then the Transmit HDLC Controller Input Interface will proceed to latch the data, residing on the TxHDLCDat[7:0] input pins, upon each rising edge of the TxHDLCClk signal. All data that is latched into the Transmit HDLC Controller Input Interface for the duration that the SendMSG input pin is "High" will be encapsulated into an HDLC frame and ultimately transported via the payload bits of the outbound DS3 or E3 data stream. If the user pulling this input pin "Low", then the Transmit HDLC Controller Input Interface will cease latching the data, residing on the TxHDLCDat[7:0] bus. ***NOTE:*** *This input pin is inactive if the XRT79L71 has been configured to operate in the PPP Mode.*
B3	TxPOHClk	O	**Transmit PLCP Frame POH Byte Insertion Clock:** This pin, along with the TxPOH and the TxPOHMSB input pins, function as the Transmit PLCP Frame POH Byte serial input port. This output pin functions as a clock output signal that is be used to sample the user's POH data at the TxPOH input pin. This output pin is always active, independent of the state of the TxPOHIns pin. ***NOTE:*** *This pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B9	TxOHInd/ TxPFrame/ TxHDLCDat_6/	I/O	**Transmit Overhead Data Indicator Output/Transmit PLCP Frame Boundary Indicator Output/Transmit HDLC Controller Data Bit 6 input pin:** The function of these input/output pins depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode, the ATM/ PLCP Mode or the High-Speed HDLC Mode. **Clear-Channel Framer Mode - TxOHInd:** In the Clear-Channel Framer Mode, this output pin functions as the transmit overhead data indicator for the local terminal equipment. This output pin is pulsed "High" for one DS3 or E3 bit period in order to indicate to the local terminal equipment that the Transmit Section of the Framer is going to be processing an overhead bit, upon the next rising edge of TxInClk., and will NOT latch the data that is applied to the TxSer input pin. Therefore, when the local terminal equipment samples the TxOHInd output pin "High", then it must not apply the next payload bit to TxSer input pin. This output pin serves as a warning that this particular payload bit is going to be ignored by the Transmit Section of the Framer, and will not be inserted into payload bits, within the outbound DS3 or E3 data stream. **ATM/PLCP Mode - TxPFrame:** If the XRT79L71 is configured to operate in the ATM UNI/PLCP Mode, then this output pin will denote the boundaries of outbound PLCP frames, as they are being processed by the Transmit PLCP Processor block. This output pulses "High" when the last nibble of a given PLCP frame is being routed to the Transmit DS3/E3 Framer block. This output pin is inactive if the XRT79L71 is operating in the Direct-Mapped ATM Mode. **High-Speed HDLC Controller Mode - TxHDLCDat_6:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 6 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.

PIN #	NAME	TYPE	DESCRIPTION
D9	TxNibClk/ TxGFCMSB/ SendFCS	I/O	**Transmit Nibble Clock Output pin/Transmit GFC Byte - MSB Indicator Output/Send FCS Value Request Input:** The function of this input/output pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNibClk:** When operating in the Nibble-Parallel Mode the XRT79L71 will derive this clock signal from either the TxInClk or the RxLineClk signal depending upon whether the chip is operating in the Local-Timing or Loop-Timing Mode. The user is advised to configure the Terminal Equipment to output the outbound payload data to the XRT79L71 onto the TxNib_[3:0] input pins, upon the rising edge of this clock signal. The Transmit Payload Data Input Interface block will sample the data, residing on the TxNib_[3:0] line, upon the falling edge this clock signal. ***NOTES:*** 1. *For DS3 applications, the XRT79L71 will output 1176 clock pulses to the local terminal equipment for each outbound DS3 frame.* 2. *For E3, ITU-T G.832 applications, the XRT79L71 will output 1074 clock pulses to the local terminal equipment for each outbound E3 frame.* 3. *For E3, ITU-T G.751 applications, the XRT79L71 will output 384 clock pulses to the local terminal equipment for each outbound E3 frame.* **ATM Mode - TxGFCMSB:** This signal, along with TxGFC and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. This output signal will pulse "High" when the MSB (most significant bit) of the GFC nibble for a given outbound cell is expected at the TxGFC input pin. **High-Speed HDLC Controller Mode - SendFCS:** The local terminal equipment is expected to control both this input pin, along with the SendMSG input pin, during the construction and transmission of each outbound HDLC frame. This input pin is used to command the Transmit HDLC Controller block to compute and insert the computed FCS (Frame-Check Sequence) value into the back-end of the outbound HDLC frame, as a trailer. If the user has configured the Transmit HDLC Controller block to compute and insert a CRC-16 value into the outbound HDLC frame, then the local terminal equipment is expected to hold this input pin "High" for two periods of TxHDLCClk.Conversely, if the user has configured the Transmit HDLC Controller block to compute and insert a CRC-32 value into the outbound HDLC frame, then the local terminal equipment is expected to hold this input pin "High" for four (4) periods of TxHDLCClk. ***NOTES:*** 1. *This input/output pin is inactive if the XRT79L71 has been configured to operate in the PPP Mode.* 2. *This input/output pin is inactive if the XRT79L71 has been configured to operate in the Clear-Channel Framer/Serial mode.*

PIN #	NAME	TYPE	DESCRIPTION
C2	TxGFCClk	O	**Transmit GFC Nibble-Field Serial Input port - Clock Output signal:** This signal, along with TxGFC and TxGFCMSB combine to function as the Transmit GFC Nibble-field serial input port. This output signal functions as the demand clock signal for this port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into the TxGFC input pin. The Transmit GFC Nibble-Field serial input port will latch the contents of TxGFC upon the rising edge of this clock signal. Hence, the local terminal equipment should be designed to place its outbound GFC bits on to the TxGFC line, upon the falling edge of this clock signal. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configure to operate in the ATM Mode.*
B8	TxNib_3/ TxPOHIns/ TxHDLCDat_3	I	**Transmit Nibble Interface - Bit 3/Transmit PLCP Path Overhead Insert enable/Transmit HDLC Controller Data Bus - Bit 3 input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_3:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 3 (MSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0 through TxNib_2) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxPOHIns:** f the XRT79L71 is configured to operate in the ATM Mode, and if (within the ATM Mode, the chip is also configured to operate in the PLCP Mode), then this input pin functions as the Transmit PLCP Path Overhead Port - Enable input pin. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input port becomes active whenever the user asserts this input pin by pulling it "High". Once this occurs, the data, residing upon the TxPOH input pin will be sampled upon the rising edge of the TxPOHClk signal. This input pin is inactive if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode. **High-Speed HDLC Controller Mode - TxHDLCDat_3:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 3 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.

PIN #	NAME	TYPE	DESCRIPTION
C8	TxNib_2/ TxStuff_Ctl/ TxHDLCDat_2	I	**Transmit Nibble Input Interface - Bit 2/Transmit PLCP Stuff Control Input/ Transmit HDLC Controller Data Bus - Bit 2 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_2:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0, TxNib_2 and TxNib_3) upon the falling edge of TxNibClk ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxStuff_Ctl:** This input pin is used to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375 us). The first PLCP frame (first, within a stuff opportunity period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a stuff opportunity period will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if this input pin is pulled "Low", and 14 trailer nibbles if this input pin is pulled "High". ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_2:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 1 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.

PIN #	NAME	TYPE	DESCRIPTION
D8	TxNib_1/ Tx8KREF/ TxHDLCDat_1	I	**Transmit Nibble Input Interface - Bit 1/Transmit PLCP Framing 8kHz Reference Input/Transmit HDLC Controller Data Bus - Bit 1 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_1:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_0, TxNib_2 and TxNib_3) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - Tx8KREF:** If the XRT79L71 is configured to operate in the ATM/PLCP Mode, then the Transmit PLCP Processor can be configured to synchronize its PLCP frame generation to this input clock signal. The Transmit PLCP Processor will also use this input signal to compute the nibble-trailer stuff opportunities. ***NOTE:*** *This input pin is inactive if the use has configured the XRT79L71 to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_1:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 1 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.
A9	TxNib_0/ TxGFC/ TxHDLCDat_0	I	**Transmit Nibble Interface - Bit 0/Transmit GFC Input pin/Transmit HDLC Controller Data Bus - Bit 0 Input:** The function of this input pin depends upon whether the XRT79L71 is configured to operate in the Clear-Channel Framer Mode, the High Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNib_0:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this input pin will function as the bit 0 (LSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signal (along with TxNib_1 through TxNib_3) upon the falling edge of TxNibClk. ***NOTE:*** *This input pin is inactive if the XRT79L71 is configured to operate in the Serial Mode.* **ATM Mode - TxGFC:** This signal, along with TxGFCMSB, and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into this input pin. Each of these four bits will be clocked into the port upon the rising edge of the TxGFCClk output signal. **High-Speed HDLC Controller Mode - TxHDLCDat_0:** If the XRT79L71 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. This input pin will function as Bit 0 (the LSB) within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signal.

PIN #	NAME	TYPE	DESCRIPTION
A10	TxCellTxed/ TxNibFrame/ ValidFCS	O	**Transmit Cell Generator indicator/Transmit Nibble Frame Indicator/Valid FCS Indicator output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM Mode, the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - TxCellTxed:** This output pin pulses "High" each time the Transmit Cell Processor transmits a cell to either the Transmit PLCP Processor or the Transmit DS3/E3 Framer block. **Clear-Channel Framer Mode - TxNibFrame:** This output pin pulses "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNib[3:0] input pins. The purpose of this output pin is to alert the local terminal equipment that it needs to begin the transmission of a new DS3 or E3 frame to the XRT79L71. ***NOTE:*** *This output pin is not active if the XRT79L71 is configured to operate in the Serial-Mode.* **High-Speed HDLC Controller Mode - ValidFCS:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive HDLC Controller output Data bus (RxHDLCDat_[7:0]). ***If RxIdle = "High":*** The Receive HDLC Controller block with drive this output pin "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDat[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received an ABORT sequence.
M2	TxPERR	I	**Transmit Error Indicator from Link Layer:** This input signal is used to indicate that the current packet is ABORTED and must be discarded. This input pin should only be asserted when the last byte (or word) is be written onto the TxPData[15:0] input pins. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
N1	TxPEOP	I	**Transmit POS-PHY Interface - End of Packet:** The link layer processor toggles this output pin "High" whenever the Link Layer Processor is writing the last byte (or word) of a given Packet into the TxPData[15:0] data bus. ***NOTES:*** 1. *This input pin is only valid when the XRT79L71 is configured to operate in the PPP Mode.* 2. *This input pin is only valid when the Transmit POS-PHY Interface - Write Enable Input pin ($\overline{TxPEn}$) is asserted.*

PIN #	NAME	TYPE	DESCRIPTION
R3	TxUPrty/ TxPPrty	I	**Transmit UTOPIA Data Bus - Parity Input/Transmit POS-PHY Interface - Parity Input:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - TxUPrty:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[7:0] or TxUData[15:0]) inputs of the XRT79L71, respectively. ***NOTE:*** *This parity value should be computed based upon the odd-parity of the data applied at the Transmit UTOPIA Data Bus.* The Transmit UTOPIA Interface block within the XRT79L71 will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin. **PPP Mode - TxPPrty:** The Link Layer Processor will apply the parity value of the byte or word which is being applied to the Transmit POS-PHY Data Bus (e.g., TxPData[7:0] or TxPData[15:0]) inputs of the XRT79L71, respectively. ***NOTE:*** *This parity value should be computed based upon the odd-parity of the data applied to the Transmit POS-PHY Data Bus. The Transmit POS-PHY Interface block within the XRT79L71 will independently compute an odd-parity value of each byte (or word) that it receives from the Link Layer processor and will compare it will the logic level of this input pin.*
M4	$\overline{\text{TxUEN}}$/ $\overline{\text{TxPEN}}$	I	Transmit UTOPIA Interface Block - Write Enable/Transmit POS-PHY Interface - Write Enable: The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode Operation - TxUEN:** This active-low signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted, then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus, will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated. **PPP Mode Operation - $\overline{\text{TxPEN}}$:** This active-low signal, from the Link Layer processor enables the data on the Transmit POS-PHY Data Bus to be written into the TxFIFO on the rising edge of TxPClk. When this signal is asserted, then the contents of the byte or word that is present, on the Transmit POS-PHY Data Bus, will be latched into the Transmit POS-PHY Interface block, on the rising edge of TxPClk. When this signal is negated, then the Transmit POS-PHY Data bus inputs will be tri-stated.

PIN #	NAME	TYPE	DESCRIPTION
N3	TxUClav/ TxPPA	O	**Transmit UTOPIA Interface - Cell Available Output Pin/Transmit POS-PHY Interface - Packet Data Available Output pin:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - TxUClav:** This output pin supports data flow control between the ATM Layer processor and the Transmit UTOPIA Interface block. This signal is asserted (toggles "High") when the TxFIFO is capable of receiving at least one more full cell of data from the ATM Layer processor. This signal is negated, if the TxFIFO is not capable of receiving one more full cell of data from the ATM Layer processor. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins match that within the Transmit UTOPIA Address Register. Afterwards, this output pin will behave in accordance with the cell-level handshake mode. **PPP Mode - TxPPA:** The XRT79L71 will drive this output pin "High" whenever a programmable number of bytes of empty space is available for writing more packet data into the TxFIFO.
P3	TxUSoC/ TxPSoP	I	**Transmit UTOPIA - Start of Cell Input/Transmit POS-PHY - Start of Packet Input:** The function of this input signal depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode Operation - TxUSoC:** This input pin is driven by the ATM Layer Processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM Layer Processor. This input pin must be pulsed "High" whenever the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus (TxUData[15:0]). This input pin must remain "Low" at all other times. **PPP Mode Operation - TxPSoP/TxPSoC:** If the XRT79L71 has been configured to operate in the Packet-Mode, then this input pin is pulsed "High" to denote that the first byte (or word) of a given packet is placed on the TxPData[15:0] input pins.If the XRT79L71 has been configured to operate in the Cell-Chunk Mode, then this input pin is pulsed "High" to denote that the first byte of a packet chunk, if placed on the TxPData[15:0] input pins. ***NOTE:*** *This input pin is only valid if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
L4	TxTSX/ TxPSOF	I	**Transmit - Start of Transfer/Transmit - Start of PPP Packet in Chunk Mode:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the Packet Mode or Cell-Chunk Mode. **Packet Mode - TxTSX:** The Link-Layer processor pulses this input pin "High" when an in-band port address is present on the TxPData[7:0] bus. When this input pin and $\overline{\text{TxPEN}}$ are both set "High" then the value of TxP-Data[7:0] is the address value of the TxFIFO to be selected. Subsequent write operations, into TxPData[15:0] will fill the TxFIFO corresponding to this inband address. **Chunk Mode - TxPSOF:** The Link Layer processor pulses this input pin "High" in order to indicate that the first byte (or word) of a given Packet is placed on the TxPData[15:0] pins. ***NOTE:*** *This input pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
P1	TxUClkO/ TxPClkO	O	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Output:** This output is derived from an internal PLL.
M1	TxUClk/ TxPClk	I	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - TxUClk:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk. **PPP Mode - TxPClk:** The Transmit POS-PHY Interface clock is used to latch the data on the Transmit POS-PHY Data bus, into the Transmit POS-PHY Interface block. This clock signal is also used as the timing source for circuitry used to process the Packet data into and through the TxFIFO.
T2 T1 R2 R1 P2	TxUAddr_0 TxUAddr_1 TxUAddr_2 TxUAddr_3 TxUAddr_4	I	**Transmit UTOPIA Address Bus:** These input pins comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the XRT79L71 is operating in the Multi-PHY mode. When the ATM Layer processor wishes to write data to a particular UNI (PHY-Layer) device, it will provide the address of the intended UNI on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of TxUClk. The UNI will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed contents of the TxUT Address Register (Address = 70h). If these two values are identical and the $\overline{\text{TxUEN}}$ pin is asserted, then the TxUClav pin will be driven to the appropriate state based upon the TxFIFO fill level for the Cell Level handshake mode of operation.

PIN #	NAME	TYPE	DESCRIPTION
M3	TxMod	I	**Transmit PPP Data Bus - Modulo Indicator:** This input pin is used to specify the number of valid packet octets are being placed on the TxPData[15:0] input pins. The Link Layer Processor is expected to set this input pin "Low" when both bytes on the TxPData[15:0] data bus is valid packet data. Conversely, the Link Layer Processor is expected to set this input pin "High" when only the upper octet has valid packet data. ***NOTES:*** 1. *This input pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.* 2. *The Link Layer Processor is expected to set this input pin to the appropriate state, as each 16-bit word is being written into the TxPData[15:0] data bus.*
T3 P4 R4 T4 N5 P5 R5 T5 N6 P6 N4 R6 T6 N7 P7 R7	TxUData_0/ TxPData_0 TxUData_1/ TxPData_1 TxUData_2/ TxPData_2 TxUData_3/ TxPData_3 TxUData_4/ TxPData_4 TxUData_5/ TxPData_5 TxUData_6/ TxPData_6 TxUData_7/ TxPData_7 TxUData_8/ TxPData_8 TxUData_9/ TxPData_9 TxUData_10/ TxPData_10 TxUData_11/ TxPData_11 TxUData_12/ TxPData_12 TxUData_13/ TxPData_13 TxUData_14/ TxPData_14 TxUData_15/ TxPData_15	I	**Transmit UTOPIA Data Bus Inputs/Transmit POS-PHY Data Bus Inputs:** The function of these input pins depends upon whether the XRT79L71 is operating in the ATM UNI Mode or in the PPP Mode. **ATM UNI Operation - TxUData[15:0]:** These input pins comprise the Transmit UTOPIA Data Bus input pins. When the ATM Layer Processor wishes to transmit ATM cell data through the XRT72L74 ATM UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block upon the rising edge of TxUClk. **PPP Operation - TxPDATA[15:0]** These input pins comprise the Transmit POS-PHY Data Bus input pins. When a Network Processor wishes to transmit PPP data through the XRT79L71 Framer/UNI IC, it must place this data on these pins. The data, on the Transmit POS-PHY Data Bus is latched into the Transmit POS-PHY Interface block upon the rising edge of TxPClk.

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE SYSTEM SIDE INTERFACE PINS			
A4	RxAIS/ RxNib_2/ RxHDLCDat_2	O	**Receive AIS Pattern Indicator/Receive Nibble Output Interface - Bit 2/ Receive HDLC Controller Data Bus - Bit 2 output pin:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Interface Mode, the High-Speed HDLC Controller Mode, or in the other modes. **Other Modes - RxAIS:** This output pin is driven "High" whenever the Receive Section of the XRT79L71 has detected and is currently declaring an AIS (Alarm Indicator Signal) condition. **Clear-Channel Framer/Nibble-Parallel Interface Mode - RxNib_2:** If the XRT79L71 is configured to operate in the Nibble-Parallel Mode, then this output pin will function as the bit 2 output from the Receive Nibble-Parallel output interface. The Receive Payload Data Output Interface block will output this signal (along with RxNib_0, RxNib_1, and RxNib_3) upon the rising edge of the RxClk output signal. **High-Speed HDLC Controller Mode - RxHDLCDat_2:** This output pin along with RxHDLCDat_[7:3] and RxHDLCDat_[1:0] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
B4	RxRED/ RxNib_3/ RxHDLCDat_3	O	**Receive Section Red Alarm Indicator/Receive Nibble Interface Output pin - Bit 3/Receive HDLC Controller Data Bus output pin - Bit 3:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_3:** The XRT79L71 will output Received data from the remote terminal equipment to the local terminal equipment via this pin, along with RxNib_0 through RxNib_2. This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's local terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_3:** This output pin along with RxHDLCDat_[7:4] and RxHDLCDat_[2:0] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. **Other Modes - RxRED:** The Framer/UNI asserts this output pin to denote that one of the following events has been detected by the Receive DS3/E3 Framer block: • LOS - Loss of Signal Condition • OOF - Out of Frame Condition • AIS - Alarm Indication Signal Detection

PIN #	NAME	TYPE	DESCRIPTION
D6	RxOOF/ RxNib_1/ RxHDLCDat_1	O	**Receive Out of Frame Indicator/Receive Nibble Interface Output pin - Bit 1/ Receive HDLC Controller Data Bus Output pin - Bit 1:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode or the High-Speed HDLC Controller Mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_1:** The XRT79L71 will output Received data from the remote terminal equipment to the local terminal equipment via this pin, along with RxNib_0, RxNib_2 and RxNib_3: This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's local terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_1:** This output pin along with RxHDLCDat_[7:2] and RxHDLCDat_0 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. **All other Modes - RxOOF:** The UNI Receive DS3 Framer will assert this output signal whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
B5	RxLCD/ RxOutClk/ RxHDLCDat_7	O	**Receive Loss of Cell Delineation indicator/Receive Output Clock signal/ Receive HDLC Controller Data Bus - Bit 7 Output:** The function of output pin depends upon whether the XRT79L71 has been configured to operate in the ATM, Clear-Channel Framer or High Speed HDLC Controller Mode. **ATM Mode - RxLCD:** This active-high output pin will be asserted whenever the Receive Cell Processor has experienced a Loss of Cell Delineation. This pin will return "Low" once the Receive Cell Processor has regained Cell Delineation. **Clear-Channel Framer Mode - RxOutClk:** This clock signal functions as the Transmit Payload Data Input Interface clock source, if the XRT79L71 has been configured to operate in the loop-timing mode. In this mode, the local terminal equipment is expected to input data to the TxSer input pin, upon the rising edge of this clock signal. The XRT79L71 will use the rising edge of this signal to sample the data on the TxSer input. **High-Speed HDLC Controller Mode - RxHDLCDat_7:** This output pin along with RxHDLCDat_[6:0] functions as the Receive HDLC Controller byte wide output data bus. This particular output pin functions as the MSB (Most Significant Bit) of the Receive HDLC Controller byte wide data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.

PIN #	NAME	TYPE	DESCRIPTION
D7	RxLOS	O	**Framer/UNI - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section of the XRT79L71 encounters 180 consecutive 0's (for DS3 applications) or 32 consecutive 0's (for E3 applications) via the RxPOS and RxNEG pins. This pin will be negated once the Receive DS3/E3 Framer has detected at least 60 "1s" out of 180 consecutive bits (for DS3 applications) or has detected at least four consecutive 32 bit strings of data that contain at least 8 "1s" in the receive path.
B2	RxPRED	O	**Receiver Red Alarm Indicator - Receive PLCP Processor:** The Framer/UNI asserts this output pin to denote that one of the following events has been detected by the Receive PLCP Processor: • OOF - Out of Frame Condition • LOF - Loss of Frame Condition ***NOTE:*** *This output pin is only valid if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
D5	RxPOOF	O	**Receive PLCP Out of Frame Indicator:** The Receive PLCP Processor will assert this pin, when it declares an Out of Frame condition. This output will be negated when the Receive PLCP Processor reaches the In Frame Condition. ***NOTE:*** *This output pin is only valid if the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
A2	RxPLOF	O	**Receive PLCP - Loss of Frame Output Indicator:** The Receive PLCP Processor will assert this pin, when it declares a Loss of Frame condition. This output will be negated when the Receive PLCP Processor reaches the In Frame Condition. ***NOTE:*** *This output pin is only active is the XRT79L71 has been configured to operate in the ATM/PLCP Mode.*
C5	RxNib_0/ RxHDLCDat_0	O	**Receive Nibble Interface Output pin - Bit 0/Receive HDLC Controller Data Bus output pin - Bit 0:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel/Nibble-Parallel Mode - RxNib_0:** The XRT79L71 will output Received data from the remote terminal equipment to the local terminal equipment via this pin, along with RxNib_1 through RxNib_3. This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's local terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_0:** This output pin along with RxHDLCDat_[7:1] functions as the Receive HDLC Controller byte wide output data bus. This particular output pin functions as the LSB (Least Significant Bit) of the Receive HDLC Controller byte wide data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. ***NOTE:*** *This output pin is only active if the XRT79L71 is configured to operate in the Clear-Channel/Nibble-Parallel Mode or in the High-Speed HDLC Controller Mode. This output is inactive for all remaining modes.*

PIN #	NAME	TYPE	DESCRIPTION
B7	RxOHEnable/ RxHDLCDat_5	O	**Receive Overhead Data Output Interface - Enable Output/Receive HDLC Controller Data Bus - Bit 5 output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHEnable:** The XRT79L71 will assert this output signal for one RxOHClk period when it is safe for the local terminal equipment to sample the data on the RxOH output pin. **High-Speed HDLC Controller Mode - RxHDLCDat_5:** This output pin along with RxHDLCDat_[4:0], RxHDLCDat_6 and RxHDLCDat_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
C7	RxOH/ RxHDLCDat_6	O	**Receive Overhead Data Output Interface - output/Receive HDLC Controller Data Bus - Bit 6 output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOH:** All overhead bits, which are received via the Receive Section of the XRT79L71 will be output via this output pin, upon the rising edge of RxOHClk. **High-Speed HDLC Controller Mode - RxHDLCDat_6:** This output pin along with RxHDLCDat_[5:0] and RxHDLCDat_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
A7	RxOHClk/ RxHDLCClk	O	**Receive Overhead Data Output Interface - clock/Receive HDLC Controller - Clock output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHClk:** The XRT79L71 will output the overhead bits within the incoming DS3 or E3 frames via the RxOH output pin, upon the falling edge of this clock signal. As a consequence, the user's local terminal equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *This clock signal is always active.* **High-Speed HDLC Controller Mode - RxHDLCClk:** This output pin functions as the Receive HDLC Controller Data bus clock output. The Receive HDLC Controller block outputs the contents of all received HDLC frames via the Receive HDLC Controller Data bus (RxHDLCDat_[7:0]) upon the rising edge of this clock signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of this clock signal.

PIN #	NAME	TYPE	DESCRIPTION
A8	RxOHFrame/ RxHDLCDat_4	O	**Receive Overhead Data Interface - Framing Pulse indicator/Receive HDLC Controller Data Bus - Bit 4 output:** The function of this output pins depends upon whether the XRT79L71 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHFrame:** This output pin pulses "High" whenever the Receive Overhead Data Output Interface block outputs the first overhead bit of a new DS3 or E3 frame. **High-Speed HDLC Controller Mode - RxHDLCDat_4:** This output pin along with RxHDLCDat_[3:0] and RxHDLCDat_[7:5] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal.
B6	RxFrame	0	**Receive Boundary of DS3 or E3 Frame Output indicator:** The function of this output pin depends upon whether or not the XRT79L71 is operating in the Clear-Channel Framer/Nibble-Parallel Mode. **Clear-Channel Framer/Nibble-Parallel Mode:** The Receive Section of the XRT79L71 will pulse this output pin "High" for one nibble period, when the Receive Payload Data Output interface block is driving the very first nibble of a given DS3 or E3 frame, on the RxNib[3:0] output pins. **Clear-Channel Framer/Serial Mode:** The Receive Section of the XRT79L71 will pulse this output pin "High" for one bit period, when the Receive Payload Data Output interface block is driving the very first bit of a given DS3 or E3 frame, on the RxSer output pin. **All Other Modes:** The Receive Section of the XRT79L71 will pulse this output pin "High" when the Receive DS3/E3 Framer block is processing the first bit within a new DS3 or E3 frame.
D4	RxCellRxed	O	**Receive Cell Processor - Cell Received Indicator:** This output pin pulses "High" each time the Receive Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3/E3 Framer block. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM UNI Mode.*

PIN #	NAME	TYPE	DESCRIPTION
A5	RxPOH/ RxSer	O	**Receive PLCP Path Overhead Output pin/Receive Serial Output pin:** The function of this output depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP Mode or in the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH:** This output pin along with the RxPOHClk, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. For each PLCP frame, that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via this pin, is updated on the rising edge of the RxPOHClk output clock signal. The RxPOHFrame pin will pulse "High" whenever the first bit of the Z6 byte is being output via this output pin. **Clear-Channel Framer Mode - RxSer:** If the XRT79L71 is configured to operate in the Clear-Channel Framer/Serial Mode, then the chip will output all received data, via this output pin. This output signal will be updated upon the rising edge of RxClk. ***NOTE:*** *The user should either configure the XRT79L71 to operate in the Gapped-Clock Mode, or validate the sampling of each bit from the RxSer output with the state of RxOHInd' output pin, in order to prevent the local terminal equipment from sampling overhead bits.* This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP or the Clear-Channel Framer/Serial Mode. This pin is inactive for all remaining modes of operation.

PIN #	NAME	TYPE	DESCRIPTION
A6	RxPOH_Clk/ RxClk/ RxNibClk	O	**Receive PLCP Path Overhead Serial Port Clock output/Receive Nibble-Parallel Output port clock/Receive Serial Clock output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP Mode or the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH_Clk:** This output clock pin along with RxPOH, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. All POH (Path Overhead) data that is output via the RxPOH output pin is updated on the rising edge of this clock signal. ***NOTE:*** *This output signal is inactive if the XRT79L71 has been configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer Mode - RxClk:** This output pin is active whenever the XRT79L71 has been configured to operate in either the Serial or Nibble Parallel Mode, as is described below.Clear-Channel Framer/Serial Mode - RxClkIn this serial mode, this output is a 44.736MHz clock output signal (for DS3 applications) or 34.368MHz clock output signal (for E3 applications). The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of this clock signal. The user is advised to design (or configure) the local terminal equipment to sample the RxSer data, upon the falling edge of this clock signal. **Clear-Channel Framer/Nibble-Parallel Mode - RxNibClk:** In the Nibble-Parallel Mode, the XRT79L71 will derive this clock signal from the RxLineClk signal. The XRT79L71 will pulse this clock signal 1176 times for each inbound DS3 frame or 1074 times for each inbound E3/ITU-T G.832 frame or 384 times for each inbound E3/ITU-T G.751 frame. The Receive Payload Data Output Interface block will update the data on the RxNib[3:0] output upon the falling edge of this clock signal. The user is advised to design (or configure) the local terminal equipment to sample the data on the RxNib[3:0] output pins, upon the rising edge of this clock signal.
C4	RxPOHFrame	O	**Receive PLCP Frame POH Serial Output Port - Frame Indicator:** This output pin along with the RxPOH RxPOHClk and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. This output pin provides framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing "High" whenever the first bit of the Z6 byte is being output via the RxPOH output pin. This pin is "Low" at all other times during this PLCP POH Framing cycle. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the ATM/PLCP Modes.*

PIN #	NAME	TYPE	DESCRIPTION
C6	RxPFrame/ RxOHInd	O	**Receive PLCP Frame Indicator/Receive Overhead Indicator Output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM/PLCP, the Clear-Channel Framer/Serial or the Clear-Channel Framer/Nibble-Parallel Modes. **ATM/PLCP Mode - RxPFrame:** This output pin pulses "High" when the Receive PLCP Processor is receiving the last bit of a PLCP frame. ***NOTE:*** *This output pin is inactive if the XRT79L71 is configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer/Serial Mode - RxOHInd:** This output pin pulses "High" for one bit-period whenever an overhead bit is being output via the RxSer output pin, by the Receive Payload Data Output Interface block. ***NOTE:*** *If the user configures the XRT79L71 to operate in the Gapped-Clock Mode, then this output pin will provide a demand clock to the local terminal equipment. In the Gapped-Clock Mode, this output pin will only provide a clock pulse, whenever a payload bit is being output via the RxSer output pin. This output pin will NOT generate a clock pulse, whenever an overhead is being output via the RxSer output pin.* **Clear-Channel Framer/Nibble-Parallel - RxOHInd:** This output pin pulse "High" for one nibble-period whenever an overhead nibble is being output via the RxNib[3:0] output pins by the Receive Payload Data Output Interface block. ***NOTE:*** *The purpose of this output pin is to alert the local terminal equipment that an overhead bit (or nibble) is being output via the RxSer or RxNib[3:0] output pins and that this data should be ignored.*
C3	RxGFC/ RxIdle	O	**Receive GFC Nibble Field - Output Pin/Receive Idle Sequence Indicator:** The function of this output pin depends upon whether the XRT79L71 is operating in the ATM Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - RxGFC:** This pin, along with the RxGFCClk and the RxGFCMSB pins form the Receive GFC Nibble-Field serial output port. This pin will serially output the contents of the GFC Nibble field of each cell that is processed via the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signal. The MSB of each GFC value is designated by a pulse at the RxGFCMSB output pin. **High-Speed HDLC Controller Mode - RxIdle:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive HDLC Controller output Data bus (RxHDLCDat_[7:0]). ***If RxIdle = "High":*** The Receive HDLC Controller block will drive this output pin "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDat[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received an ABORT sequence.

PIN #	NAME	TYPE	DESCRIPTION
A1	RxGFCClk	O	**Received GFC Nibble Serial Output Port Clock Signal:** This output pin functions as a part of the Receive GFC Nibble-Field Serial Output Port, also consisting of the RxGFC and RxGFCMSB pins. This pin provides a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin. ***NOTE:*** *This output pin is only active if the XRT79L71 is operating in the ATM UNI Mode.*
B1	RxGFCMSB	O	**Receive GFC Nibble Field - MSB Indicator:** This output pin functions as a part of the Receive GFC Nibble Field Serial Output port which also consists of the RxGFC and RxGFCClk pins. This pin pulses "High" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin. ***NOTE:*** *This output pin is only active if the XRT79L71 is operating in the ATM UNI Mode.*
H1	RxUClav/RxPPA	O	**Receive UTOPIA - Cell Available/Receive POS-PHY Interface - Packet Available:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClav:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the Rx FIFO has some ATM cell data that needs to be read by the ATM Layer Processor. This signal is asserted if the RxFIFO contains at least one full cell of data. This signal toggle "Low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. ***Multi-PHY Operation:*** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the RxClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins match that with the Receive UTOPIA Address Register. Afterwards, this output pin will behave in accordance with the cell-level handshake mode. **PPP Mode - RxPPA:** The XRT79L71 will drive this output pin "High" whenever a programmable number of bytes are available to be read from the RxFIFO.
K2	RxUClkO/ RxPClkO	O	**Receive UTOPIA Interface Clock/Receive POS-PHY Interface Clock Output:** This clock output signal is derived from an internal PLL.
L3	RxUClk/ RxPClk	I	**Receive UTOPIA Interface Clock Input/Receive POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L71 is operating in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClk:** The byte (or word) data, on the Receive UTOPIA Data bus (RxUData[15:0]) is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz. **PPP Mode - RxPClk:** This byte (or word) data, on the Receive POS-PHY Data Bus (RxPData[15:0]) is updated on the rising edge of this signal. The Receive POS-PHY Interface can be clocked at rates up to 50MHz.

PIN #	NAME	TYPE	DESCRIPTION
L2	RxPERR	O	**Receive POS-PHY Interface - Error Indicator:** This output pin indicates whether or not the Receive POS-PHY Interface has detected an error in the inbound PPP Packet. This output pin toggles "High" if the Receive Section of the XRT79L71 detects an FCS Error, an ABORT sequence or a Runt Packet. ***NOTE:*** *This output pin is only valid if the XRT79L71 has been configured to operate in the PPP Mode.*
K4	RxTSX/ RxPSOF	O	**Receive - Start of Transfer/Receive - Start of PPP Packet in Chunk Mode:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the Packet Mode or Cell-Chunk Mode. **Packet Mode - RxTSX:** The XRT79L71 pulses this output pin "High" when an inband port address is present on the RxPData[7:0] bus. When this output pin is "High", the value of RxPData[7:0] is the address value of the RxFIFO to be selected. Subsequent read operations, from RxPData[15:0] will be from the RxFIFO corresponding to this inband address. **Chunk Mode - RxPSOF:** The XRT79L71 pulses this output pin "High" in order to indicate that the first byte (or word) of a given Packet is placed on the RxPData[15:0] pins. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
H4	$\overline{\text{RxUEN}}$/ $\overline{\text{RxPEN}}$	I	**Receive UTOPIA Interface - Output Enable/Receive POS-PHY Interface - Output Enable:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or PPP mode. **ATM UNI Mode - $\overline{\text{RxUEN}}$:** This active-low input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is "High" (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk. **PPP Mode - $\overline{\text{RxPEN}}$:** This active-low input signal is used to control the drivers of the Receive POS-PHY Data Bus. When this signal is "High" (negated) then the Receive POS-PHY Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive POS-PHY Data bus on the very next rising edge of RxPClk.
H2	RxUSoC/ RxPSOP	O	**Receive UTOPIA Interface - Start of Cell Indicator/Receive POS-PHY Interface - Start of Packet Indicator:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - RxUSoC:** This output pin allows the ATM Layer Processor to determine the boundaries of the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0]. **PPP Mode - RxPSOP:** This output pin allows the Link Layer Processor to determine the boundaries of the PPP packets that are output via the Receive POS-PHY Data Bus. The Receive POS-PHY Interface block will assert this signal when the first byte (or word) of a new packet is present on the Receive POS-PHY Data Bus, RxP-Data[15:0].

PIN #	NAME	TYPE	DESCRIPTION
H3	RxUPrty/ RxPPrty	O	**Receive UTOPIA Interface - Parity Output pin/Receive POS-PHY Interface - Parity Output:** The function of this output pin depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or the PPP Modes. **ATM UNI Mode - RxUPrty:** The Receive UTOPIA interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus **PPP Mode - RxPPrty:** The Receive POS-PHY Interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive POS-PHY Data Bus. This odd parity value will be output on this pin, which the corresponding byte (or word) is present on the Receive POS-PHY Data Bus.
K3	RxPEOP	O	**Receive POS-PHY Interface - End of Packet:** The XRT79L71 drives this output pin "High" whenever the last byte of a given Packet is being output via the RxPData[15:0] data bus. ***NOTES:*** *1. This output pin is only valid when the XRT79L71 is configured to operate in the PPP Mode.* *2. This output pin is only valid when the Receive POS-PHY Interface - Read Enable Output pin.*
N2	RxPDVAL	O	**Receive POS-PHY Interface Signal Valid Indicator:** This output signal indicates whether or not the Receive POS-PHY Interface signals (e.g., PRData[15:0], RxPSOP, RxPEOP, RxPPrty, RxPERR) are valid. This output pin will be driven "High", when these signals are valid. Conversely, this output pin will be driven "Low" when these signals are NOT valid. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*
J1 J2 J3 J4 K1	RxAddr_0 RxAddr_1 RxAddr_2 RxAddr_3 RxAddr_4	I	**Receive UTOPIA Address Bus input MSB:** These input pins functions as the Receive UTOPIA Address bus inputs. These input pins are only active when the Framer/UNI device is operating in the ATM UNI Mode. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxClk signal. The contents of this address bus are compared with the value stored in the Rx UT Address Register (Address = 0x6C). If these two values match, then the UNI will inform the ATM Layer Processor on whether or not it has any new ATM cells to be read from the RxFIFO by driving the RxClav output to the appropriate level. If these two address values do not match, then the UNI will not respond to the ATM Layer Processor and will keep its RxClav output signal tri-stated.

PIN #	NAME	TYPE	DESCRIPTION
G2 G1 F1 G3 F2 E1 G4 F3 E2 D1 F4 E3 D2 C1 E4 D3	RxUData_0/ RxPData_0 RxUData_1/ RxPData_1 RxUData_2/ RxPData_2 RxUData_3/ RxPData_3 RxUData_4/ RxPData_4 RxUData_5/ RxPData_5 RxUData_6/ RxPData_6 RxUData_7/ RxPData_7 RxUData_8/ RxPData_8 RxUData_9/ RxPData_9 RxUData_10/ RxPData_10 RxUData_11/ RxPData_11 RxUData_12/ RxPData_12 RxUData_13/ RxPData_13 RxUData_14/ RxPData_14 RxUData_15/ RxPData_15	O	**Receive UTOPIA Data Bus Input/Receive POS-PHY Data Bus Output pins:** The function of these output pins depends upon whether the XRT79L71 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - RxUData[15:0]:** These output pins function as the Receive UTOPIA Data Bus. ATM cell data that has been received from the Remote Terminal Equipment is output on the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor. **PPP Mode - RxPData[15:0]:** These output pins function as the Receive POS-PHY Data Bus output pins. PPP Packet data that has been received from the Remote Terminal Equipment is output on the Receive POS-PHY Data Bus, where it can be reads and processed by the Link Layer Processor.
L1	RxMod	O	**Receive PPP Data Bus - Modulus Indicator:** The XRT79L71 will indicate the number of valid packet octets that are being read out of the RxPData[15:0] output pins. The XRT79L71 will drive this output pin "Low" when both bytes of the RxPData[15:0] data bus consists of valid packet data. Conversely, the XRT79L71 will drive this output pin "High" when only the upper byte of the RxPData[15:0] data bus consists of valid packet data. The Link Layer Processor is expected to validate all packet data that it reads out of the RxPData[15:0] output pins by also reading the state of this output pin. ***NOTE:*** *This output pin is only active if the XRT79L71 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT LINE SIDE SIGNALS			
R15	TxON	I	**Transmit Driver ON - Channel n:** This input pin is used to either enable or disable the Transmit Output Driver of the XRT79L71. "Low" - Disables the XRT79L71 Transmit Output Driver. In this setting, the TTIP and TRING output pins will be tri-stated. "High" - Enables the XRT79L71 Transmit Output Driver. In this setting, the TTIP and TRING output pins will be enabled. ***NOTES:*** *1. Whenever the transmitters are turned off , the TTIP and TRING output pins will be tri-stated.* *2. These pins are internally pulled high.*
P16 M16	DS3CLK E3CLK	I	**Transmit Clock Input:** These input pins function as the timing source for the XRT79L71 Transmit Section. ***NOTE:*** *The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications) or a 34.368MHz ± 20 ppm clock signal (for E3 applications).*
T11	TTIP	O	**Transmit Output - Positive Polarity Signal:** This output pin, along with the TRING output pin, function as the Transmit DS3/E3 output signal drivers for the XRT79L71. The user is expected to connect this signal and the TRING output signal to a 1:1 transformer. Whenever the Transmit Section of the XRT79L71 generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a "higher-voltage" than the TRING output pin. Conversely, whenever the Transmit Section of the XRT79L71 generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a "lower-voltage" than the TRING output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the TxON input pin (or bit-field) to "0".*
T10	TRING	O	**Transmit Output - Negative Polarity Signal:** This output pin along with the TTIP output pin, functions as the Transmit DS3/E3 output signal drivers for the XRT79L71. The user is expected to connect this signal and the TTIP output signal to a 1:1 transformer. Whenever the Transmit Section of the XRT79L71 generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a "lower-voltage" than the TTIP output pin. Conversely, whenever the Transmit Section of the XRT79L71 generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a "higher-voltage" than the TTIP output pin. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the TxON input pin (or bit-field) to "0".*

PIN #	NAME	TYPE	DESCRIPTION
P10	MTIP	I	**Transmit Drive Monitor Input pin - Positive Polarity Input:** This input pin along with MRING functions as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect this particular pin to the TTIP output pin via a 274 ohm series resistor. Similarly, the user MUST also connect the MRING input pin to the TRING output pin via a 274 ohm series resistor. The MTIP and MRING input pins will continuously monitor the Transmit Output line signal via the TTIP and TRING output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMO output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. This input pin is inactive if the user choose to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the user is operating the XRT79L71 in the Host Mode.*
P11	MRING	I	**Transmit Drive Monitor Input pin - Negative Polarity Input:** This input pin along with MTIP functions as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect this particular input pin to the TRING output pin via a 274 ohm series resistor. Similarly, the user MUST also connect the MTIP input pin to the TTIP output pin via a 274 ohm series resistor. The MTIP and MRING input pins will continuously monitor the Transmit Output line signal via the TTIP and TRING output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMO output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. This input pin is inactive if the user chooses to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the user is operating the XRT79L71 in the Host Mode.*

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE LINE SIDE SIGNALS			
R14	RTIP	I	**Receive Input - Positive Polarity Signal:** This input pin, along with the RRING input pin, functions as the Receive DS3/E3/STS-1 Line input signal receiver of the XRT79L71. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a "higher-voltage" than the RRING input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a "lower-voltage" than the RRING input pin.

PIN #	NAME	TYPE	DESCRIPTION
R13	RRING	I	**Receive Input - Negative Polarity Signal:** This input pin, along the RTIP input pin, functions as the Receive DS3/E3/STS-1 Line input signal receiver for the XRT79L71. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "lower-voltage" than the RTIP input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "higher-voltage" than the RTIP input pin.
K16	CLKOUT	O	**Receive (Recovered) Clock Output:** This output pin functions as the Receive or recovered clock signal. All Receive (or recovered) data will output via the RTIP and RRING outputs upon the user-selectable edge of this clock signal.

PIN #	NAME	TYPE	DESCRIPTION
VDD PINS			
G7 G8 G9 G10 K7 K8 K9 K10 H14 N14			3.3V Power Supply Pins
R16	CLKVDD		3.3V Clock Power Supply Pin
T16	JAAVDD		3.3V Jitter Attenuator Analog Power Supply Pin
N13	OVDD		3.3V Output Power Supply Pin
R12	REFAVDD		3.3V Reference Analog Power Supply Pin
T13	RXAVDD		3.3V Receive Analog Power Supply Pin
N11	TXDVDD		3.3V Transmit Digital Power Supply Pin
T12	TXAVDD		3.3V Transmit Analog Power Supply Pin

PIN #	NAME	TYPE	DESCRIPTION
GND PINS			
H7 H8 H9 H10 J7 J8 J9 J10 H15 N15			Ground Pins
N16	CLKGND		3.3V Clock Ground Pin
T15	JAAGND		3.3V Jitter Attenuator Analog Ground Pin
M13	OGND		3.3V Output Ground Pin
P12	REFAGND		3.3V Reference Analog Ground Pin
T14	RXAGND		3.3V Receive Analog Ground Pin
N10	TXDGND		3.3V Transmit Digital Ground Pin
N12	TXAGND		3.3V Transmit Analog Ground Pin

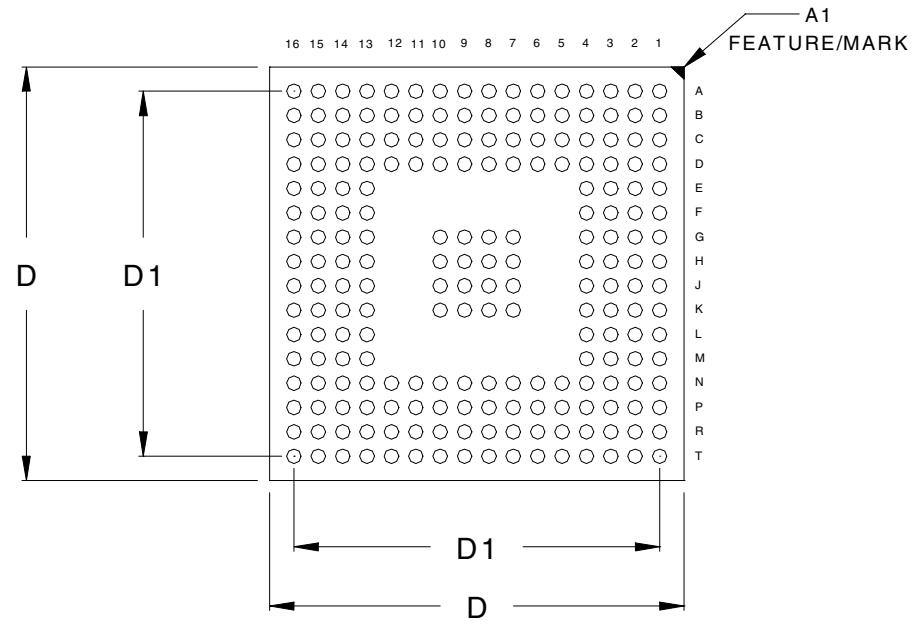
PIN #	NAME	TYPE	DESCRIPTION
NOT CONNECTED PINS			
R11			No Connect Pin

ORDERING INFORMATION

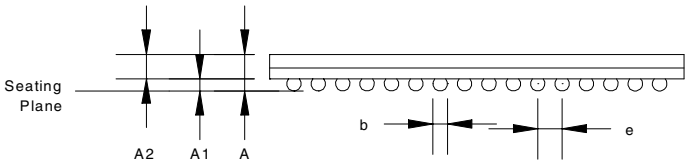
PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L71IB	17X17 mm 208 Ball Shrink Thin Ball Grid Array	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS

208 SHRINK THIN BALL GRID ARRAY (17.0 MM X 17.0 MM, STBGA)



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.047	0.067	1.20	1.70
A1	0.010	0.022	0.25	0.55
A2	0.031	0.043	0.80	1.10
D	0.661	0.677	16.80	17.20
D1	0.591 BSC		15.00 BSC	
b	0.018	0.022	0.45	0.55
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	07/18/02	1st release of the XRT99L00 mkII.0 preliminary data sheet.
P1.0.1	02/12/03	Added package outline and pin-out diagram.
P1.0.2	05/03	Added Pin Descriptions