



Single Supply / Low Power / 256-tap / SPI bus

X9251

Quad Digitally-Controlled (XDCP™) Potentiometer

FEATURES

- Quad—Four Separate Potentiometers
- 256 resistor taps/pot—0.4% resolution
- SPI Serial Interface for write, read, and transfer operations of the potentiometer
- Wiper Resistance, 100Ω typical @ $V_{CC} = 5V$
- 4 Nonvolatile Data Registers for Each Potentiometer
- Nonvolatile Storage of Multiple Wiper Positions
- Power On Recall. Loads Saved Wiper Position on Power Up.
- Standby Current < 5μA Max
- V_{CC} : 2.7V to 5.5V Operation
- 50KΩ, 100KΩ versions of End to End Resistance
- 100 yr. Data Retention
- Single Supply version of X9250
- Endurance: 100,000 Data Changes per Bit per Register
- 24-Lead SOIC, 24-Lead TSSOP, 24-Lead XBGA
- Low Power CMOS

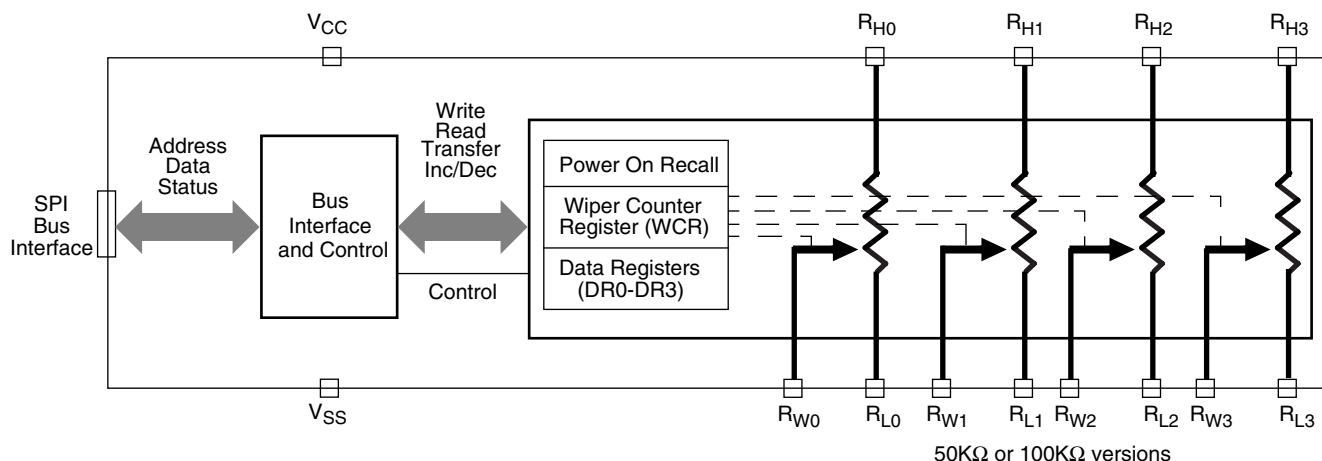
DESCRIPTION

The X9251 integrates 4 digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

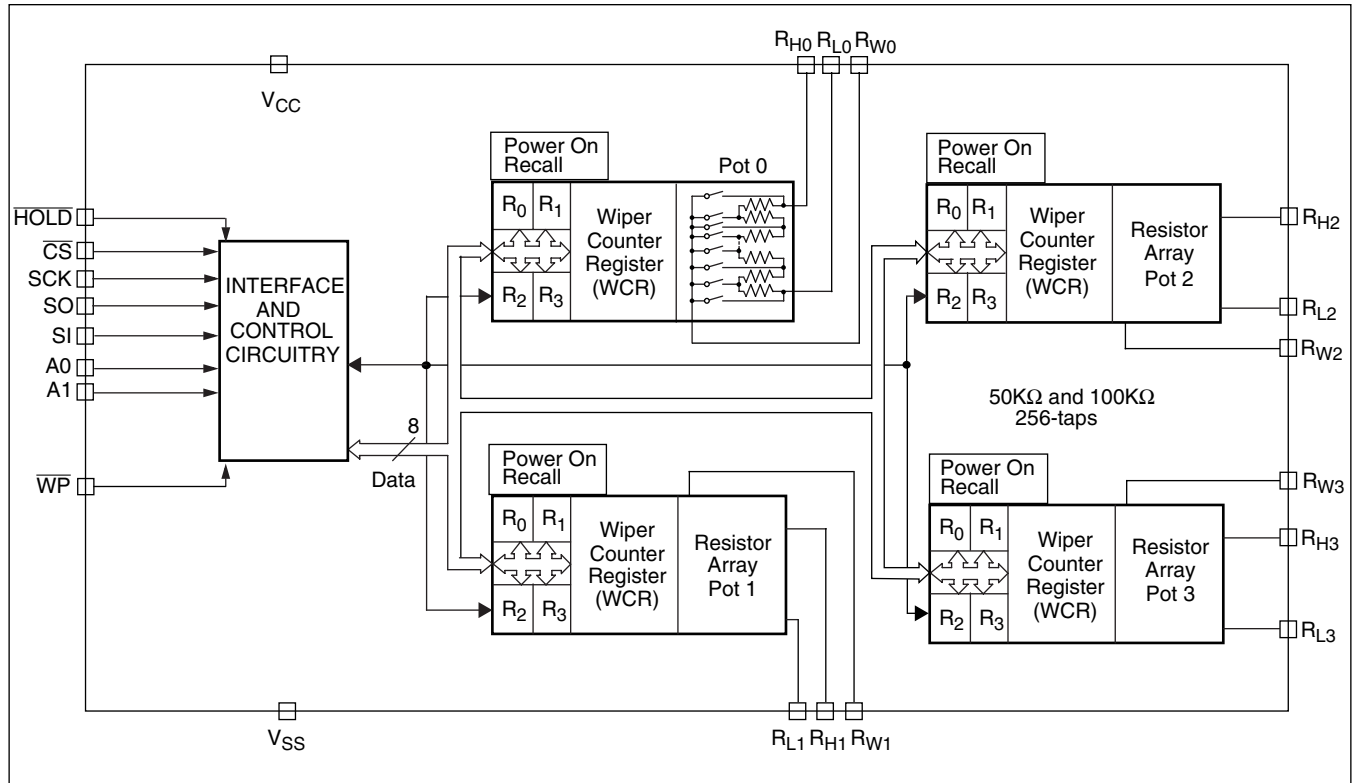
The digital controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four nonvolatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Powerup recalls the contents of the default Data Register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

FUNCTIONAL DIAGRAM



DETAILED FUNCTIONAL DIAGRAM



CIRCUIT LEVEL APPLICATIONS

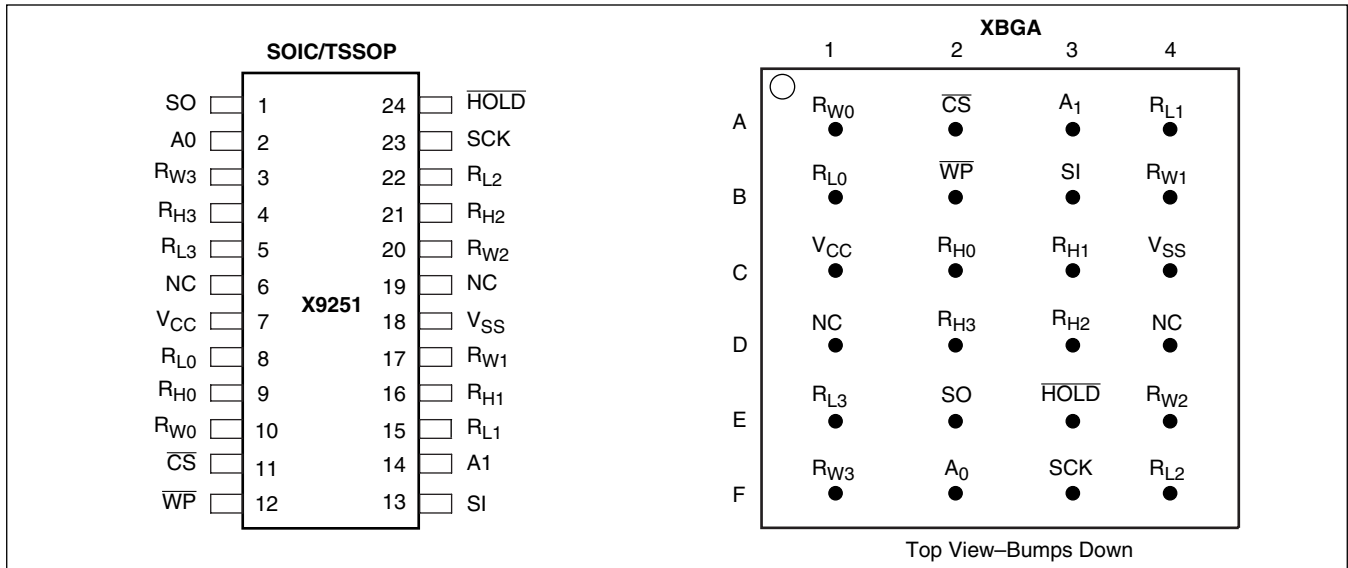
- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

X9251

PIN CONFIGURATION



PIN ASSIGNMENTS

| Pin (SOIC) | Pin (XBGA) | Symbol | Function |
|------------|------------|-----------------|--|
| 1 | E2 | SO | Serial Data Output for SPI bus |
| 2 | F2 | A0 | Device Address for SPI bus. (See Note 1) |
| 3 | F1 | R _{W3} | Wiper Terminal for Potentiometer 3. |
| 4 | D2 | R _{H3} | High Terminal for Potentiometer 3. |
| 5 | E1 | R _{L3} | Low Terminal for Potentiometer 3. |
| 7 | C1 | V _{CC} | System Supply Voltage |
| 8 | B1 | R _{L0} | Low Terminal for Potentiometer 0. |
| 9 | C2 | R _{H0} | High Terminal for Potentiometer 0. |
| 10 | A1 | R _{W0} | Wiper Terminal for Potentiometer 0. |
| 11 | A2 | CS | Device Address for SPI bus. |
| 12 | B2 | WP | Hardware Write Protect |
| 13 | B3 | SI | Serial Data Input for SPI bus |
| 14 | A3 | A1 | Device Address for SPI bus. (See Note 1) |
| 15 | A4 | R _{L1} | Low Terminal for Potentiometer 1. |
| 16 | C3 | R _{H1} | High Terminal for Potentiometer 1. |
| 17 | B4 | R _{W1} | Wiper Terminal for Potentiometer 1. |
| 18 | C4 | V _{SS} | System Ground |
| 20 | E4 | R _{W2} | Wiper Terminal for Potentiometer 2. |
| 21 | D3 | R _{H2} | High Terminal for Potentiometer 2. |
| 22 | F4 | R _{L2} | Low Terminal for Potentiometer 2. |
| 23 | F3 | SCK | Serial Clock for SPI bus |
| 24 | E3 | HOLD | Device select. Pause the SPI serial bus. |
| 6, 19 | D1, D4 | NC | No Connect |

Note 1: A0-A1 device address pins must be tie to a logic level.

X9251

PIN DESCRIPTIONS

Bus Interface Pins

SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9251.

HOLD ($\overline{\text{HOLD}}$)

$\overline{\text{HOLD}}$ is used in conjunction with the $\overline{\text{CS}}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{\text{HOLD}}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{\text{HOLD}}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{\text{HOLD}}$ should be held HIGH at all times.

DEVICE ADDRESS (A1 - A0)

The address inputs are used to set the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9251. Device pins A1-A0 must be tie to a logic level which specify the internal address of the device, see Figures 2, 3, 4, 5 and 6.

CHIP SELECT ($\overline{\text{CS}}$)

When $\overline{\text{CS}}$ is HIGH, the X9251 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{\text{CS}}$ LOW enables the X9251, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{\text{CS}}$ is required prior to the start of any operation.

Potentiometer Pins

R_H , R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R_H and R_L such that R_{H0} and R_{L0} are the terminals of POT 0 and so on.

R_W

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R_W such that R_{W0} is the terminals of POT 0 and so on.

Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

No CONNECT

No connect pins should be left floating. This pins are used for Xicor manufacturing and testing purposes.

HARDWARE WRITE PROTECT INPUT ($\overline{\text{WP}}$)

The $\overline{\text{WP}}$ pin when LOW prevents nonvolatile writes to the Data Registers.

X9251

PRINCIPLES OF OPERATION

Serial Interface

The X9251 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. \overline{CS} must be LOW and the \overline{HOLD} and \overline{WP} pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Array Description

The X9251 is comprised of a resistor array (see Figure 1). The array contains the equivalent of 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

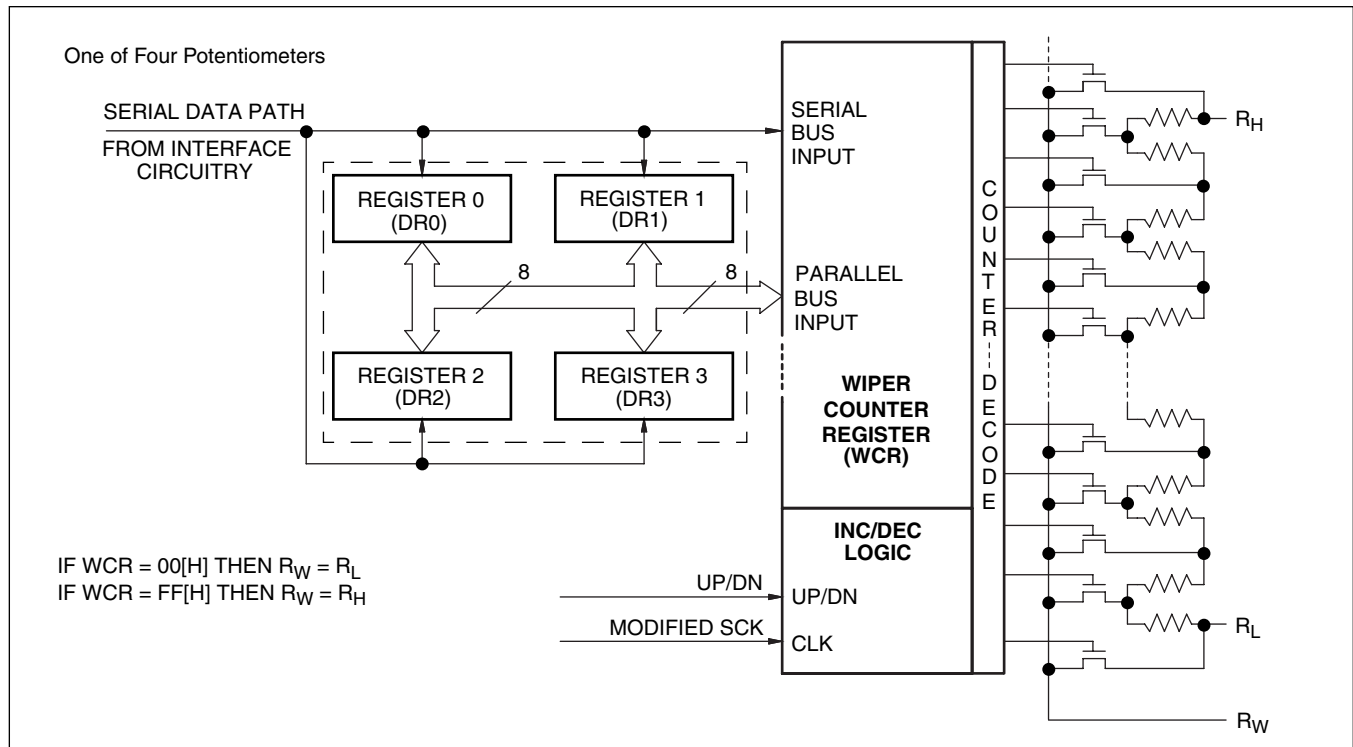
At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8-bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (see Table 1).

Power Up and Down Recommendations.

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H , V_L , and V_W , i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} ramp rate specification is always in effect.

Figure 1. Detailed Potentiometer Block Diagram



X9251

DEVICE DESCRIPTION

Wiper Counter Register (WCR)

The X9251 contains four Wiper Counter Registers, one for each DCP potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (see Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The wiper counter register is a volatile register; that is, its contents are lost when the X9251 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

Data Registers (DR)

The potentiometer has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0~255).

Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

- When WIP=1, indicates that high-voltage write cycle is in progress.
- When WIP=0, indicates that no high-voltage write cycle is in progress.

Table 1. Wiper counter Register, WCR (8-bit), WCR[7:0]: Used to store the current wiper position (Volatile, V).

| WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |
|-------|------|------|------|------|------|------|-------|
| V | V | V | V | V | V | V | V |
| (MSB) | | | | | | | (LSB) |

Table 2. Data Register, DR (8-bit), DR[7:0]: Used to store wiper positions or data (Nonvolatile, NV).

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| NV | NV | NV | NV | NV | NV | NV | NV |
| MSB | | | | | | | LSB |

X9251

DEVICE DESCRIPTION

Instructions

IDENTIFICATION BYTE (ID AND A)

The first byte sent to the X9251 from the host, following a CS going HIGH to LOW, is called the Identification Byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device id for the X9251; this is fixed as 0101[B] (refer to Table 3).

The AD[3:0] bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A3-A0 input pins. The slave address is externally specified by the user. The X9251 compares the serial data stream with the address input state; a

successful compare of both address bits is required for the X9251 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3-A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

INSTRUCTION BYTE (I[3:0])

The next byte sent to the X9251 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCP. The least two significant bits point to one of four Wiper Counter Registers or Pots. The format is shown below in Table 4.

Table 3. Identification Byte Format

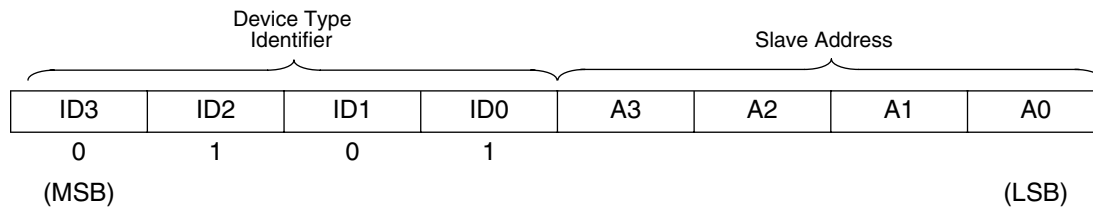
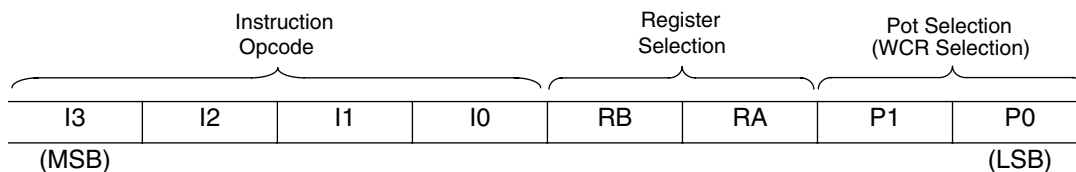


Table 4. Instruction Byte Format



DEVICE DESCRIPTION

Instructions

Four of the ten instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,
- **Read Data Register** – read the contents of the selected Data Register;
- **Write Data Register** – write a new value to the selected Data Register.
- **Read Status** - This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the three byte instructions is illustrated in Figure 3. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL} . A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (see Figure 5).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9251; either between the host and one

of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (see Figures 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9251 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal. A detailed illustration of the sequence and timing for this operation are shown. See Instruction format for more details.

Figure 2. Two-Byte Instruction Sequence

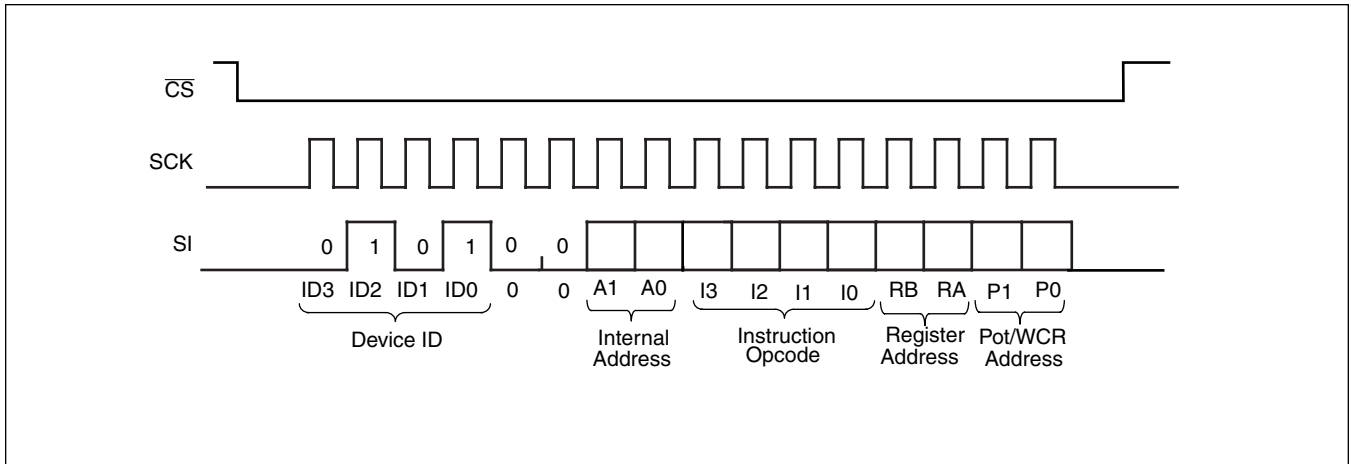


Figure 3. Three-Byte Instruction Sequence SPI (Write) Interface

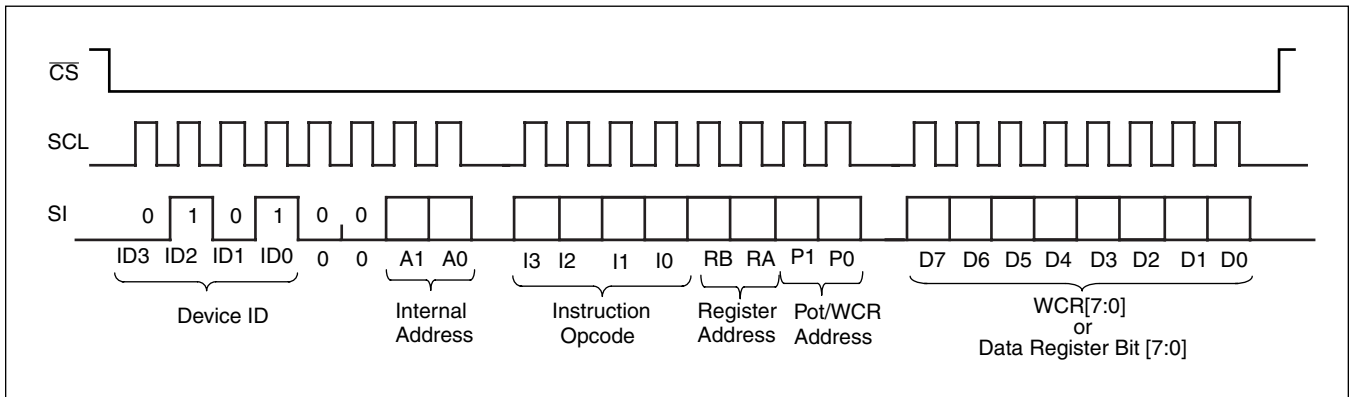


Figure 4. Three-Byte Instruction Sequence (Read) SPI Interface

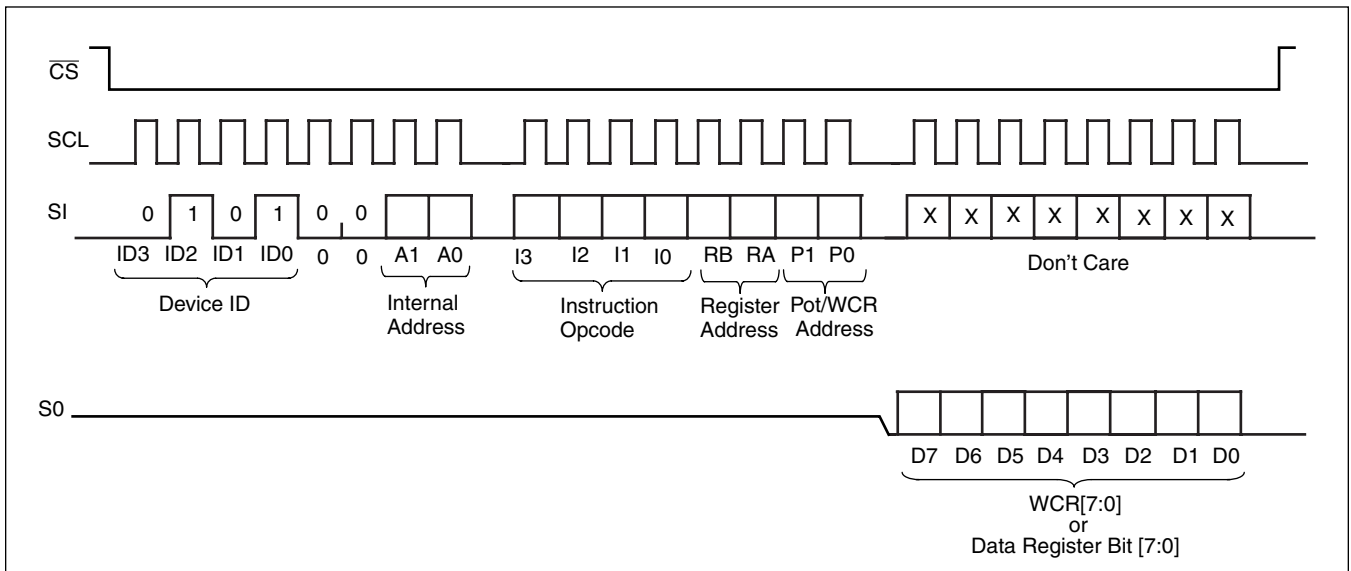


Figure 5. Three-Byte Instruction Sequence (Read Status Register)

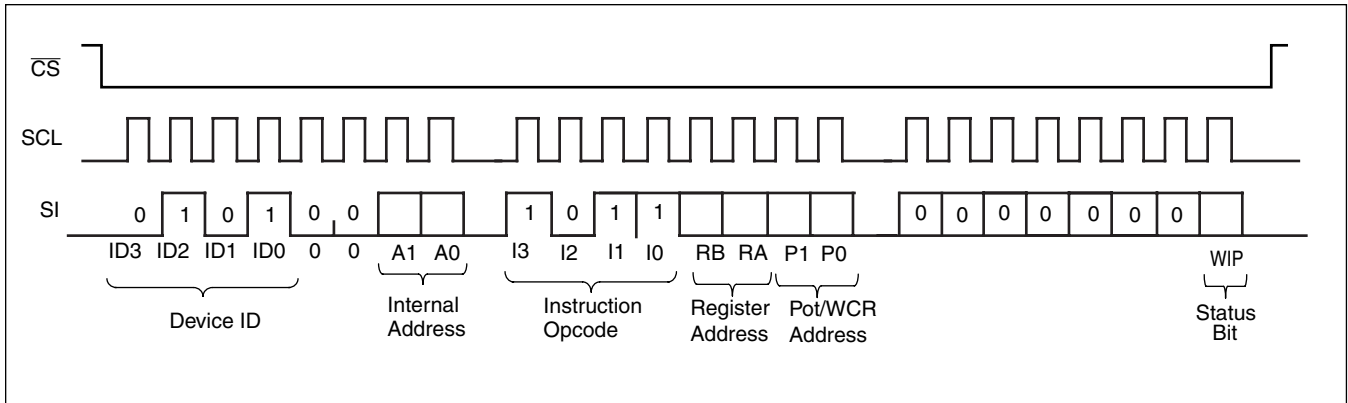


Figure 6. Increment/Decrement Instruction Sequence

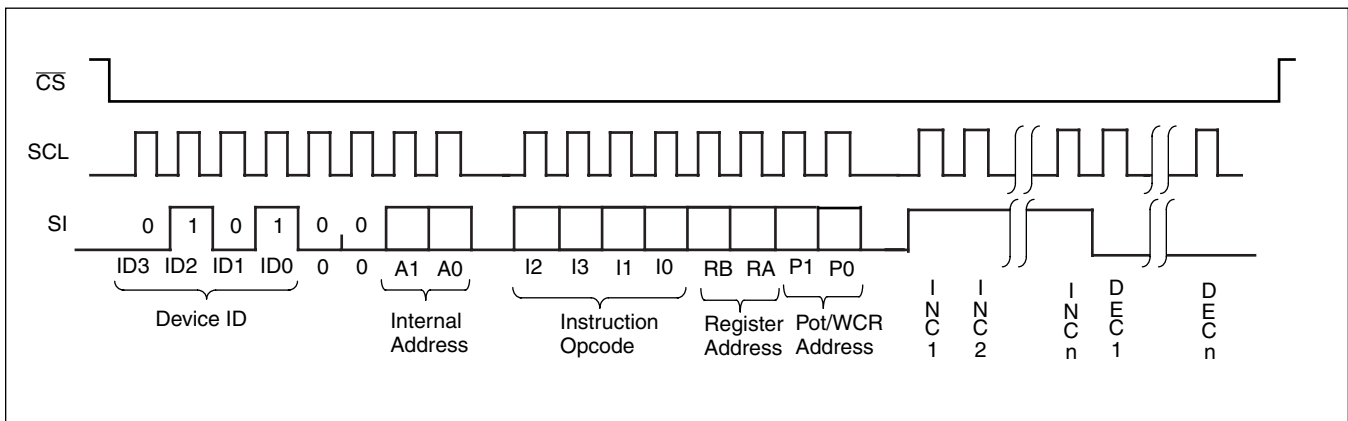
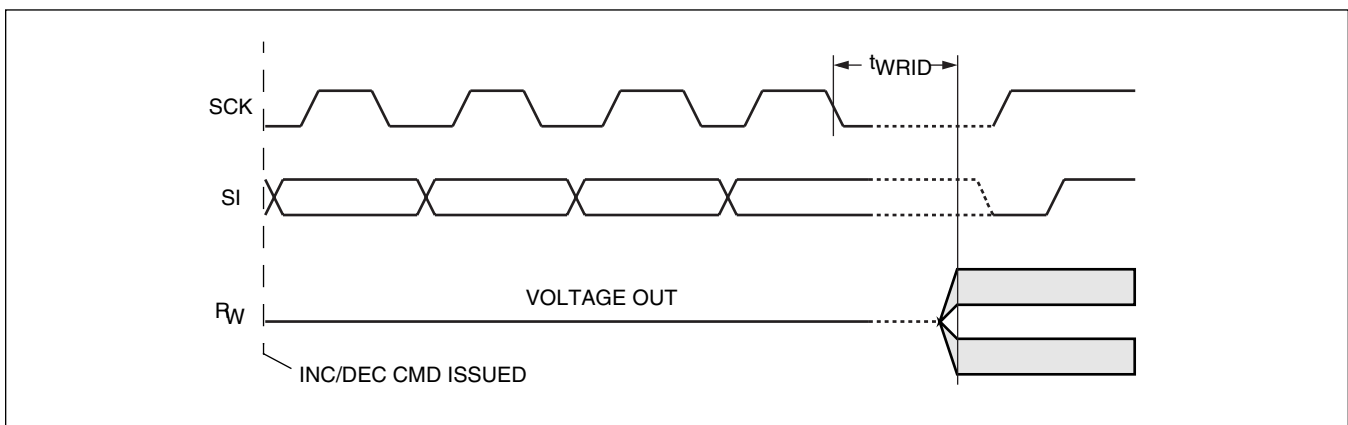


Figure 7. Increment/Decrement Timing Limits



X9251

Table 5. Instruction Set

| Instruction | Instruction Set | | | | | | | | Operation |
|--|-----------------|----|----|----|-----|-----|-----|-----|---|
| | I3 | I2 | I1 | I0 | RB | RA | P1 | P0 | |
| Read Wiper Counter Register | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 | 1/0 | Read the contents of the Wiper Counter Register pointed to by P1-P0 |
| Write Wiper Counter Register | 1 | 0 | 1 | 0 | 0 | 0 | 1/0 | 1/0 | Write new value to the Wiper Counter Register pointed to by P1-P0 |
| Read Data Register | 1 | 0 | 1 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | Read the contents of the Data Register pointed to by P1-P0 and RB-RA |
| Write Data Register | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | Write new value to the Data Register pointed to by P1-P0 and RB-RA |
| XFR Data Register to Wiper Counter Register | 1 | 1 | 0 | 1 | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Data Register pointed to by P1-P0 and RB-RA to its associated Wiper Counter Register |
| XFR Wiper Counter Register to Data Register | 1 | 1 | 1 | 0 | 1/0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Wiper Counter Register pointed to by P1-P0 to the Data Register pointed to by RB-RA |
| Global XFR Data Registers to Wiper Counter Registers | 0 | 0 | 0 | 1 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Data Registers pointed to by RB-RA of all four pots to their respective Wiper Counter Registers |
| Global XFR Wiper Counter Registers to Data Register | 1 | 0 | 0 | 0 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB-RA of all four pots |
| Increment/Decrement Wiper Counter Register | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 | 1/0 | Enable Increment/decrement of the Control Latch pointed to by P1-P0 |

Note: 1/0 = data is one or zero

X9251

INSTRUCTION FORMAT

Read Wiper Counter Register (WCR)

| \overline{CS} Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Wiper Position (Sent by X9251 on SO) | | | | | | | | \overline{CS} Rising Edge |
|------------------------------------|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|------------------|---|---|---|---|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | W C R 7 | W C R 6 | W C R 5 | W C R 4 | W C R 3 | W C R 2 | W C R 1 | W C R 0 | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | |

Write Wiper Counter Register (WCR)

| \overline{CS} Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Data Byte (Sent by Host on SI) | | | | | | | | \overline{CS} Rising Edge |
|------------------------------------|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|------------------|---|---|---|-----------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | W C R 7 | W C R 6 | W C R 5 | W C R 4 | W C R 3 | W C R 2 | W C R 1 | W C R 0 | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | |

Read Data Register (DR)

| \overline{CS} Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | Data Byte (Sent by X9271 on SO) | | | | | | | | \overline{CS} Rising Edge |
|------------------------------------|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-------------------------|----|----|----|------------------------------------|--------|--------|--------|--------|--------|--------|--------|-----------------------------------|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 1 | RB | RA | P1 | P0 | D 7 | D 6 | D 5 | D 4 | D 3 | D 2 | D 1 | D 0 | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 1 | RB | RA | P1 | P0 | | | | | | | | | |

Write Data Register (DR)

| \overline{CS} Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | Data Byte (Sent by Host on SI) | | | | | | | | \overline{CS} Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|------------------------------------|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-------------------------|----|----|----|-----------------------------------|--------|--------|--------|--------|--------|--------|--------|-----------------------------------|-----------------------------|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 0 | RB | RA | P1 | P0 | D 7 | D 6 | D 5 | D 4 | D 3 | D 2 | D 1 | D 0 | | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 0 | RB | RA | P1 | P0 | | | | | | | | | | |

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

| \overline{CS} Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR Addresses | | | | \overline{CS} Rising Edge |
|------------------------------------|---------------------------|---|---|---|---------------------|---|----|----|-----------------------|---|---|---|-----------------|----|---|---|-----------------------------------|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 0 | 1 | RB | RA | 0 | 0 | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 0 | 1 | RB | RA | 0 | 0 | |

X9251

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

| | | | | | | | | | | | | | | | | | | |
|---|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|--------------|----|---|---|--|-----------------------------|
| $\overline{\text{CS}}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR Addresses | | | | $\overline{\text{CS}}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 0 | RB | RA | 0 | 0 | | |

Transfer Wiper Counter Register (WCR) to Data Register (DR)

| | | | | | | | | | | | | | | | | | | |
|---|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|----------------------|----|---|---|--|-----------------------------|
| $\overline{\text{CS}}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | $\overline{\text{CS}}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 1 | 0 | RB | RA | 0 | 0 | | |

Transfer Data Register (DR) to Wiper Counter Register (WCR)

| | | | | | | | | | | | | | | | | | |
|---|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|----------------------|----|---|---|--|
| $\overline{\text{CS}}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | DR and WCR Addresses | | | | $\overline{\text{CS}}$ Rising Edge |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 1 | RB | RA | 0 | 0 | |

Increment/Decrement Wiper Counter Register (WCR)

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|---------------|---|---|---|---|-----|---|---|--|---|---|
| $\overline{\text{CS}}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Increment/Decrement (Sent by Master on SI) | | | | $\overline{\text{CS}}$ Rising Edge | | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 1 | 0 | X | X | 0 | 0 | I/D | I/D | . | . | | . | . |

Read Status Register (SR)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|------------------------|---|---|---|------------------|---|----|----|--------------------|---|---|---|---------------|---|---|---|------------------------------------|---|---|---|---|---|---|---|--|---|---|---|---|---|
| $\overline{\text{CS}}$ Falling Edge | Device Type Identifier | | | | Device Addresses | | | | Instruction Opcode | | | | WCR Addresses | | | | Data Byte (Sent by X9251 on SO) | | | | | | | | $\overline{\text{CS}}$ Rising Edge | | | | | |
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 |

- Notes:**
- (1) "A1 ~ A0": stands for the device addresses sent by the master.
 - (2) WPx refers to wiper position data in the Counter Register
 - (2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
 - (3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

X9251

ABSOLUTE MAXIMUM RATINGS

Temperature under bias-65°C to +135°C
 Storage temperature-65°C to +150°C
 Voltage on SCK any address input
 with respect to V_{SS}-1V to +7V
 $\Delta V = | (V_H - V_L) |$ 5.5V
 Lead temperature (soldering, 10 seconds).....300°C
 I_W (10 seconds) ± 6 mA

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|------------|-------|-------|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |

| Device | Supply Voltage (V_{CC}) ⁽⁴⁾ Limits |
|-----------|---|
| X9251 | 5V $\pm 10\%$ |
| X9251-2.7 | 2.7V to 5.5V |

ANALOG CHARACTERISTICS (Over recommended industrial operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---------------|--|----------|-----------|----------|-------------------|--|
| | | Min. | Typ. | Max. | Units | |
| R_{TOTAL} | End to End Resistance | | 100 | | k Ω | T version |
| R_{TOTAL} | End to End Resistance | | 50 | | k Ω | U version |
| | End to End Resistance Tolerance | | | ± 20 | % | |
| | Power Rating | | | 50 | mW | 25°C, each pot |
| I_W | Wiper Current | | | ± 3 | mA | |
| R_W | Wiper Resistance | | | 300 | Ω | $I_W = \pm 3$ mA @ $V_{CC} = 5$ V |
| R_W | Wiper Resistance | | | 150 | Ω | $I_W = \pm 3$ mA @ $V_{CC} = 5$ V |
| V_{TERM} | Voltage on any R_H or R_L Pin | V_{SS} | | V_{CC} | V | $V_{SS} = 0$ V |
| | Noise | | -120 | | dBV/ \sqrt{Hz} | Ref: 1V |
| | Resolution | | 0.4 | | % | |
| | Absolute Linearity ⁽¹⁾ | | | +1 | MI ⁽³⁾ | $R_{W(n)}(actual) - R_{W(n)}(expected)$ ⁽⁵⁾ |
| | Relative Linearity ⁽²⁾ | | | +0.2 | MI ⁽³⁾ | $R_{W(n+1)} - [R_{W(n)} + MI]$ ⁽⁵⁾ |
| | Temperature Coefficient of R_{TOTAL} | | ± 300 | | ppm/ $^{\circ}C$ | |
| | Ratiometric Temp. Coefficient | | | 20 | ppm/ $^{\circ}C$ | |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | 10/10/25 | | pF | See Macro model |

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.

(3) $MI = RTOT / 255$ or $(R_H - R_L) / 255$, single pot

(4) During power up $V_{CC} > V_H, V_L,$ and V_W .

(5) $n = 0, 1, 2, \dots, 255; m = 0, 1, 2, \dots, 254$.

X9251

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|------------------|--|-----------------------|------|-----------------------|-------|--|
| | | Min. | Typ. | Max. | Units | |
| I _{CC1} | V _{CC} supply current (active) | | | 400 | μA | f _{SCK} = 2.5 MHz, SO = Open, V _{CC} =6V Other Inputs = V _{SS} |
| I _{CC2} | V _{CC} supply current (nonvolatile write) | | 1 | 5 | mA | f _{SCK} = 2.5MHz, SO = Open, V _{CC} =6V Other Inputs = V _{SS} |
| I _{SB} | V _{CC} current (standby) | | | 3 | μA | SCK = SI = V _{SS} , Addr. = V _{SS} , CS = V _{CC} = 6V |
| I _{LI} | Input leakage current | | | 10 | μA | V _{IN} = V _{SS} to V _{CC} |
| I _{LO} | Output leakage current | | | 10 | μA | V _{OUT} = V _{SS} to V _{CC} |
| V _{IH} | Input HIGH voltage | V _{CC} × 0.7 | | V _{CC} + 1 | V | |
| V _{IL} | Input LOW voltage | -1 | | V _{CC} × 0.3 | V | |
| V _{OL} | Output LOW voltage | | | 0.4 | V | I _{OL} = 3mA |
| V _{OH} | Output HIGH voltage | V _{CC} - 0.8 | | | V | I _{OH} = -1mA, V _{CC} ≥ +3V |
| V _{OH} | Output HIGH voltage | V _{CC} - 0.4 | | | V | I _{OH} = -0.4mA, V _{CC} ≤ +3V |

ENDURANCE AND DATA RETENTION

| Parameter | Min. | Units |
|-------------------|---------|-----------------------------------|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention | 100 | years |

CAPACITANCE

| Symbol | Test | Max. | Units | Test Conditions |
|------------------------------------|---|------|-------|-----------------------|
| C _{IN/OUT} ⁽⁶⁾ | Input / Output capacitance (SI) | 8 | pF | V _{OUT} = 0V |
| C _{OUT} ⁽⁶⁾ | Output capacitance (SO) | 8 | pF | V _{OUT} = 0V |
| C _{IN} ⁽⁶⁾ | Input capacitance (A0, A1, CS, WP, HOLD, and SCK) | 6 | pF | V _{IN} = 0V |

POWER-UP TIMING

| Symbol | Parameter | Min. | Max. | Units |
|---|---|------|------|-------|
| t _r V _{CC} ⁽⁶⁾ | V _{CC} Power-up rate | 0.2 | 50 | V/ms |
| t _{PUR} ⁽⁷⁾ | Power-up to initiation of read operation | | 1 | ms |
| t _{PUW} ⁽⁷⁾ | Power-up to initiation of write operation | | 50 | ms |

A.C. TEST CONDITIONS

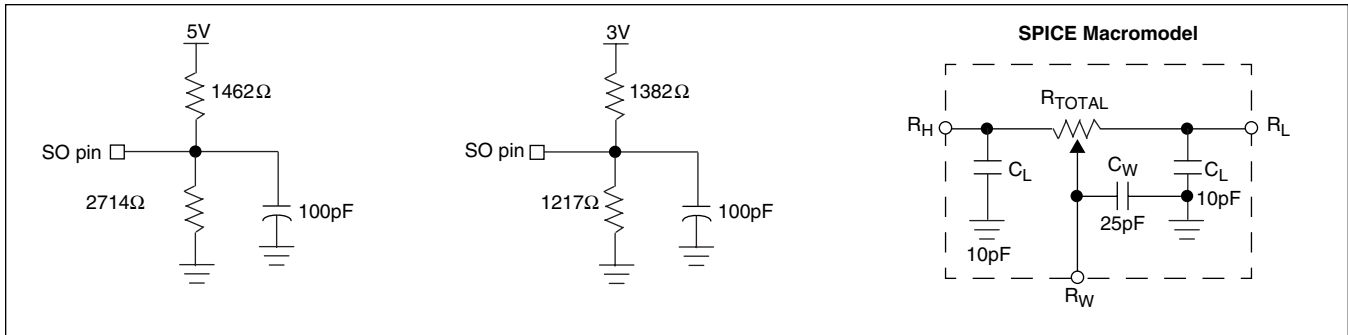
| | |
|-------------------------------|--|
| Input Pulse Levels | V _{CC} × 0.1 to V _{CC} × 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing level | V _{CC} × 0.5 |

Notes: (6) This parameter is not 100% tested

(7) t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

X9251

EQUIVALENT A.C. LOAD CIRCUIT



AC TIMING

| Symbol | Parameter | Min. | Max. | Units |
|-------------|--|------|------|---------|
| f_{SCK} | SSI/SPI clock frequency | | 2 | MHz |
| t_{CYC} | SSI/SPI clock cycle time | 500 | | ns |
| t_{WH} | SSI/SPI clock high time | 200 | | ns |
| t_{WL} | SSI/SPI clock low time | 200 | | ns |
| t_{LEAD} | Lead time | 250 | | ns |
| t_{LAG} | Lag time | 250 | | ns |
| t_{SU} | SI, SCK, \overline{HOLD} and \overline{CS} input setup time | 50 | | ns |
| t_H | SI, SCK, \overline{HOLD} and \overline{CS} input hold time | 50 | | ns |
| t_{RI} | SI, SCK, \overline{HOLD} and \overline{CS} input rise time | | 2 | μ s |
| t_{FI} | SI, SCK, \overline{HOLD} and \overline{CS} input fall time | | 2 | μ s |
| t_{DIS} | SO output disable time | 0 | 250 | ns |
| t_V | SO output valid time | | 200 | ns |
| t_{HO} | SO output hold time | 0 | | ns |
| t_{RO} | SO output rise time | | 100 | ns |
| t_{FO} | SO output fall time | | 100 | ns |
| t_{HOLD} | \overline{HOLD} time | 400 | | ns |
| t_{HSU} | \overline{HOLD} setup time | 100 | | ns |
| t_{HH} | \overline{HOLD} hold time | 100 | | ns |
| t_{HZ} | \overline{HOLD} low to output in high Z | | 100 | ns |
| t_{LZ} | \overline{HOLD} high to output in low Z | | 100 | ns |
| T_I | Noise suppression time constant at SI, SCK, \overline{HOLD} and \overline{CS} inputs | | 10 | ns |
| t_{CS} | \overline{CS} deselect time | 2 | | μ s |
| t_{WPASU} | \overline{WP} , A0 setup time | 0 | | ns |
| t_{WPAH} | \overline{WP} , A0 hold time | 0 | | ns |

X9251

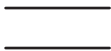


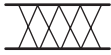

HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Typ. | Max. | Units |
|----------|--|------|------|-------|
| t_{WR} | High-voltage write cycle time (store instructions) | 5 | 10 | ms |

XDCP TIMING

| Symbol | Parameter | Min. | Max. | Units |
|------------|--|------|------|---------|
| t_{WRPO} | Wiper response time after the third (last) power supply is stable | 5 | 10 | μ s |
| t_{WRL} | Wiper response time after instruction issued (all load instructions) | 5 | 10 | μ s |

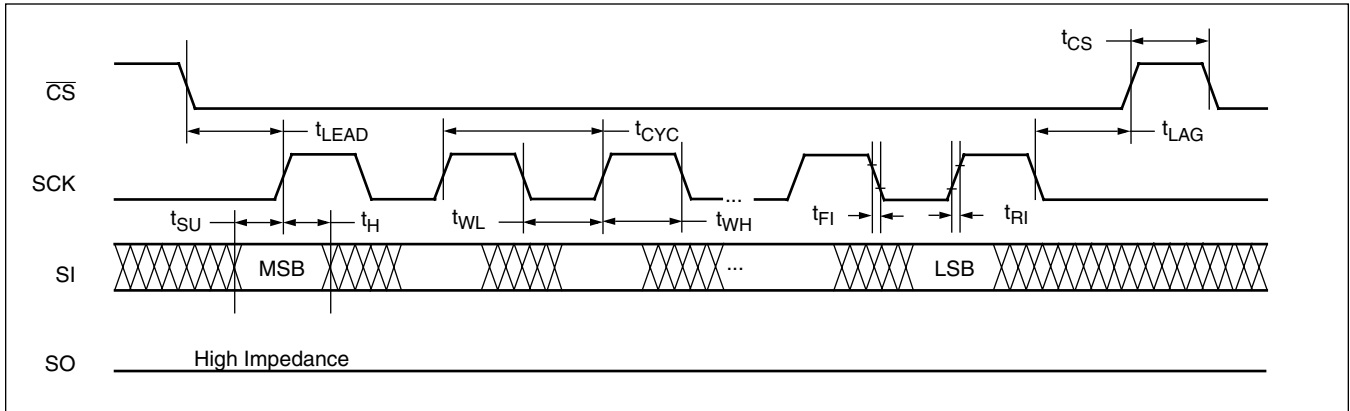
SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|-----------------------------|-------------------------------|
|  | Must be steady | Will be steady |
|  | May change from Low to High | Will change from Low to High |
|  | May change from High to Low | Will change from High to Low |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

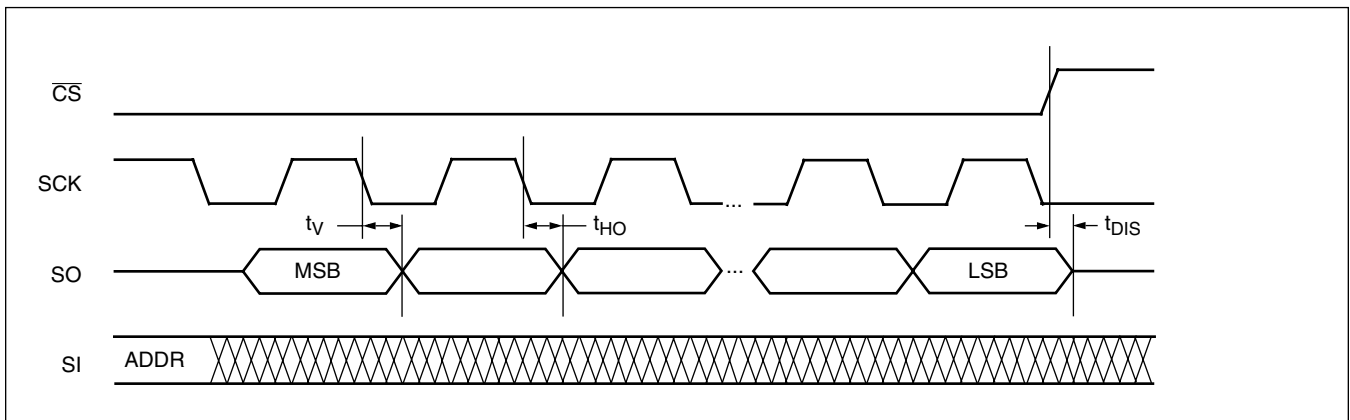
X9251

TIMING DIAGRAMS

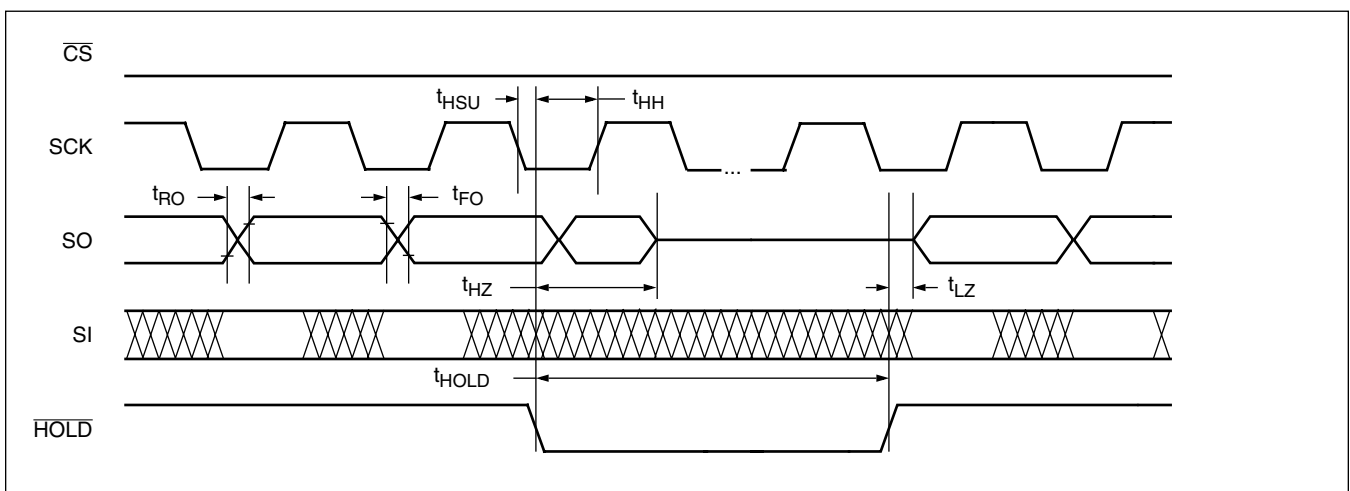
Input Timing



Output Timing

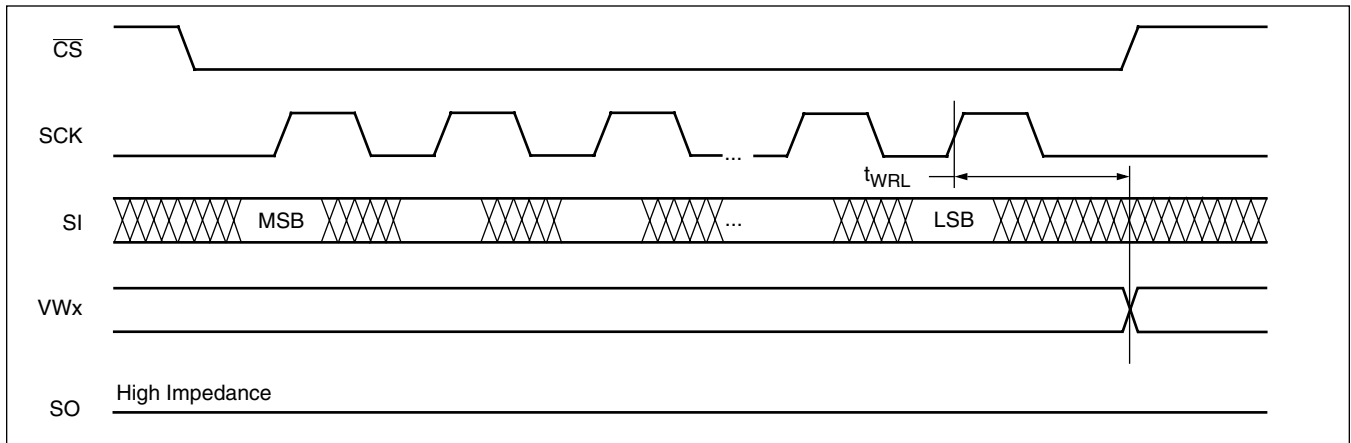


Hold Timing

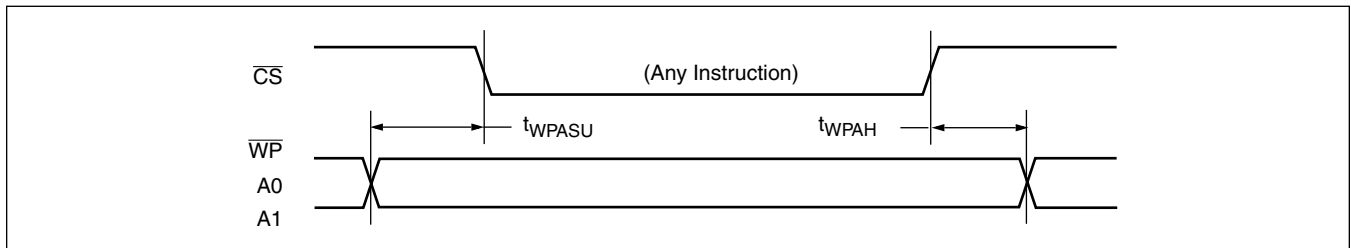


X9251

XDCP Timing (for All Load Instructions)

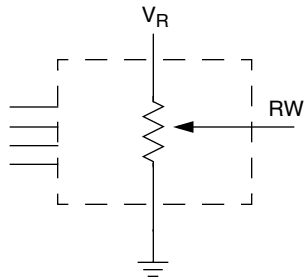


Write Protect and Device Address Pins Timing

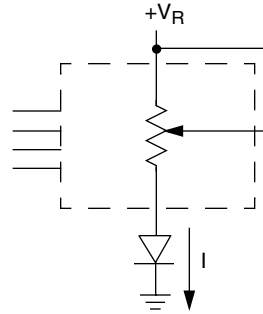


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



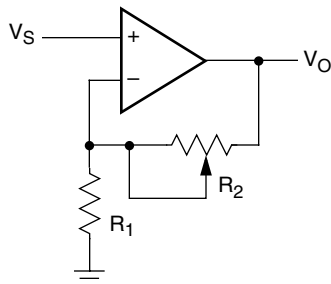
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

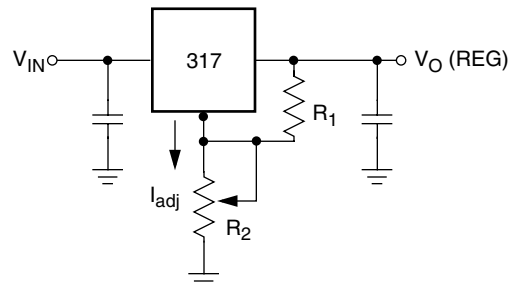
Application Circuits

Noninverting Amplifier



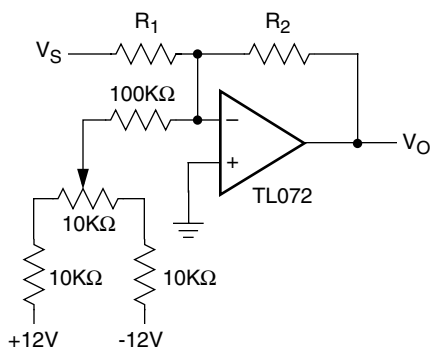
$$V_O = (1 + R_2/R_1)V_S$$

Voltage Regulator

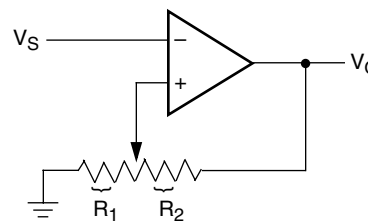


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

Offset Voltage Adjustment



Comparator with Hysteresis

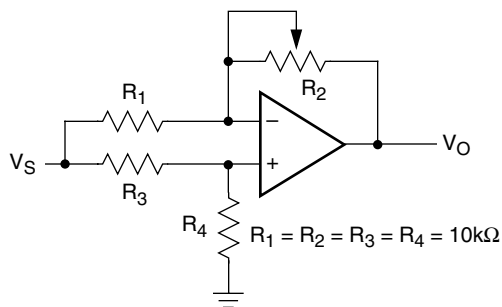


$$V_{UL} = \{R_1/(R_1 + R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1 + R_2)\} V_O(\text{min})$$

Application Circuits (continued)

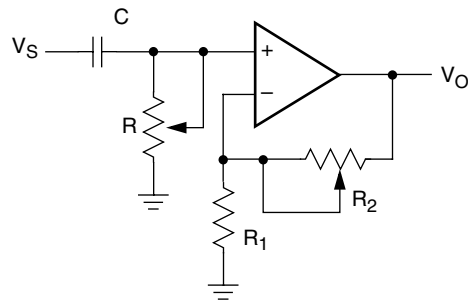
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

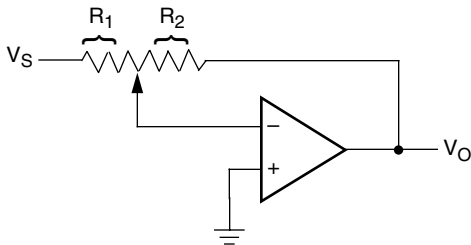
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

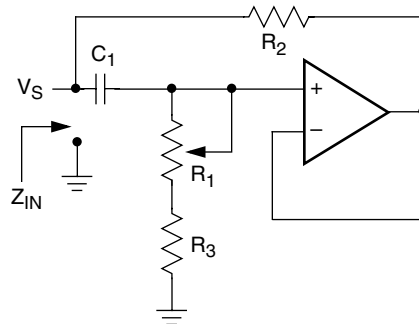
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

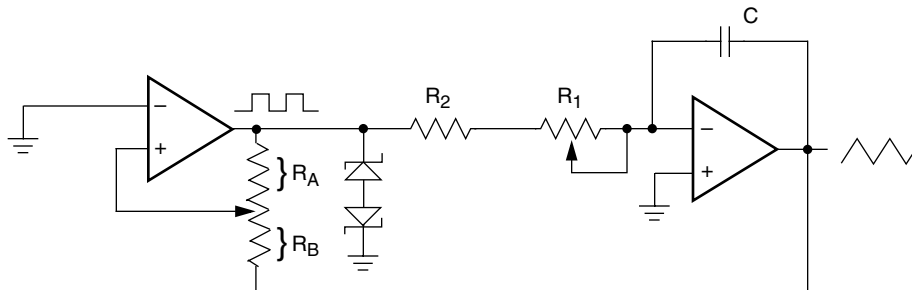
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) \quad C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

Function Generator



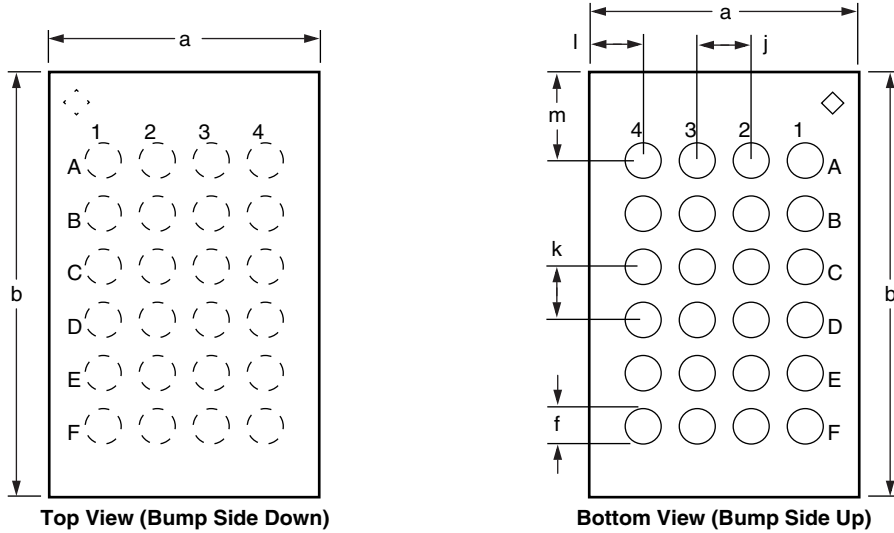
$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

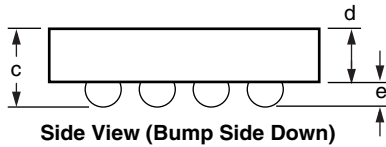
X9251

PACKAGING INFORMATION

24-Ball BGA (X9251TA/X9251UA)



Note: Drawing not to scale
 ◇ = Die Orientation mark



Ball Matrix

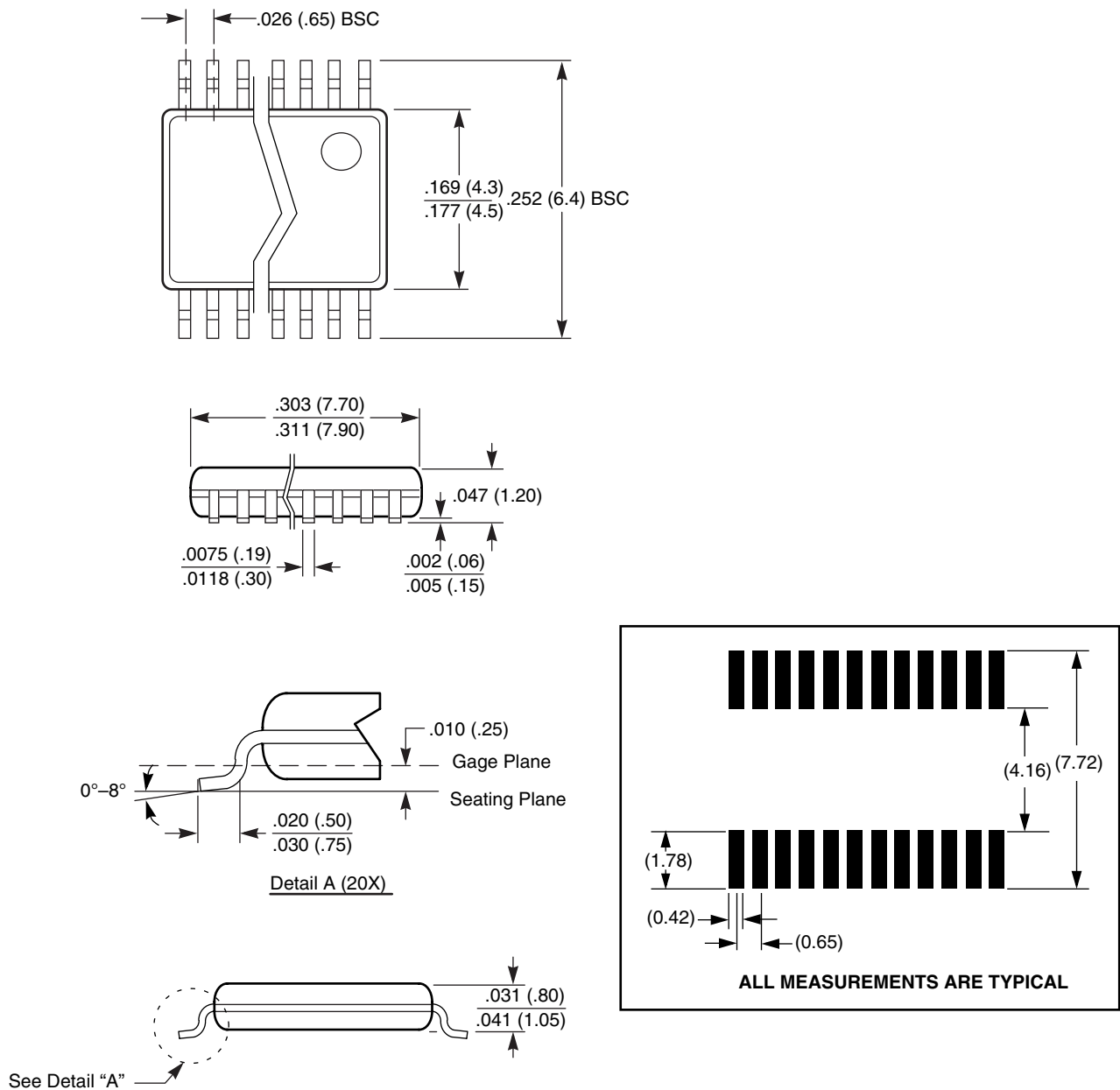
| | 4 | 3 | 2 | 1 |
|---|-----------------|-----------------|-----------------|-----------------|
| A | R _{L1} | A1 | \overline{CS} | R _{W0} |
| B | R _{W1} | SI | \overline{WP} | R _{L0} |
| C | VSS | R _{H1} | R _{H0} | VCC |
| D | NC | R _{H2} | R _{H3} | NC |
| E | R _{W2} | HOLD | SO | R _{L3} |
| F | R _{L2} | SCK | A0 | R _{W3} |

| | Symbol | Millimeters | | | Inches | | |
|---------------------------------------|--------|-------------|-------|-------|--------|--------|--------|
| | | Min | Nom. | Max | Min | Nom. | Max |
| Package Body Dimension X | a | 2.727 | 2.757 | 2.787 | 0.1074 | 0.1086 | 0.1097 |
| Package Body Dimension Y | b | 4.505 | 4.535 | 4.565 | 0.1774 | 0.1786 | 0.1797 |
| Package Height | c | 0.654 | 0.682 | 0.710 | 0.0258 | 0.0269 | 0.0280 |
| Body Thickness | d | 0.444 | 0.457 | 0.470 | 0.0175 | 0.0180 | 0.0185 |
| Ball Height | e | 0.210 | 0.225 | 0.240 | 0.0083 | 0.0089 | 0.0094 |
| Ball Diameter | f | 0.316 | 0.326 | 0.336 | 0.0124 | 0.0128 | 0.0132 |
| Ball Pitch-X Axis | j | 0.5 | | | 0.0197 | | |
| Ball Pitch-Y Axis | k | 0.5 | | | 0.0197 | | |
| Ball to Edge Spacing-Distance Along X | l | 0.594 | 0.629 | 0.664 | 0.0234 | 0.0248 | 0.0261 |
| Ball to Edge Spacing-Distance Along Y | m | 0.983 | 1.018 | 1.053 | 0.0387 | 0.0401 | 0.0414 |

X9251

PACKAGING INFORMATION

24-Lead Plastic, TSSOP, Package Code V24

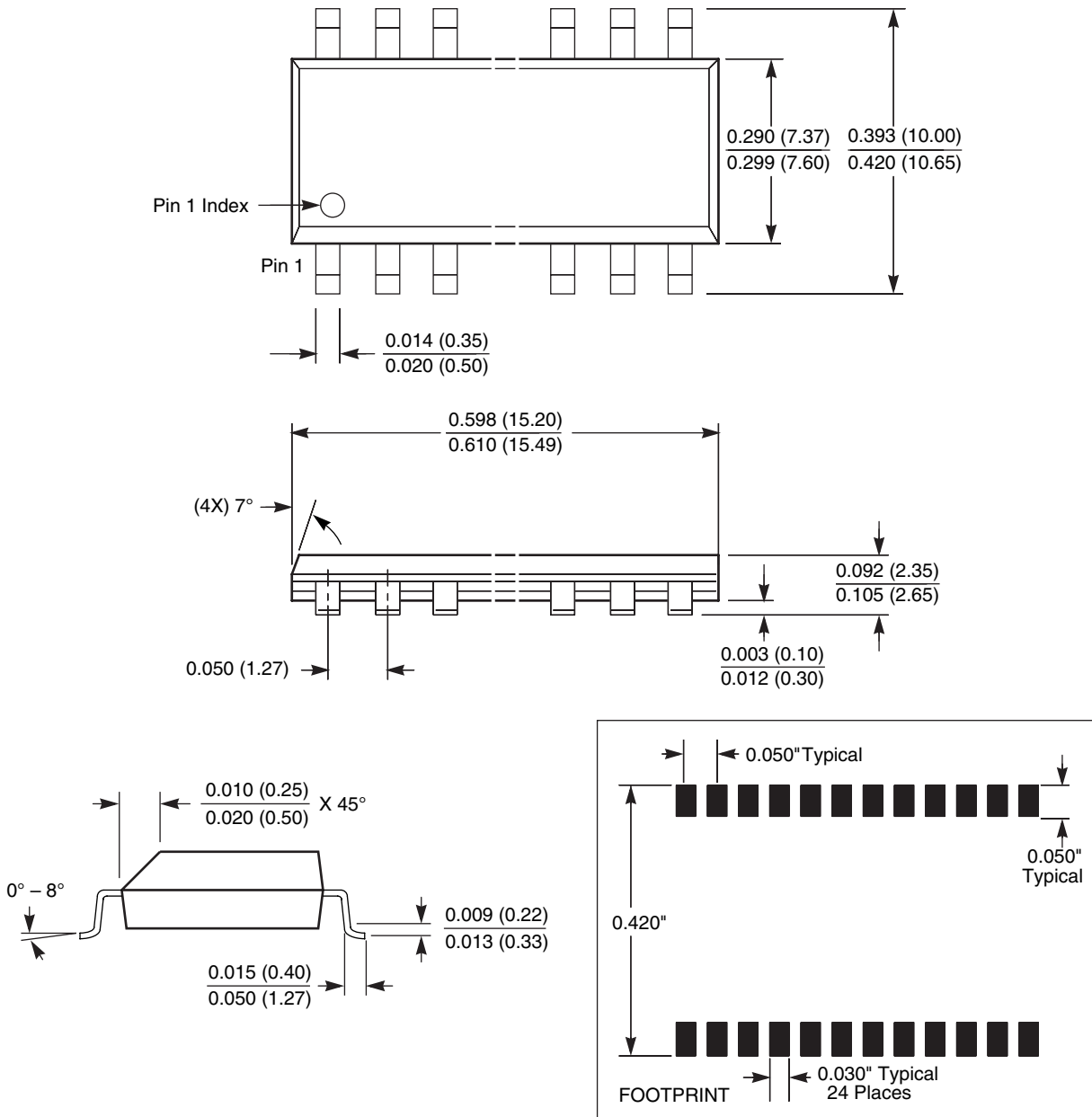


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X9251

PACKAGING INFORMATION

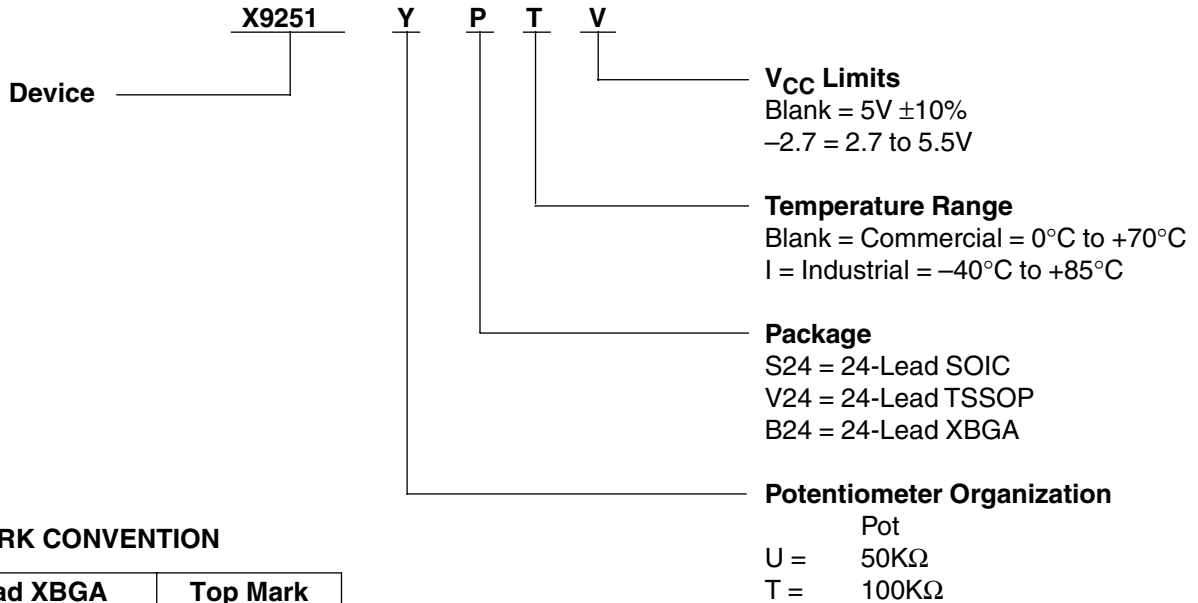
24-Lead Plastic, SOIC, Package Code S24



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

X9251

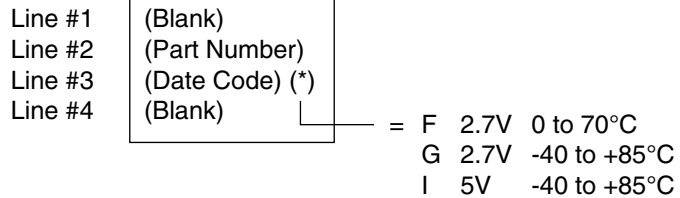
ORDERING INFORMATION



PART MARK CONVENTION

| 24 Lead XBGA | Top Mark |
|----------------|----------|
| X9251TB24 | XAAZ |
| X9251TB24-2.7 | XABL |
| X9251TB24I | XACV |
| X9251TB24I-2.7 | XACX |
| X9251UB24 | XACZ |
| X9251UB24-2.7 | XADA |
| X9251UB24I | XADB |
| X9251UB24I-2.7 | XADC |

S & V Package Marking



LIMITED WARRANTY

©Xicor, Inc. 2001 Patents Pending

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, or licenses are implied.

TRADEMARK DISCLAIMER:

Xicor and the Xicor logo are registered trademarks of Xicor, Inc. AutoStore, Direct Write, Block Lock, SerialFlash, MPS, and XDCP are also trademarks of Xicor, Inc. All others belong to their respective owners.

U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976; 4,980,859; 5,012,132; 5,003,197; 5,023,694; 5,084,667; 5,153,880; 5,153,691; 5,161,137; 5,219,774; 5,270,927; 5,324,676; 5,434,396; 5,544,103; 5,587,573; 5,835,409; 5,977,585. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.