偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT6804

Monitor On-Screen Display

Data Sheet

REV. 1.02

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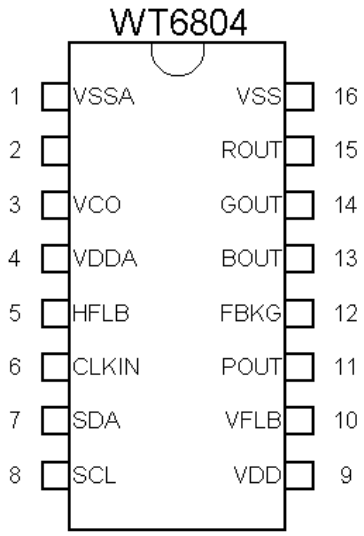
GENERAL DESCRIPTION

The WT6804 is an on-screen display (OSD) IC which display color symbols or characters onto monitor. With the control of microcontroller through I^2C interface, it can display characters with special effect like blinking or shadowing automatically.

FEATURES

- Programmable horizontal resolutions up to 1530 dots per line
- Horizontal frequency up to 120KHz
- On-chip PLL up to 100MHz
- Fully programmable character array of 15 rows by 30 columns
- 12x18 dot matrix per character
- 256 characters and graphic symbols ROM including 16 multi-color fonts
- 8 colors per display character
- 7 colors per display character background
- 4 programmable windows
- Double character height and width control
- Programmable character height (18 to 71 lines)
- Programmable row-to-row spacing
- Programmable vertical and horizontal positioning for display screen center
- Bordering, shadowing and blinking effect
- Fade-in/fade-out effects
- I^2C interface with slave address $7AH
- Power supply : 5V
- Package type : 16-pin plastic DIP/SOP

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	VSSA		Analog ground.
2	NC		No connection.
3	LF	I/O	Loop filter of PLL.
4	VDDA		Analog power supply
5	HFLB	I	Horizontal sync input.
6	CLKIN	I	External clock input.
7	SDA	I/O	Serial data of I^2C interface.
8	SCL	I	Serial clock of I^2C interface.
9	VDD		Digital power supply
10	VFLB	I	Vertical sync input.
11	POUT	O	Programmable general purpose output pad
12	FBKG	O	Fast Blanking output. This pin controls the mixer of vedio amplifier to cutoff the video signal while displaying character or window.
13	BOUT	O	Blue color output
14	GOUT	O	Green color output
15	ROUT	O	Red color output
16	VSS		Digital ground

FUNCTIONAL DESCRIPTION

I²C Interface

This is a slave mode I²C interface which address is $7AH.
There are three data transmission formats for writing: Format (a), (b) and (c).

Format (a):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	ROW	A	COL	A	Data	A	•••••	P

Format (b):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	COL	A	Data	A	COL	A	•••••	P

Format (c):

S	0 1 1 1 1 0 1 0	A	ROW	A	COL	A	Data	A	Data	A	Data	A	Data	A	•••••	P

Where S = START condition
R/W = Read/Write control bit. “1” means READ operation and “0” means WRITE operation.
A = Acknowledge bit. “0” means acknowledge.
P = STOP condition
ROW = Row address byte
COL = Column address byte
Data = Data byte

Format (a) is used when write data in different row and column address.
Format (b) is used when write data in the same row.
Format (c) is suitable for writing data sequentially. The column address will increase automatically.

Format (a)→(b), Format (a)→(c), Format (b)→(a) or Format (b)→(c) is allowed. But Format (c)→(a) and Format (c)→(b) is not allowed.

Transmission Format

	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Format
Address Bytes Control Bytes	Row	1	0	0	D	D	D	D	D	a,b,c
	$Column_{a,b}$	0	0	x	D	D	D	D	D	a,b
	$Column_c$	0	1	x	D	D	D	D	D	c
Attribute Bytes	Row	1	0	1	D	D	D	D	D	a,b,c
	$Column_{a,b}$	0	0	x	D	D	D	D	D	a,b
	$Column_c$	0	1	x	D	D	D	D	D	c

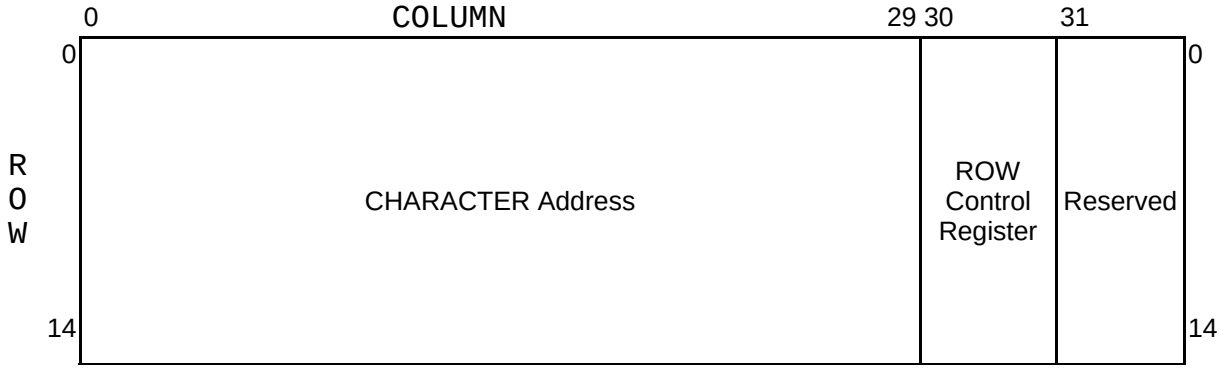
“x” : Don’t care.

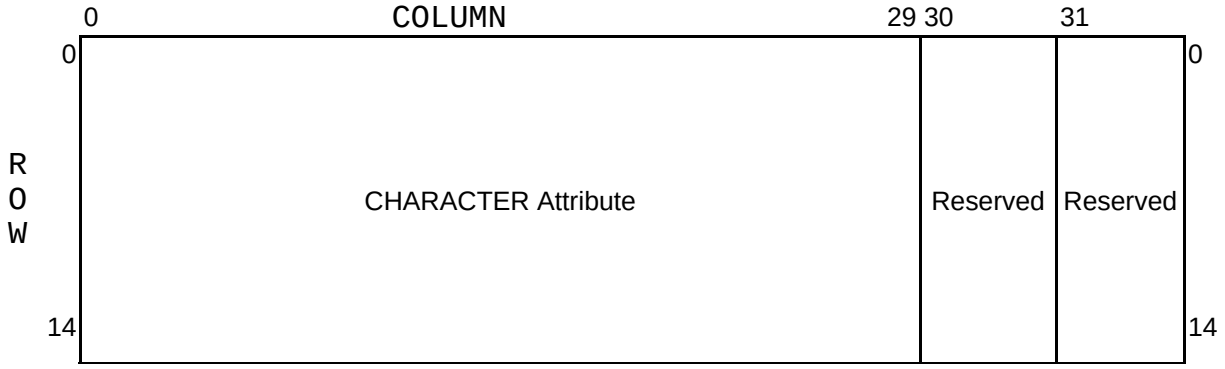
Display RAM and Row Control Register

DISPLAY RAM

The display RAM stores the data to be displayed. Address byte determines display character and attribute bytes determines character background, character color and blinking effect.

The memory location is shown as below.





Address Byte

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0, 0) : (14,29)	W	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA7~CA0 – Address of Character ROM

Attribute Byte

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0, 0) : (14,29)	W	--	BG_R	BG_G	BG_B	BLINK	CH_R	CH_G	CH_B

BG_R, BG_G, BG_B – Background color of its corresponding character.
BLINK – Enable blinking effect of its corresponding character. The blinking speed is controlled by BNK1 and BNK0 bits.
CH_R, CH_G, CH_B – Color of its corresponding character.

CH_R	CH_G	CH_B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

BG_R	BG_G	BG_B	Color
0	0	0	Background
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

ROW Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(0,30) : (14,30)	W	--	--	--	--	--	--	DCH	DCW

DCH – Double Character height
DCW – Double Character width. The character width of even column (column 0, 2, 4, 6, ….) is doubled and the odd column will not display.

Note:
1) Writing data into RAM must enable PLL or using external clock.
2) The I^2C interface clock frequency must less than 1/24 PLL clock frequency when writing RAM.

Window Control

Window 1 has the highest priority and window 4 is the least. If window overlapping occurs, the higher priority covers the lower and the higher priority color will take over on the overlap window area.

Window 1 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,0)	W	W1RS3	W1RS2	W1RS1	W1RS0	W1RE3	W1RE2	W1RE1	W1RE0
(15,1)	W	W1CS4	W1CS3	W1CS2	W1CS1	W1CS0	W1EN	--	W1SHD
(15,2)	W	W1CE4	W1CE3	W1CE2	W1CE1	W1CE0	W1_R	W1_G	W1_B

W1RS3~0 – Window 1 Row start address
W1RE3~0 – Window 1 Row end address
W1CS4~0 – Window 1 Column start address
W1CE4~0 – Window 1 Column end address
W1EN – Enable Window 1. Default value = 0
W1SHD – Enable the shadow effect of the window 1. Default value = 0
W1_R, W1_G, W1_B – Define the color of window 1

Window 2 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,3)	W	W2RS3	W2RS2	W2RS1	W2RS0	W2RE3	W2RE2	W2RE1	W2RE0
(15,4)	W	W2CS4	W2CS3	W2CS2	W2CS1	W2CS0	W2EN	--	W2SHD
(15,5)	W	W2CE4	W2CE3	W2CE2	W2CE1	W2CE0	W2_R	W2_G	W2_B

Window 3 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,6)	W	W3RS3	W3RS2	W3RS1	W3RS0	W3RE3	W3RE2	W3RE1	W3RE0
(15,7)	W	W3CS4	W3CS3	W3CS2	W3CS1	W3CS0	W3EN	--	W3SHD
(15,8)	W	W3CE4	W3CE3	W3CE2	W3CE1	W3CE0	W3_R	W3_G	W3_B

Window 4 Control Registers

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,9)	W	W4RS3	W4RS2	W4RS1	W4RS0	W4RE3	W4RE2	W4RE1	W4RE0
(15,10)	W	W4CS4	W4CS3	W4CS2	W4CS1	W4CS0	W4EN	--	W4SHD
(15,11)	W	W4CE4	W4CE3	W4CE2	W4CE1	W4CE0	W4_R	W4_G	W4_B

Frame Control Register

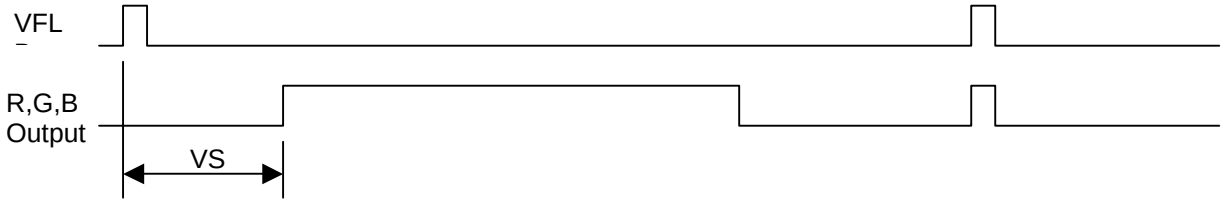
OSD Vertical Starting Position Register

This register controls the vertical displacement from top.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,12)	W	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0

Default Value = $04h
Minimum value = $01h

VS7~VS0 – Vertical starting position. Each step is 4 Horizontal lines.
Vertical starting position = (VS x 4) +2



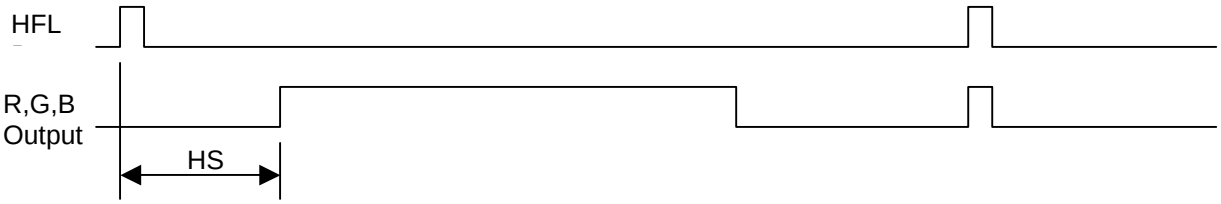
OSD Horizontal Starting Position Register

This register controls the vertical displacement from top.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,13)	W	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0

Default Value = $0Fh
Minimum value = $01h

HS7~HS0 – Horizontal starting position. Each step is 6 dots.
Horizontal starting position = (HS x 6) + 45 dot ± PLL phase error



Character Height Enlargement Register

This register enlarges the character height. The enlargement is done by repeating lines of every row.

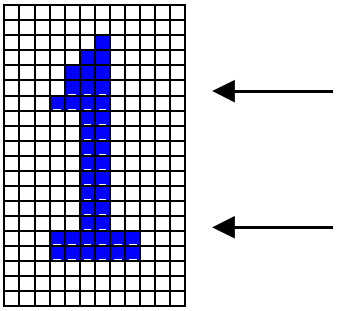
(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,14)	W	--	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Default Value = $00h

CH6~CH0 – Define the enlargement of character height.

CH6	CH5	CH4	CH3	CH2	CH1	CH0	Total Lines	Repeat Line																		
								0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0	X	0	0	0	0	0	18																		
0	X	0	0	0	0	1	19									v									
0	X	0	0	0	1	0	20					v								v					
0	X	0	0	1	0	0	22			v				v				v				v			
0	X	0	1	0	0	0	26		v		v		v		v		v		v		v		v		
0	X	0	1	1	1	1	33		v	v	v	v	v	v	v	v	v	v	v	v	v	v	v		
0	X	1	0	0	0	0	34		v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	
0	X	1	0	0	0	1	35	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	
1	0	0	0	0	0	0	36	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v
1	0	1	0	0	0	1	53																		
1	1	0	0	0	0	0	54																		
1	1	1	0	0	0	0	70																		
1	1	1	0	0	0	1	71																		

For example, if CH[6:0] = $02h, insert line#4 and line#12.



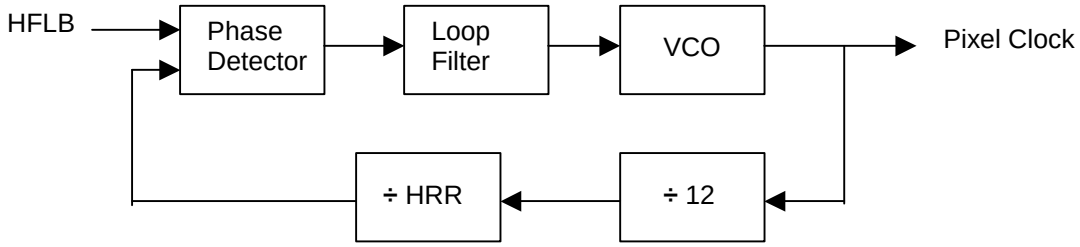
Horizontal Resolution Register

This register controls the pixel clock frequency which is multiplied by HFLB input.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,15)	W	--	HR6	HR5	HR4	HR3	HR2	HR1	HR0

Default Value = $40h

HR6~HR0 – Define the Horizontal resolution (i.e. pixels per horizontal line).
VCO frequency is (HR[6:0] x12 +6) x f_{HFLB} .



Row-to-Row Spacing Register

This register controls the row-to-row spacing. It adds line(s) below each row.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,16)	W	--	--	--	RSP4	RSP3	RSP2	RSP1	RSP0

Default Value = $00h

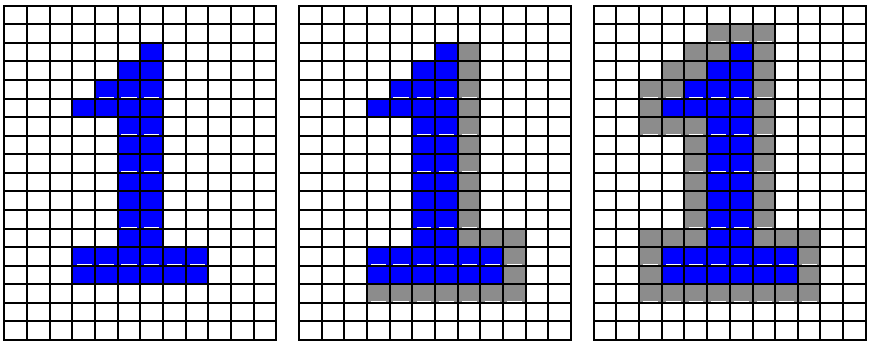
RSP4~RSP0 – Define the line(s) below each row.

Display Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,17)	W	ENOSD	BSEN	SHADW	FADE	BLANK	WINCLR	RAMCLR	FBKGC

Default Value = $00h

ENOSD – Enable OSD Display.
BSEN – Enable bordering and shadowing effect
SHADW – "1" : Shadowing.
"0" : Bordering
FADE – Fade in /Fade out Enable
BLANK – Force FBKG pin output high level when this bit is set.
WINCLR – Clear all window enable bits. (W1EN ~ W4EN)
RAMCLR – Clear all ADDRESS bytes, BG_R, BG_G, BG_B and BLINK bits of display RAM.
FBKGC – FBKG pin control.
"0" : FBKG pin active during display character or window
"1" : FBKG pin active during display character only.
The polarity of FBKG pin is controlled by FBKGP bit.



Normal Shadow Effect Border Effect

Output Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,18)	W	TRIC	FBKGP	--	SELVCL	HPOL	VPOL	VCO1	VCO0

Default Value = $FCh

TRIC – Tri-state control of ROUT, GOUT, BOUT and FBKG pin.
"1" – When OSD is disabled, these pins will drive low.
"0" – When OSD is disabled, these pins will be in high impedance state

FBKGP – Controls the polarity of FBKG pin.
"0" – Negative polarity.
"1" – Positive polarity.

SELVCL – Auto synchronize Hsync with Vsync.
"0" – Disable.
"1" – Enable.

HPOL – "1": Accept positive polarity of Hsync input.
"0" : Accept negative polarity of Hsync input.

VPOL – "1": Accept positive polarity of Vsync input.
"0" : Accept negative polarity of Vsync input.

VCO1,VCO0 – VCO control

VCO1	VCO0	Frequency Range
0	0	>104MHz
0	1	13MHz ~ 26MHz
1	0	26MHz ~ 52MHz
1	1	52MHz ~ 104MHz

Shadow and Border Effect

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,19)	W	--	WS_R	WS_G	WS_B	--	CS_R	CS_G	CS_B

WS_R, WS_G, WS_B – Define the color of window shadow
CS_R, CS_G, CS_B – Define the color of character shadow or border

WS_R	WS_G	WS_B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Multi-color Font

The character ROM has 256 fonts and16 multi-color fonts. Each character font has 12 dots width and 18 lines height.
Multi-color font character address is located from $F0h to $FFh when CFONT bit is set.

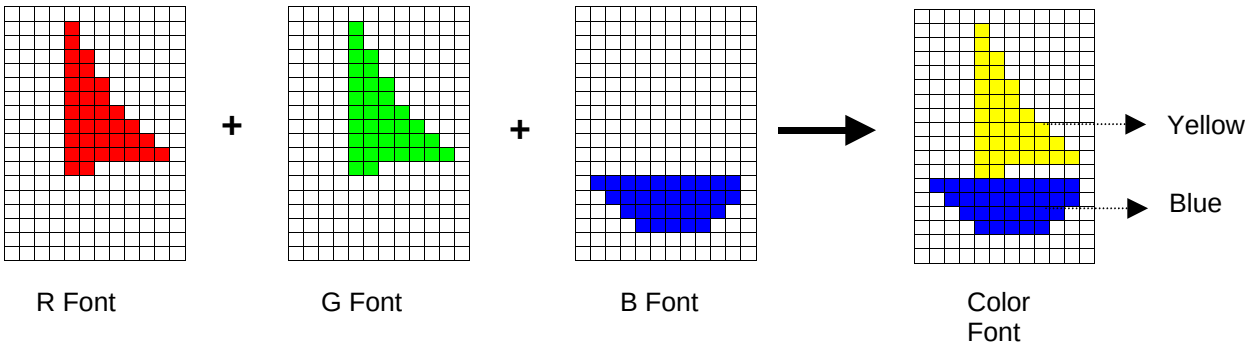
(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,20)	W	--	--	--	--	--	--	--	CFONT

Defualt = $00h

CFONT – Enable multi-color font character when this bit is set.

Multi-color font color table

R	G	B	Color
0	0	0	Background color
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White



Window Shadow Width Register

This register controls the width of window shadow.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,21)	W	WSW41	WSW40	WSW31	WSW30	WSW21	WSW20	WSW11	WSW10

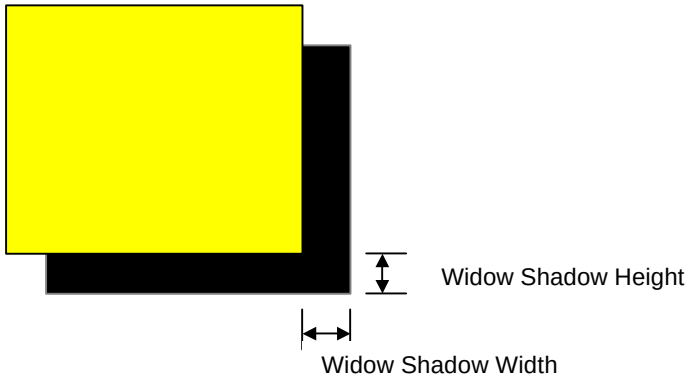
WSW41,WSW40 – Shadow width of Window 4.
WSW31,WSW30 – Shadow width of Window 3.
WSW21,WSW20 – Shadow width of Window 2.
WSW11,WSW10 – Shadow width of Window 1.
Width = (bit value x 2) + 2 dots

Window Shadow Height Register

This register controls the height of window shadow.

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,22)	W	WSH41	WSH40	WSH31	WSH30	WSH21	WSH20	WSH11	WSH10

WSH41,WSH40 – Shadow height of Window 4.
WSH31,WSH30 – Shadow height of Window 3.
WSH21,WSH20 – Shadow height of Window 2.
WSH11,WSH10 – Shadow height of Window 1.
Height = (bit value x 2) + 2 lines



Fade in/Fade out Effect

The fade-in/fade-out effect can be controlled either in horizontal direction only, vertical direction only or both direction.

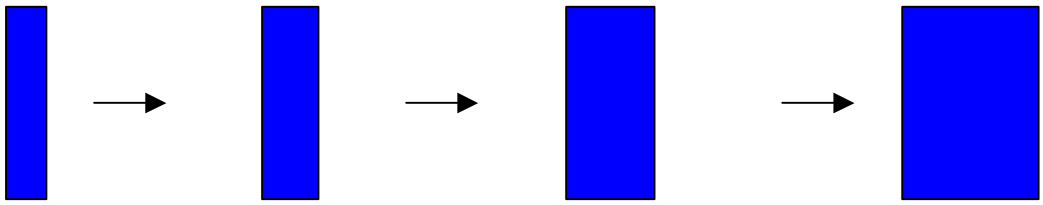
Fade in/out Control Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,23)	W	DISH	DISV	FVC1	FVC0	BKS1	BKS0	--	HORR

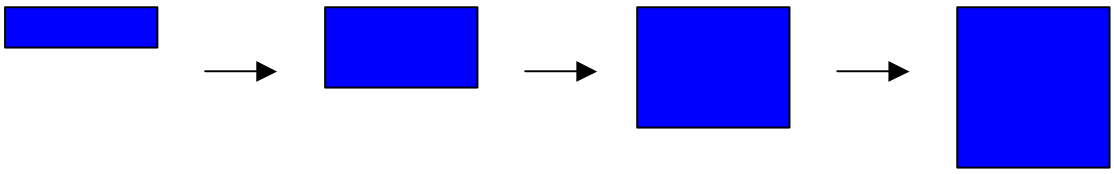
Default Value = $00h

DISH : Disable fade in/out horizontal direction. Increment/decrement one column per frame.
DISV : Disable fade in/out vertical direction
FVC1,FVC0 : Fade in/out vertical speed control
  00 – increment/decrement 1 row per frame
  01 – increment/decrement 2 row per frame
  10 – increment/decrement 3 row per frame
  11 – increment/decrement 4 row per frame
BKS1,BKS0 : Blinking speed select
  00 – 32 frames on, 32 frames off
  01 – 40 frames on, 40 frames off
  10 – 48 frames on, 48 frames off
  11 – 56 frames on, 56 frames off
HORR : Extension bit of horizontal resolution.
  VCO frequency is (HR[6:0] x12 + HORRx6 +6) x f_{HFLB}

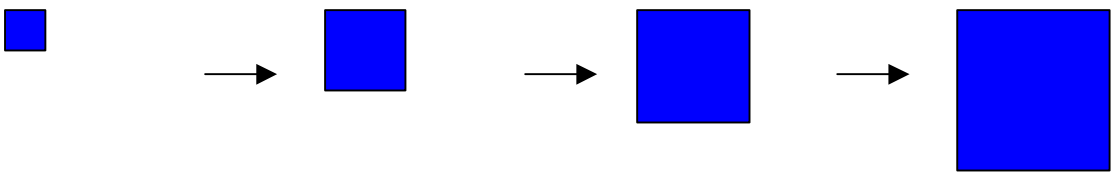
Enable horizontal direction only.



Enable vertical direction only.



Enable both direction.



RGB Output Control

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,24)	W	POC	ROC	GOC	BOC	PO	RO	GO	BO

Default = $00h

POC: POUT pin output control
- "0" : POUT pin is tri-state
- "1" : POUT pin is output

ROC: ROUT pin output control
- "0" : OSD red color output
- "1" : General output pin. The output level is controlled by RO bit

GOC: GOUT pin output control
- "0" : OSD green color output
- "1" : General output pin. The output level is controlled by GO bit

BOC: BOUT pin output control
- "0" : OSD blue color output
- "1" : General output pin. The output level is controlled by BO bit

PO: POUT pin output level when POC bit is 1
- "0" : POUT pin outputs low
- "1" : POUT pin outputs high

RO: ROUT pin output level when ROC bit is 1
- "0" : ROUT pin outputs low
- "1" : ROUT pin outputs high

GO: GOUT pin output level when GOC bit is 1
- "0" : GOUT pin outputs low
- "1" : GOUT pin outputs high

BO: BOUT pin output level when BOC bit is 1
- "0" : BOUT pin outputs low
- "1" : BOUT pin outputs high

Clock Source Selection Register

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,25)	W	ENPLL	CLKS	--	--	CKP	CKD2	CKD1	CKD0

Default = $80h

ENPLL – "1" : Enable PLL.
"0" : Disable PLL.

CLKS – Clock source select.
"0" : From PLL.
"1" : External clock from CLKIN pin. (For LCD monitor use)

When CLKS=1,
CKP control the polarity of CLKIN pin.
If CKP =0, no change of CLKIN polarity.
If CKP =1, reverse the polarity of CLKIN.
CKD2~ CKD0 select the pixel clock delay time from CLKIN pin.

CKD [2:0]	Delay Time
000	No delay.
001	Delay 2ns.
010	Delay 4ns.
011	Delay 6ns.
100	Delay 8ns.
101	Delay 10ns.
110	Delay 12ns.
111	Delay 14ns.

Reset

Write (16,31) register will reset all registers same as power on reset. All registers are set to default value.

TEST Mode

(Row,Col)	R/W	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
(15,31)	W	--	--	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0

Default $00h

For CRT monitor use, this register must keep $00h.
For LCD monitor, this register must be $08h. (Set TEST3 bit)

REGISTER MAP

(Row,Col)	R/W	Initial Value	Bit 7	Bit 6	Bit 5	Bit4	Bit 3	Bit 2	Bit 1	Bit 0
Address Byte										
(0, 0) : (14,29)	W	b'00000000	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Attribute Byte										
(0, 0) : (14,29)	W	b'xxxx0000	--	BG_R	BG_G	BG_B	BLINK	CH_R	CH_G	CH_B
Address Byte										
(0,30) : (14,30)	W	b'xxxxxx00	--	--	--	--	--	--	DCH	DCW
(15,0)	W	b'xxxxxxxx	W1RS3	W1RS2	W1RS1	W1RS0	W1RE3	W1RE2	W1RE1	W1RE0
(15,1)	W	b'xxxxx0x0	W1CS4	W1CS3	W1CS2	W1CS1	W1CS0	W1EN	--	W1SHD
(15,2)	W	b'xxxxxxxx	W1CE4	W1CE3	W1CE2	W1CE1	W1CE0	W1_R	W1_G	W1_B
(15,3)	W	b'xxxxxxxx	W2RS3	W2RS2	W2RS1	W2RS0	W2RE3	W2RE2	W2RE1	W2RE0
(15,4)	W	b'xxxxx0x0	W2CS4	W2CS3	W2CS2	W2CS1	W2CS0	W2EN	--	W2SHD
(15,5)	W	b'xxxxxxxx	W2CE4	W2CE3	W2CE2	W2CE1	W2CE0	W2_R	W2_G	W2_B
(15,6)	W	b'xxxxxxxx	W3RS3	W3RS2	W3RS1	W3RS0	W3RE3	W3RE2	W3RE1	W3RE0
(15,7)	W	b'xxxxx0x0	W3CS4	W3CS3	W3CS2	W3CS1	W3CS0	W3EN	--	W3SHD
(15,8)	W	b'xxxxxxxx	W3CE4	W3CE3	W3CE2	W3CE1	W3CE0	W3_R	W3_G	W3_B
(15,9)	W	b'xxxxxxxx	W4RS3	W4RS2	W4RS1	W4RS0	W4RE3	W4RE2	W4RE1	W4RE0
(15,10)	W	b'xxxxx0x0	W4CS4	W4CS3	W4CS2	W4CS1	W4CS0	W4EN	--	W4SHD
(15,11)	W	b'xxxxxxxx	W4CE4	W4CE3	W4CE2	W4CE1	W4CE0	W4_R	W4_G	W4_B
(15,12)	W	b'00000100	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
(15,13)	W	b'00001111	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
(15,14)	W	b'x0000000	--	CH6	CH5	CH4	CH3	CH2	CH1	CH0
(15,15)	W	b'x0000100	--	HR6	HR5	HR4	HR3	HR2	HR1	HR0
(15,16)	W	b'xxx00000	--	--	--	RSP4	RSP3	RSP2	RSP1	RSP0
(15,17)	W	b'00000000	ENOSD	BSEN	SHADW	FADE	BLANK	WINCLR	RAMCLR	FBKGC
(15,18)	W	b'11x11100	TRIC	FBKGP	--	SELVCL	HPOL	VPOL	VCO1	VCO0
(15,19)	W	b'xxxxxxxx	--	WS_R	WS_G	WS_B	--	CS_R	CS_G	CS_B
(15,20)	W	b'xxxxxxx0	--	--	--	--	--	--	--	CFONT
(15,21)	W	b'xxxxxxxx	WSW41	WSW40	WSW31	WSW30	WSW21	WSW20	WSW11	WSW10
(15,22)	W	b'xxxxxxxx	WSH41	WSH40	WSH31	WSH30	WSH21	WSH20	WSH11	WSH10
(15,23)	W	b'00000000	DISH	DISV	FVC1	FVC0	BKS1	BKS0	--	HORR
(15,24)	W	b'00000000	POC	ROC	GOC	BOC	POUT	ROUT	GOUT	BOUT
(15,25)	W	b'10xx0000	ENPLL	CLKS	--	--	CKP	CKD2	CKD1	CKD0
(15,31)	W	b'00000000	--	--	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
DC Supply Voltage (VDD)	-0.3	7.0	V
Input and output voltage with respect to Ground	-0.3	VDD+0.3	V
Storage temperature	-25	125	^{o}C
Ambient temperature with power applied	0	85	^{o}C

***Note: Stresses above those listed may cause permanent damage to the devices**

D.C Characteristics (VDD=5.0V±5%, Ta=0-70°C)

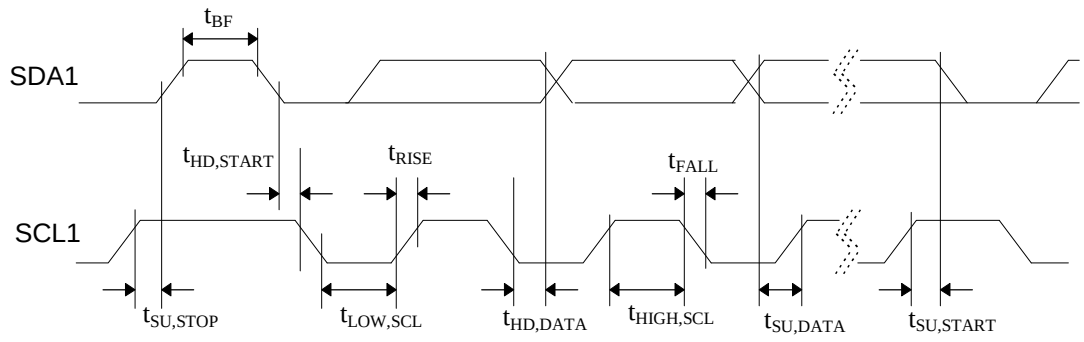
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75	5	5.25	V
$V_{IH,I2C}$	SDA and SCL Input High Voltage		$0.7V_{DD}$	--	V_{DD}+0.3	V
$V_{IL,I2C}$	SDA and SCL Input Low Voltage		-0.3	--	$0.3V_{DD}$	V
$V_{IH,SYNC}$	Sync Input High Voltage		2.0	--	V_{DD}+0.3	V
$V_{IL,SYNC}$	Sync Input Low Voltage		-0.3	--	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -6mA	4	--	V_{DD}	V
V_{OL}	Output Low Voltage	I_{OL} = 6mA	0	--	0.4	V
I_{IL}	Input Leakage Current	$0V < V_{IN} < V_{DD}$	-10	--	10	μA
I_{DD}	Operating Current	Dot rate=90MHz, no load	--	15	25	mA
V_{RESET}	Low VDD Reset Voltage		3.0	3.2	3.5	V

A.C Characteristics (VDD=5.0V, Ta=0-70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{RISE}	Rise time (ROUT,GOUT,BOUT and FBKG pins)	Cload=20pF	-	2.5	4	ns
t_{FALL}	Fall time (ROUT,GOUT,BOUT and FBKG pins)	Cload=20pF	-	2.5	4	ns
f_{HFLB}	HFLB Input Frequency		10	-	120K	Hz
f_{VFLB}	VFLB Input Frequency		4	-	2047	H lines
F_{PLL}	PLL Frequency		13	-	104	MHz

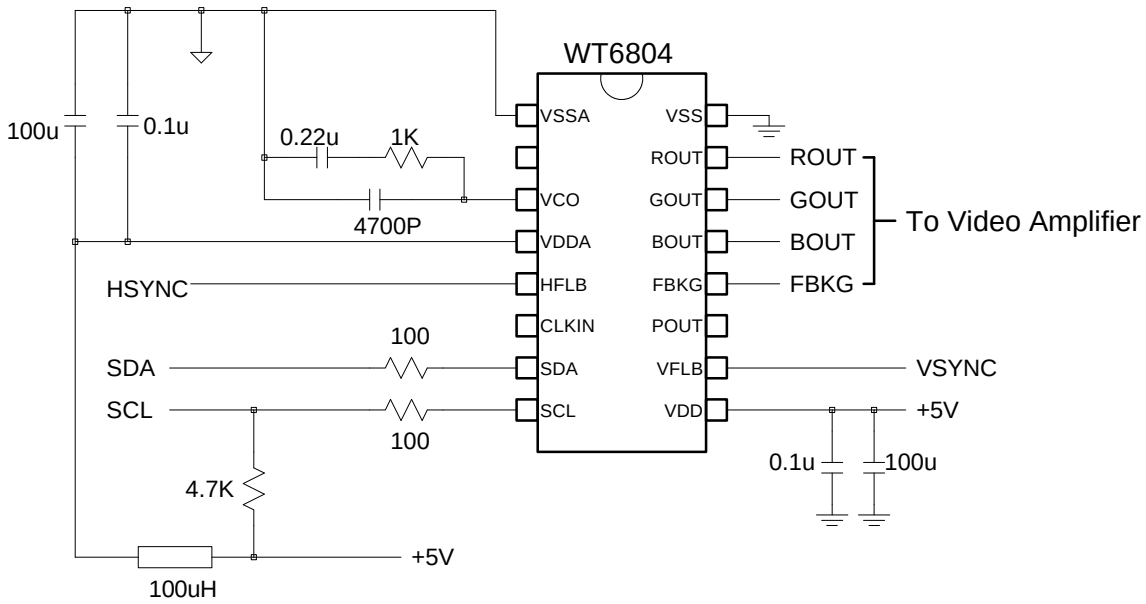
I2C Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL input clock frequency	0	-	100	kHz
t_{BF}	Bus free time	2	-	-	us
$t_{HD,START}$	Hold time for START condition	1	-	-	us
$t_{SU,START}$	Set-up time for START condition	1	-	-	us
$t_{HIGH,SCL}$	SCL clock high time	1	-	-	us
$t_{LOW,SCL}$	SCL clock low time	1	-	-	us
$t_{HD,DATA}$	Hold time for DATA input	0	-	-	ns
	Hold time for DATA output	80	-	-	ns
$t_{SU,DATA}$	Set-up time for DATA input	20	-	-	ns
	Set-up time for DATA output	100	-	-	ns
$t_{RISE,I2C}$	SCL and SDA rise time	-	-	1	us
$t_{FALL,I2C}$	SCL and SDA fall time	-	-	300	ns
$t_{SU,STOP}$	Set-up time for STOP condition	1	-	-	us



TYPICAL APPLICATION CIRCUIT

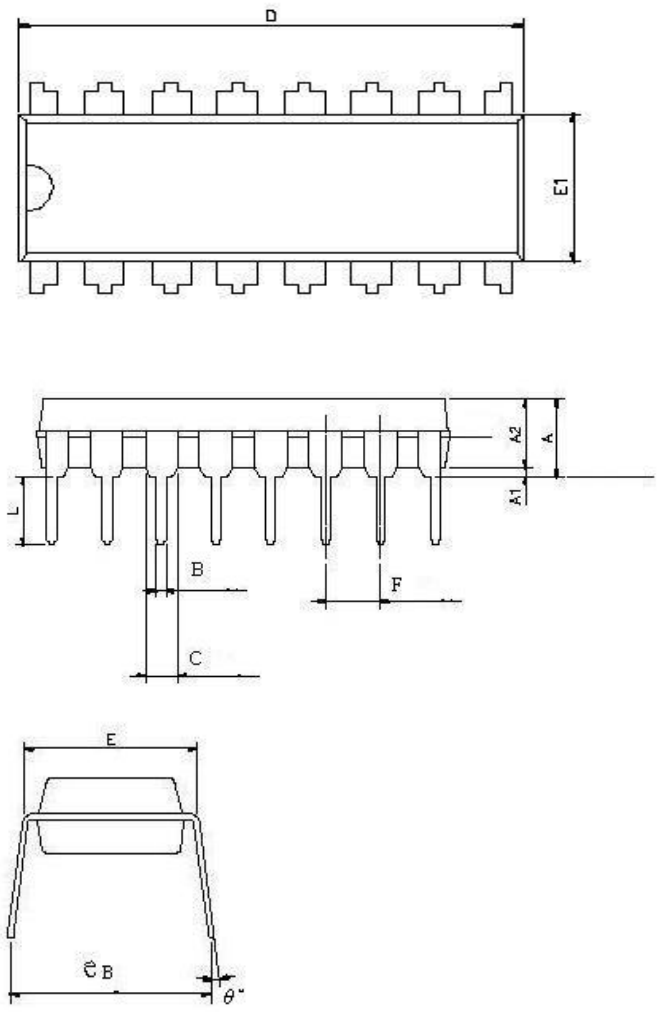
This circuit is for reference only.



PACKAGE OUTLINE

PDIP 16-pin package

Package type：16 Pin DIP 300mil



UNIT：INCH

SYMBOLS	MIN	NOR	MAX
A			0.210
A1	0.015		
A2	0.125	0.130	0.135
B		0.018	
C		0.060	
D	0.735	0.755	0.775
E		0.300 BSC	
E1	0.245	0.250	0.255
F		0.100	
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ °	0	7	15