



Preliminary W24LH8

32K × 8 CMOS STATIC RAM

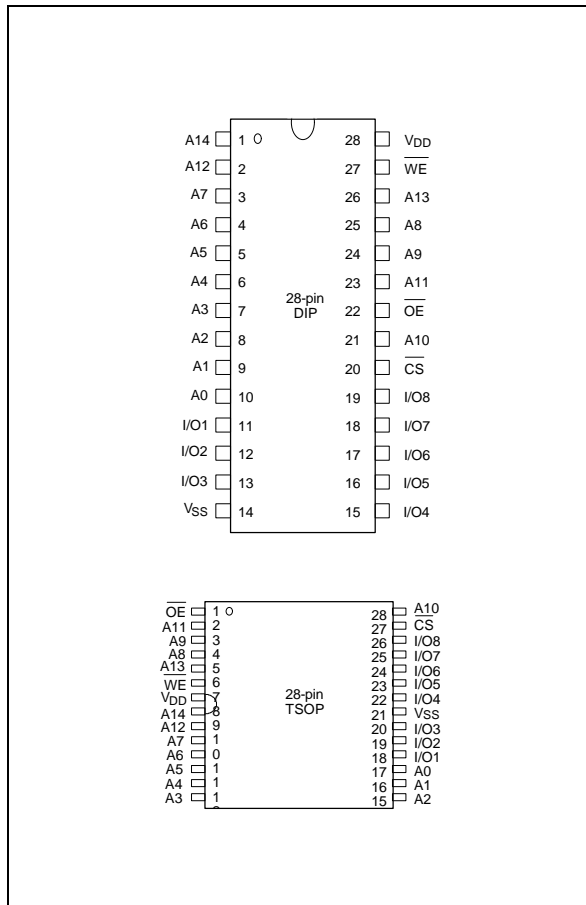
GENERAL DESCRIPTION

The W24LH8 is a normal speed, very low power CMOS static RAM organized as 32768 × 8 bits that operates on a wide voltage range from 2.7V to 3.6V power supply. The W24LH8 family, W24LH8-70LE and W24LH8-70LI, can meet requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

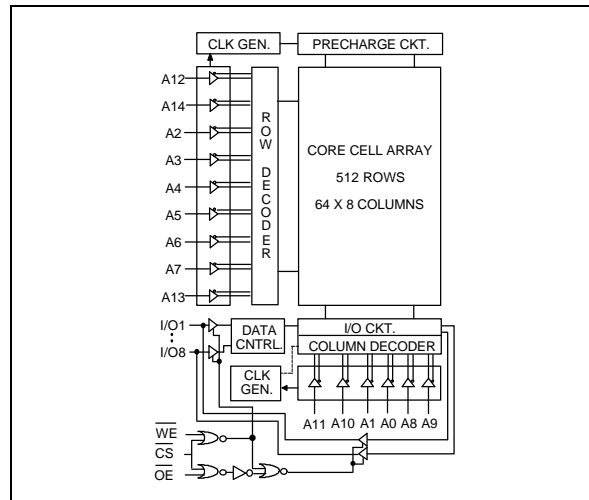
FEATURES

- Low power consumption:
 - Active: 156 mW (max.)
 - Standby: 10.8 μW (max.)
- Access time: 70 nS
- 2.7V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 600 mil DIP, 330 mil SOP and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground

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TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	MODE	I/O1- I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Supply Voltage to V _{SS} Potential		-0.5 to +4.6	V
Input/Output to V _{SS} Potential		-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation		1.0	W
Storage Temperature		-65 to +150	°C
Operating Temperature	SL	0 to 70	°C
	LE	-20 to 85	°C
	LI	-40 to 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 2.7V–3.6V; V_{SS} = 0V; T_A (°C) = 0 to 70 for SL; -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	+0.6	V
Input High Voltage	V _{IH}	-	+2.0	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-1	+1	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{\text{CS}}$ = V _{IH} (min.) or $\overline{\text{OE}}$ = V _{IH} (min.) or $\overline{\text{WE}}$ = V _{IL} (max.)	-1	+1	μA
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.2	-	V

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Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Current	I _{DD}	$\overline{CS} = V_{IL} \text{ (max.)}$, I/O = 0 mA, Cycle = min. Duty = 100%	-	-	40	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH} \text{ (min.)}$, Cycle = min. Duty = 100%	-	-	1	mA
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	0.5	3	μA

Note: Typical parameter is measured under ambient temperature $T_A = 25^\circ C$ and $V_{DD} = 5V/3V$.

CAPACITANCE

($V_{DD} = 3.3V$, $T_A = 25^\circ C$, $f = 1 \text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	C _{I/O}	$V_{OUT} = 0V$	8	pF

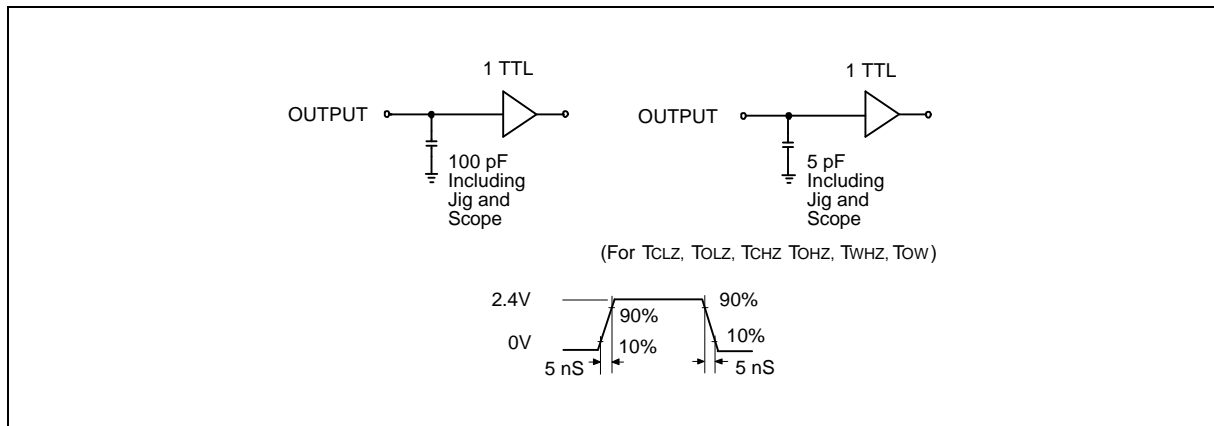
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform



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AC Characteristics, continued

(V_{DD} = 2.7V–3.6V; V_{SS} = 0V; T_A (°C) = 0 to 70 for SL; -20 to 85 for LE; -40 to 85 for LI)

Read Cycle

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Hold from Address Change	TOH	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write Cycle Time	TWC	70	-	nS
Chip Selection to End of Write	TCW	50	-	nS
Address Valid to End of Write	TAW	50	-	nS
Address Setup Time	TAS	0	-	nS
Write Pulse Width	TWP	50	-	nS
Write Recovery Time	\overline{CS} , \overline{WE} TWR	0	-	nS
Data Valid to End of Write	TDW	40	-	nS
Data Hold from End of Write	TDH	0	-	nS
Write to Output in High Z	TWHZ*	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	25	nS
Output Active from End of Write	TOW	5	-	nS

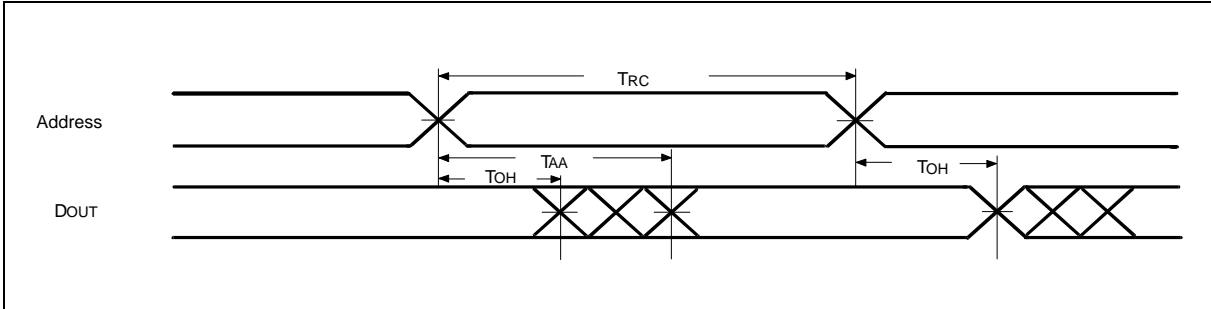
* These parameters are sampled but not 100% tested



TIMING WAVEFORMS

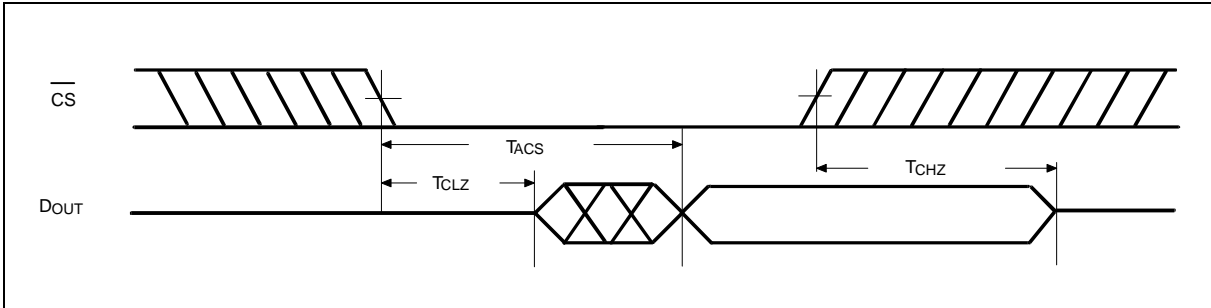
Read Cycle 1

(Address Controlled)



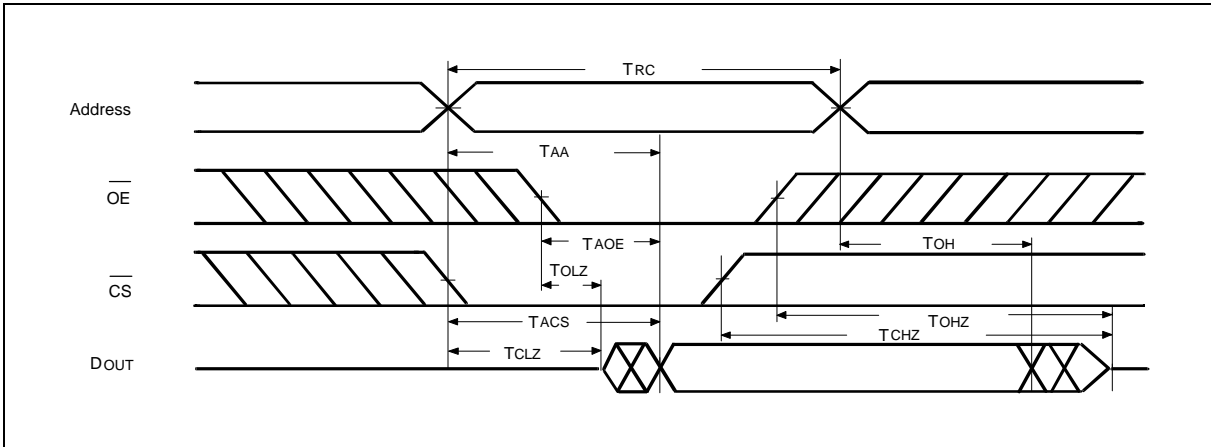
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)

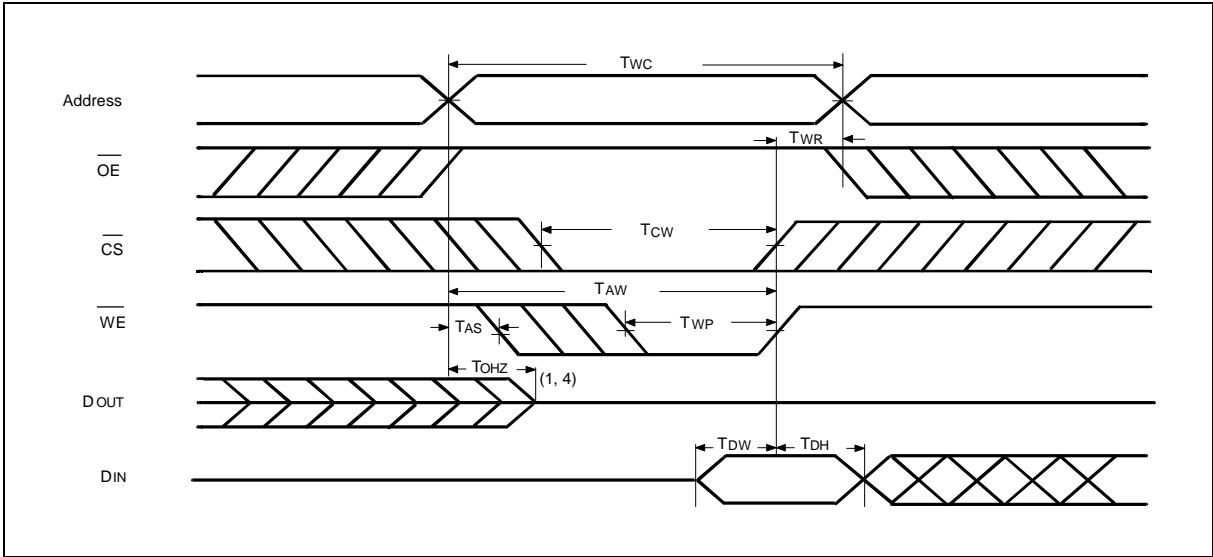


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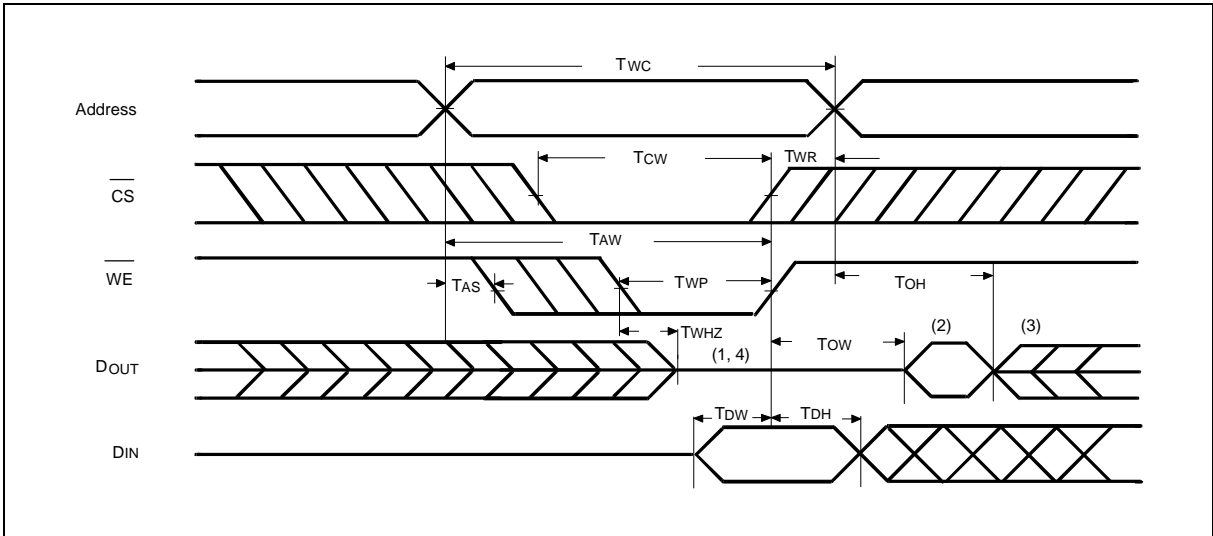
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

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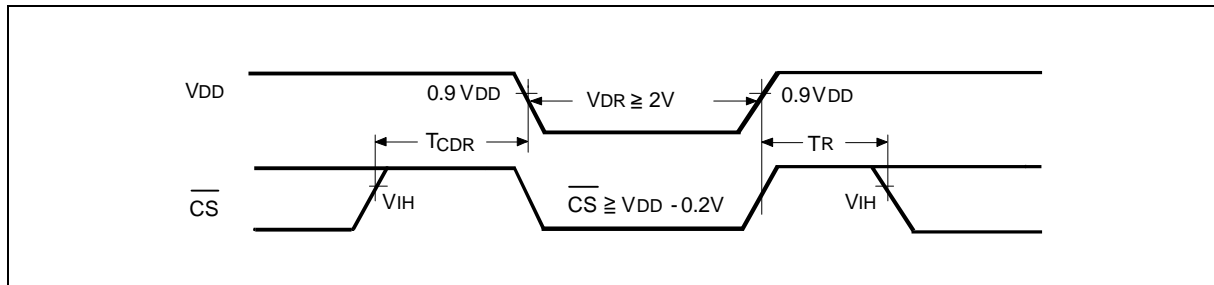
DATA RETENTION CHARACTERISTICS

(TA (°C) = 0 to 70 for SL; -20 to 85 for LE; -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3V$	-	-	3	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	PACKAGE
W24LH8-70SL	70	2.7V to 3.6V	0 to 70	600 mil DIP
W24LH8S-70SL	70	2.7V to 3.6V	0 to 70	330 mil SOP
W24LH8Q-70SL	70	2.7V to 3.6V	0 to 70	Standard type one TSOP
W24LH8-70LE	70	2.7V to 3.6V	-20 to 85	600 mil DIP
W24LH8S-70LE	70	2.7V to 3.6V	-20 to 85	330 mil SOP
W24LH8Q-70LE	70	2.7V to 3.6V	-20 to 85	Standard type one TSOP
W24LH8-70LI	70	2.7V to 3.6V	-40 to 85	600 mil DIP
W24LH8S-70LI	70	2.7V to 3.6V	-40 to 85	330 mil SOP
W24LH8Q-70LI	70	2.7V to 3.6V	-40 to 85	Standard type one TSOP

Notes:

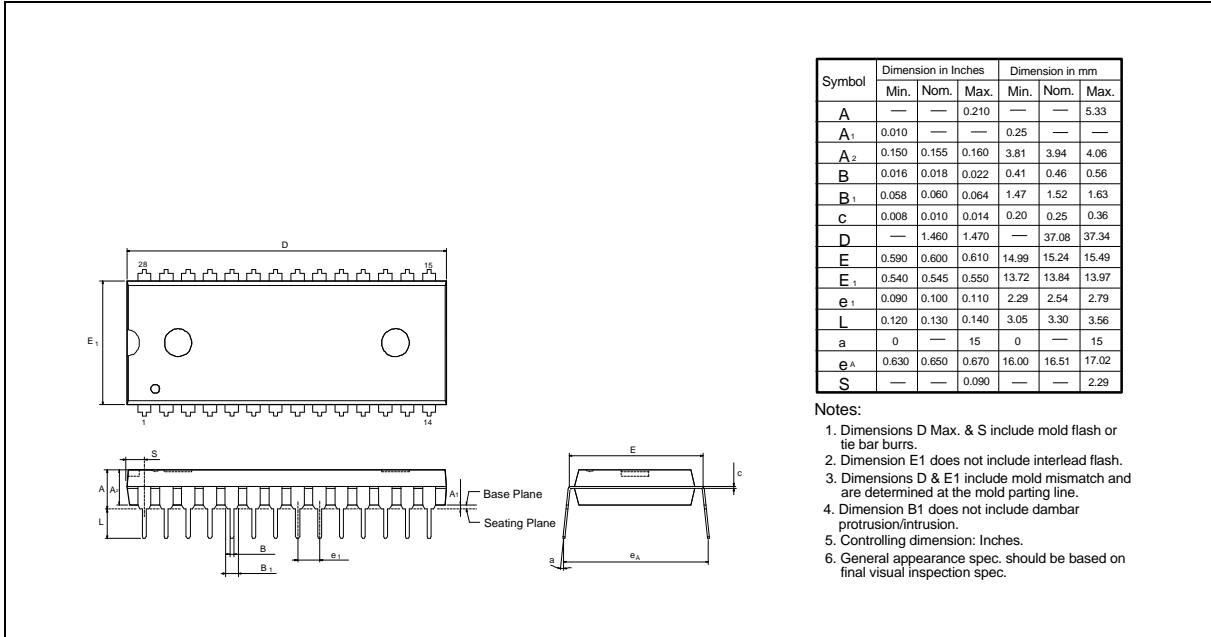
- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

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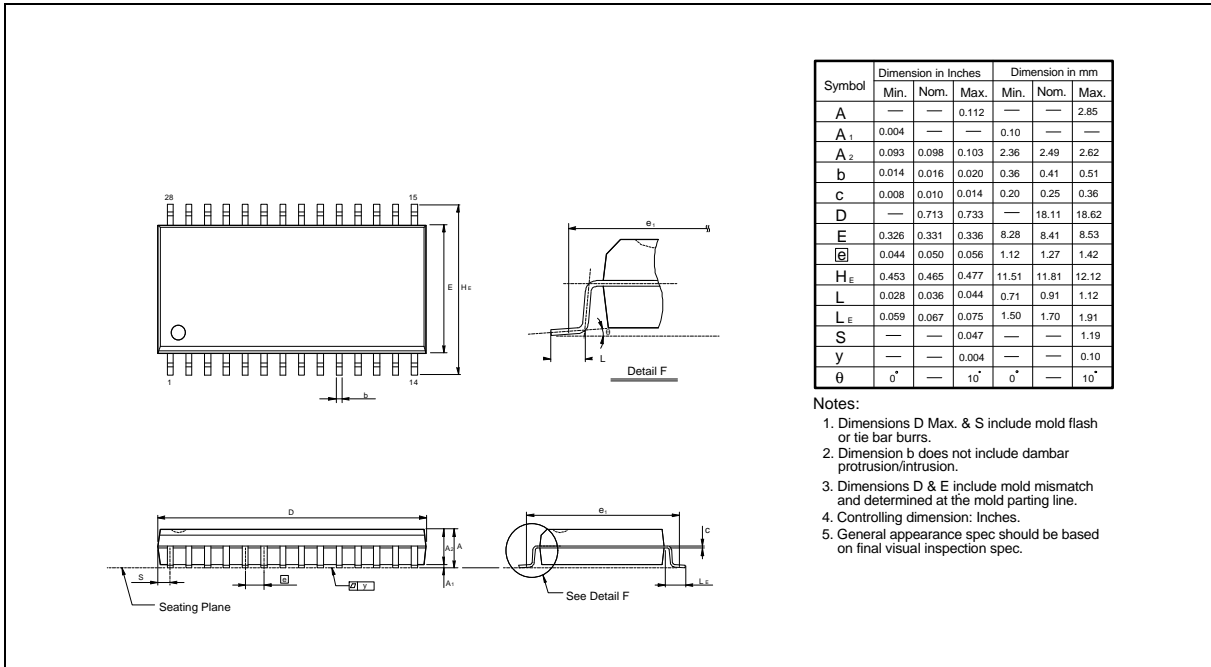
Revision A2

PACKAGE DIMENSIONS

28-pin P-DIP

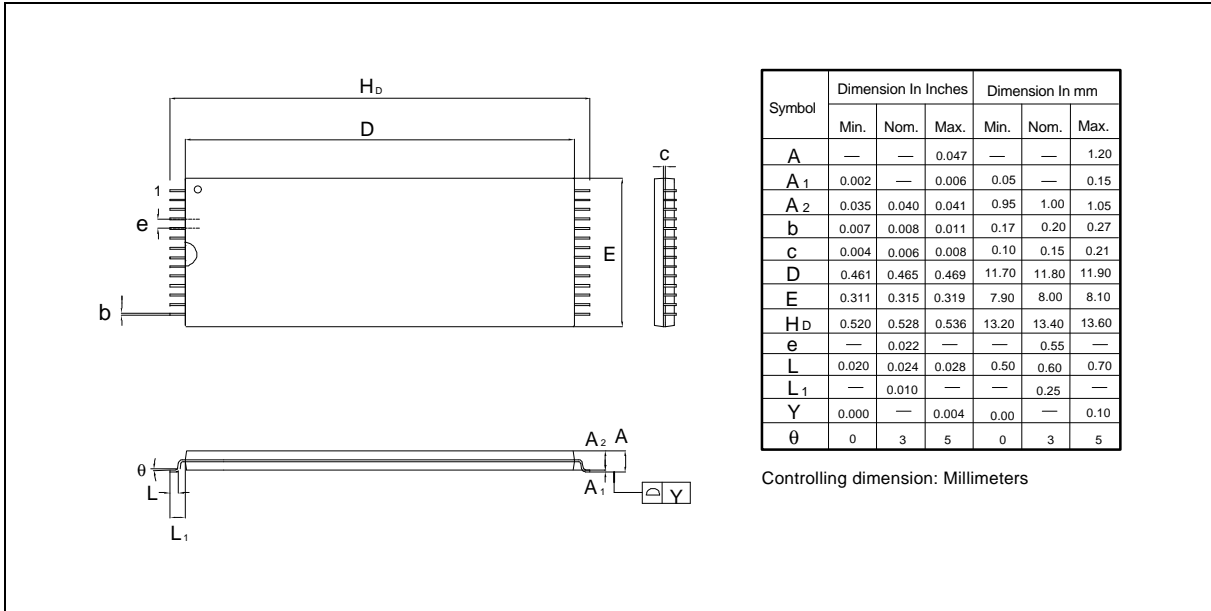


28-pin SOP Wide Body



Package Dimensions, continued

28-pin Standard Type One TSOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 1998	-	Initial Issued
A2	Jan. 1999	1	Change low power consumption active: from 108 to 156 mW (max.)
		3	Change operating power supply current (IDD) from 30 to 40 mA (max.)



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.