SGS-THOMSON
MICROELECTRONICS

STE100N20

N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR IN ISOTOP PACKAGE

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STE100N20	200 V	< 0.021 Ω	100 A

- HIGH CURRENT POWER MODULE
- AVALANCHE RUGGED TECHNOLOGY (SEE STH33N20FI FOR RATING)
- VERY LARGE SOA - LARGE PEAK POWER CAPABILITY
- EASY TO MOUNT
- SAME CURRENT CAPABILITY FOR THE TWO SOURCE TERMINALS
- EXTREMELY LOW R_{th} JUNCTION TO CASE
- VERY LOW DRAIN TO CASE CAPACITANCE
- VERY LOW INTERNAL PARASITIC INDUCTANCE (TYPICALLY < 5 nH)
- ISOLATED PACKAGE UL RECOGNIZED (FILE No E81743)

INDUSTRIAL APPLICATIONS:
- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS

ISOTOP

INTERNAL SCHEMATIC DIAGRAM
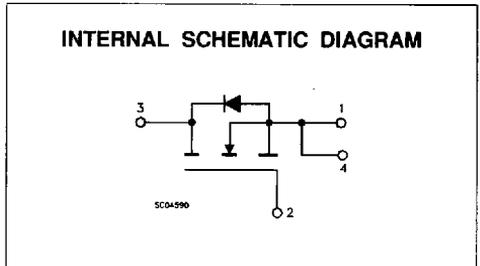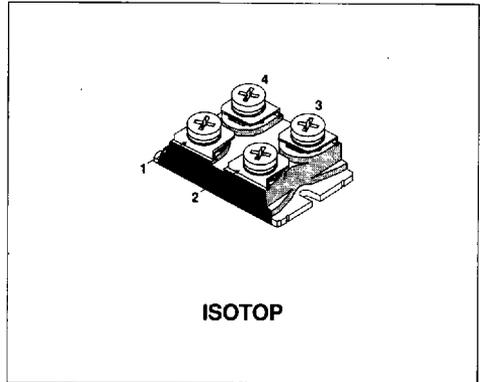
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0$)	200	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} = 20$ kΩ)	200	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current (continuous) at $T_c = 25\ ^oC$	100	A
I_D	Drain Current (continuous) at $T_c = 100\ ^oC$	65	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	400	A
P_{tot}	Total Dissipation at $T_c = 25\ ^oC$	450	W
	Derating Factor	3.6	W/^oC
T_{stg}	Storage Temperature	-55 to 150	^oC
T_j	Max. Operating Junction Temperature	150	^oC
V_{ISO}	Insulation Withstand Voltage (AC-RMS)	2500	V

($\bullet$) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.27	°C/W
R_{thc-h}	Thermal Resistance Case-heatsink With Conductive Grease Applied	Max	0.05	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA V_{GS} = 0 V	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125 °C			400 2	µA mA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 400	nA

ON (∗)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 1 mA	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 60 A			0.021	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (∗)	Forward Transconductance	V_{DS} = 15 V I_D = 60 A	38			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0 V			12 3200 1200	nF pF pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 100 V I_D = 50 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 1)		75 140		ns ns
$(di/dt)_{on}$	Turn-on Current Slope	V_{DD} = 160 V I_D = 100 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		480		A/µs
Q_g	Total Gate Charge	V_{DD} = 160 V I_D = 100 A V_{GS} = 10 V		505		nC

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 160 V I_D = 100 A		230		ns
t_f	Fall Time	R_G = 4.7 Ω V_{GS} = 10 V		155		ns
t_c	Cross-over Time	(see test circuit, figure 3)		370		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				100	A
I_{SDM}(•)	Source-drain Current (pulsed)				400	A
V_{SD} (∗)	Forward On Voltage	I_{SD} = 100 A V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 100 A di/dt = 100 A/μs		580		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 30 V T_j = 150 °C (see test circuit, figure 3)		3.5		μC
I_{RRM}	Reverse Recovery Current			12		A

(∗) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

Safe Operating Area   Thermal Impedance
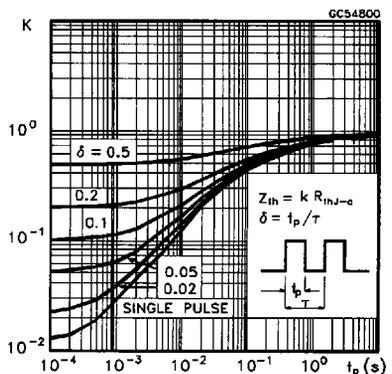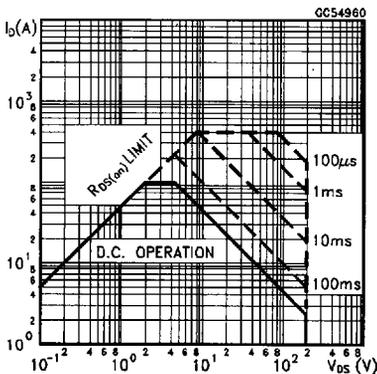
Derating Curve
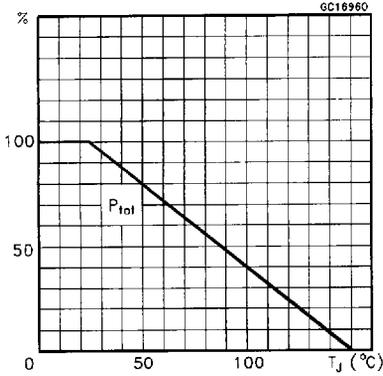
Output Characteristics
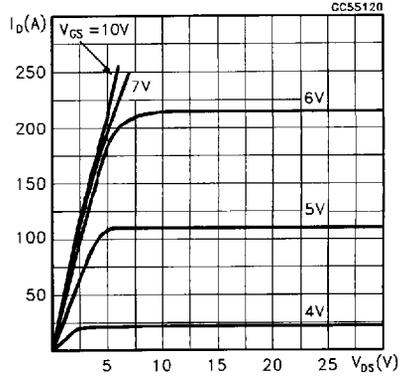

Transfer Characteristics
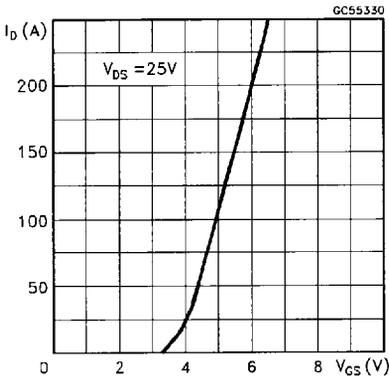
Transconductance
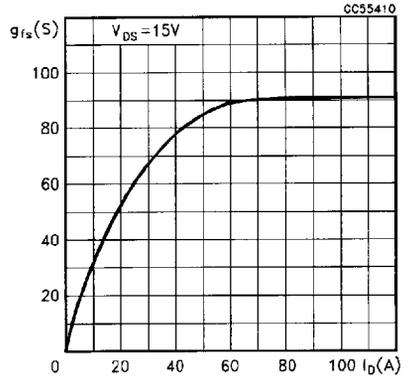

Static Drain-source On Resistance
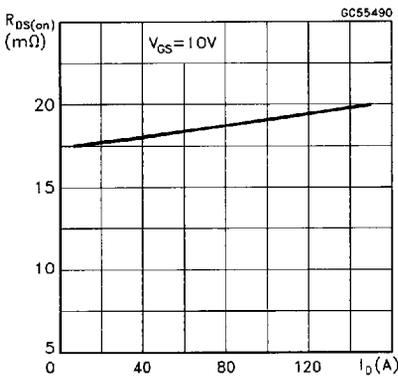
Gate Charge vs Gate-source Voltage

SGS-THOMSON
MICROELECTRONICS
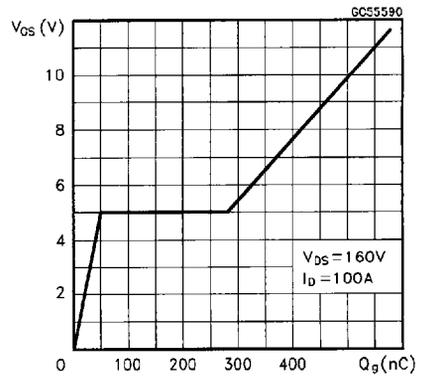
Capacitance Variations
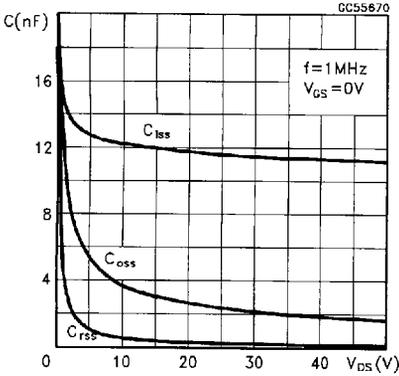
Normalized Gate Threshold Voltage vs Temperature
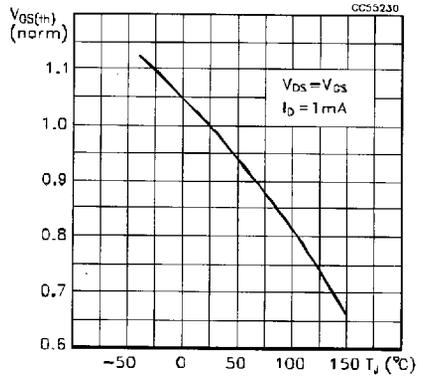

Normalized Breakdown Voltage vs Temperature
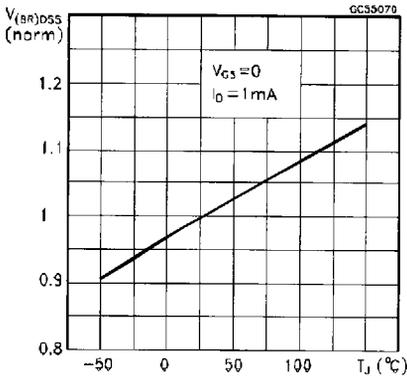

Normalized On Resistance vs Temperature
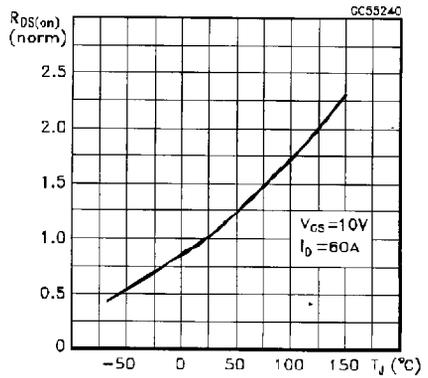
Turn-on Current Slope
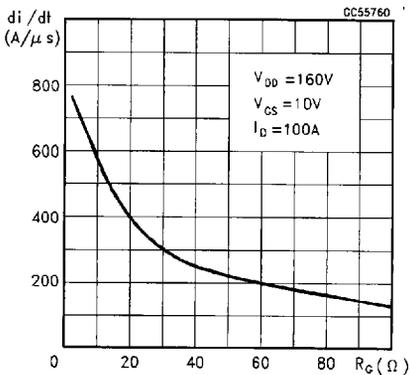
Turn-off Drain-source Voltage Slope

Cross-over Time

Source-drain Diode Forward Characteristics
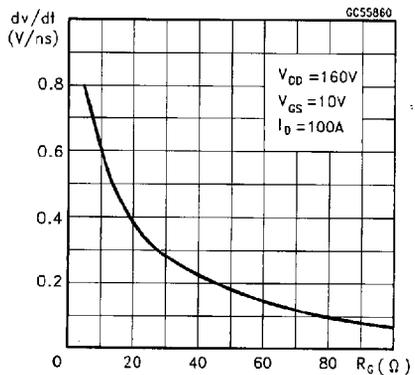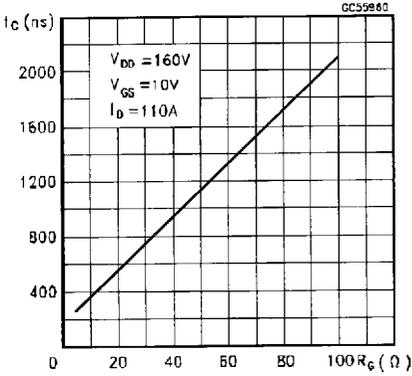
Fig. 1: Switching Times Test Circuits For Resistive Load
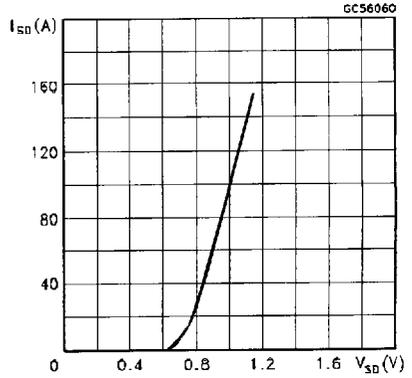
Fig. 2: Gate Charge Test Circuit
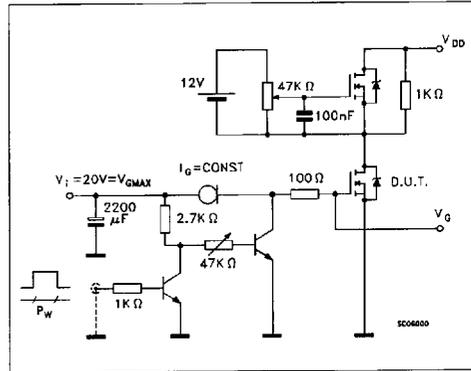
Fig. 3: Test Circuit For Inductive Load Switching And Diode Recovery Times

SGS-THOMSON
MICROELECTRONICS