TEXAS INSTRUMENTS

TSB15LV01

Video Signal Processor With IEEE-1394 Link Layer Controller

Data Manual

2000

Mixed Signal Products

SLLS425

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1 Introduction

The TSB15LV01 is a video signal processor integrated with a 1394 link layer controller. It is designed to be the center of a host-controlled, full-motion color camera when coupled with a 1394 PHY, CCD sensor and driver, analog front end, and an external EEPROM device. A camera based on the TSB15LV01 is compliant with the IEEE 1394a standard and the 1394 Trade Association's Digital Camera specification, Draft 1.04.

The TSB15LV01 offers the advantage of 24-bit true-color digital video processing. This gives superior video quality at higher sustained data rates. Isochronous transfer of the video data and asynchronous control of the camera are accomplished via the 1394 high-speed serial bus, operating at data rates of up to 400 Mbits/s. This bus allows noncompressed full-motion digital video at rates of 30 frames/sec. Use of this serial connection eliminates the need for expensive video capture cards. The chipset supports the YUV 4:1:1, YUV 4:2:2, YUV 4:4:4, and RGB 24-bit formats.

The video signal processor (VSP) portion of the device incorporates proprietary digital image processing techniques, implemented with an advanced digital signal processing (DSP) ASIC. These techniques enable a camera to achieve excellent color accuracy and resolution. The use of a custom advanced CMOS ASIC process allows for both the advanced digital image processing techniques and for advanced color space conversion. This allows the multiple output formats required for a multipurpose video conferencing camera. Use of this advanced, low-power CMOS process also enables the camera to be powered by a notebook computer operating on battery power. The device is designed to work with CCDs that have a pixel resolution of 640(H) y 480(V). This resolution meets the VGA square pixel standards.

The 1394 link layer controller is capable of up to 400 Mbits/s operation and is compatible with both the IEEE 1394–1995 and 1394a standards. The TSB15LV01 implements all registers and address space required by the 1394 Trade Association's Digital Camera specification, Draft 1.04 (hereafter referred to as the Digital Camera Specification).

The device supports packet speeds of up to 400 Mbits/s, but the maximum bandwidth consumed by the device is 200 Mbits/s. This means that a TSB15LV01-based camera leaves at least 200 Mbits/s available to other functions.

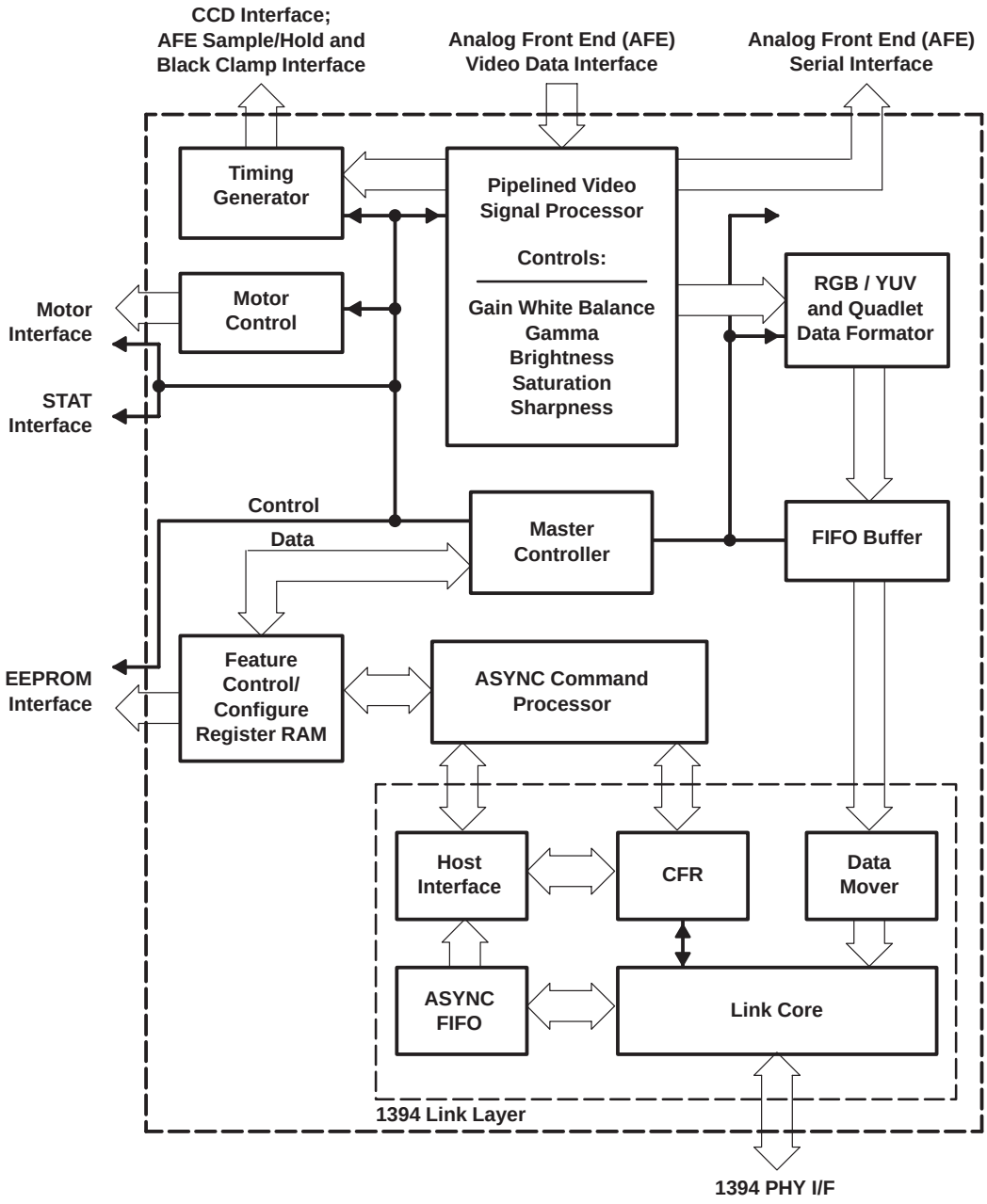
With its balance of features and low cost, a system based on TSB15LV01 is well-suited for applications such as:

- PC Video Camera
- Video Conferencing
- Video Capture
- Still Picture Capture
- Set-Top Boxes
- Video Phone
- Gaming
- Webcam
- Robotics
- Security

1.1 Features

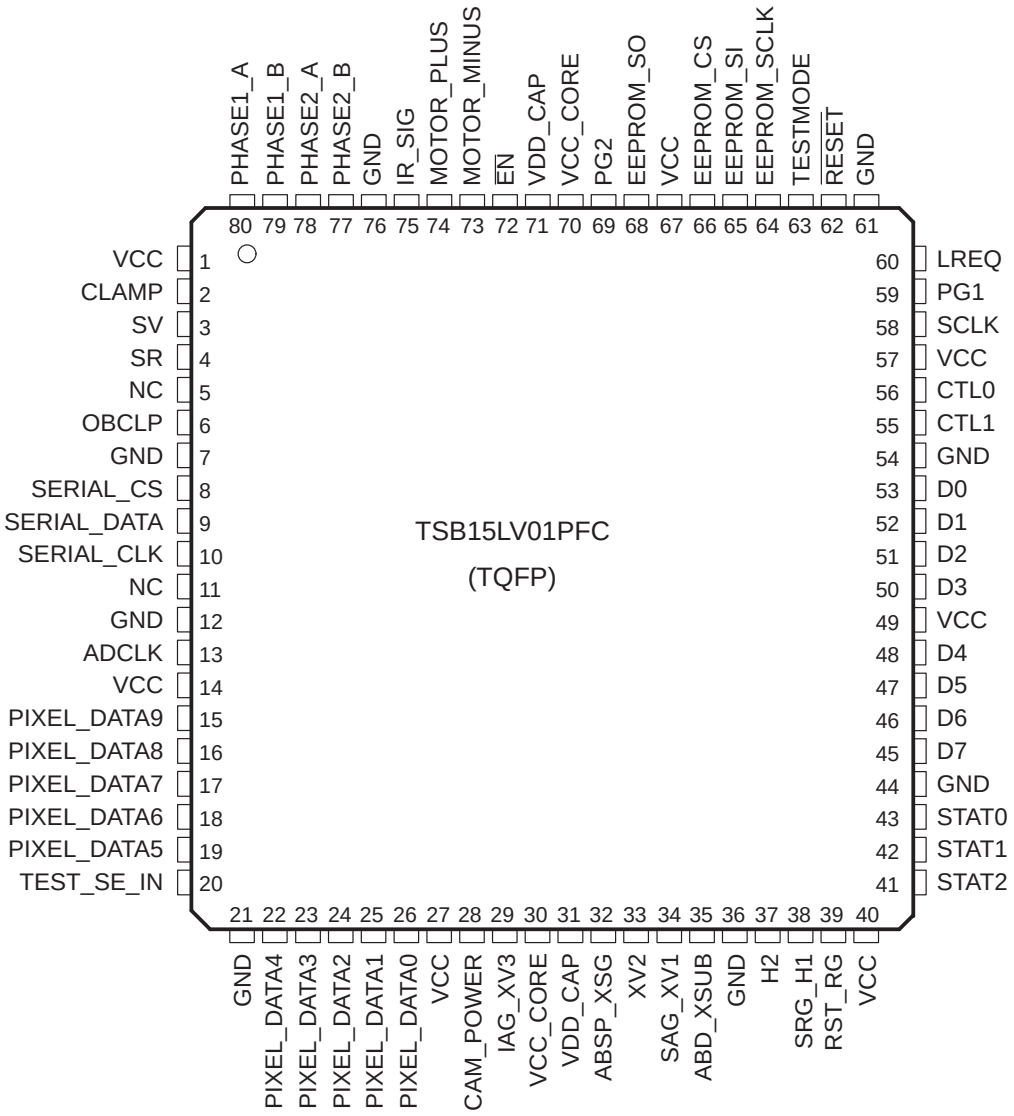
- Compatible With 1394 Trade Association’s Digital Camera Specification, Draft 1.04
- 1394a Link Layer Controller With 400 Mbits/s Capability
- Support for Several CCD Sensors
  - Sony ICX084AK, ICX098AK
  - Sharp LZ24BP
  - Texas Instruments TC237
- Integrated CCD (Charge-Coupled Device) and CDS (Correlated Double Sampling) Pulse Timer With Programmable Pulse Skew
- Video Controls
  - Brightness (Auto/Manual)
  - Exposure (Auto/Manual)
  - Sharpness (Manual)
  - Saturation (Manual)
  - White Balance (Auto/Manual)
  - Gamma (Manual)
  - Backlight Compensation (Manual)
- Three Stepper Motor Controls for Focus/Zoom/Tilt or Other Motorized Functions
- EEPROM Interface
- Programmable Status/Test Terminals
- Seamlessly Connects to TI’s 1394 Physical Layer Devices

1.2 Functional Block Diagram



1.3 Terminal Assignments

TQFP PACKAGE
(TOP VIEW)



NC – No internal connection

1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
			Analog Front End (AFE) Interface
ADCLK	13	O	ADC clock. Triggers the AFE's analog/digital converter to sample the amplifier output, and clocks the digital data out of the AFE to the TSB15LV01.
CLAMP	2	O	Pulse that instructs AFE to electrically clamp the ac-coupled pixel pulse to a fixed reference voltage.
OBCLP	6	O	Optical Black Clamp pulse. Instructs the AFE to clamp its ADC output to a digital black reference value. Samples occur during the *black pixel* portion of the CCD's image signal.
PIXEL_DATA9– PIXEL_DATA0	15–19, 22–26	I	Data bus that inputs processed video data from the AFE's analog/digital converter. PIXEL_DATA_IN9 is the MSB of these 10 bits.
SERIAL _CS	8	O	Serial interface chip select. Allows programming of AFE control registers. Signifies the beginning of data transmission on SERIAL_DATA.
SERIAL _DATA	9	O	Serial interface digital data input. Allows programming of AFE control registers.
SERIAL _CLK	10	O	Serial interface clock. Allows programming of AFE control registers. Clocks data out of SERIAL_DATA.
SR	4	O	CCD reset-pedestal sampling pulse. Triggers the AFE to sample the reset pedestal of the pixel pulse received from the CCD image sensor.
SV	3	O	CCD video data sampling pulse. Triggers the AFE to sample the data pedestal of the pixel pulse received from the CCD image sensor.
			CCD Interface
ABD_XSUB	35	O	Image area clear bias. Goes high to clear the image area. This pulse performs an *electronic shutter* function, controlling the integration time of the CCD image. Performed at the beginning of every frame.
ABSP_XSG	32	O	Antiblack smear. Goes low to increase the pixel well size during parallel transfer.
H2	37	O	Horizontal transfer 2. Horizontal charge transfer control for CCD.
IAG_XV3	29	O	Image-area gate/vertical transfer 3. Charge transfer control for CCD.
RST_RG	39	O	Reset gate. Reset pulse for the CCD's charge-detection amplifier, generated for every pixel moved out of the CCD.
SAG_XV1	34	O	Storage-area gate/vertical transfer 1. Charge transfer control for CCD.
SRG_H1	38	O	Serial register gate/horizontal transfer 1. Horizontal charge transfer control for CCD.
XV2	33	O	Vertical transfer 2. Charge transfer control for CCD.
			PHY Interface
CTL1, CTL0	55 56	I/O	Control 1 and control 0 of the PHY-link control bus.
D[7..0]	45–48, 50–53	I/O	Data signals of the PHY-link data bus. Data is expected on D0-D1 at 100 Mbits/s, D0-D3 at 200 Mbits/s, and D0-D7 at 400 Mbits/s. D0 is the MSB.
LREQ	60	I/O	Makes bus requests and accesses to the PHY.
$\overline{\text{RESET}}$	62	I	Reset, active low. The asynchronous reset to the link controller.
SCLK	58	I	System clock. SCLK is a 49.152-MHz clock supplied by the PHY.
			EEPROM Interface
EEPROM_CS	66	O	EEPROM chip select.
EEPROM_SCLK	64	O	EEPROM serial data clock.
EEPROM_SI	65	O	EEPROM serial data output.
EEPROM_SO	68	I	EEPROM serial data input.

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
			Motor Control Interface
IR_SIG	75	I	Position feedback from infrared detectors on motorized mechanisms. Applies to the stepper motor currently selected by the STATn terminals.
MOTOR_MINUS	73	I	Negative pushbutton input. Applies to the stepper motor currently selected by the STATn terminals.
MOTOR_PLUS	74	I	Positive pushbutton input. Applies to the stepper motor currently selected by the STATn terminals.
PHASE2_B	77	O	Drive signal for stepper motors, phase 2, signal B. Applies to the stepper motor currently selected by the STATn terminals.
PHASE2_A	78	O	Drive signal for stepper motors, phase 2, signal A. Applies to the stepper motor currently selected by the STATn terminals.
PHASE1_B	79	O	Drive signal for stepper motors, phase 1, signal B. Applies to the stepper motor currently selected by the STATn terminals.
PHASE1_A	80	O	Drive signal for stepper motors, phase 1, signal A. Applies to the stepper motor currently selected by the STATn terminals.
			Miscellaneous Interface
CAM_POWER	28	O	Power switch. Toggles with bit in *CAMERA_POWER_CNTL* register, which is low upon device power up. Used to instruct system power supply to enter power saving mode.
$\overline{\text{EN}}$	72	I	Regulator enable. When low, the device supply power regulator is active. Should be kept low during normal operation.
GND	7, 12, 21, 36, 44, 54, 61, 76		Connect to ground.
NC	5, 11		No connect
PG1, PG2	59, 69		No connect
STAT2 STAT1 STAT0	41 42 43	I/O	Status signals
TEST_SE_IN	20	I	Factory test terminal. Connect to ground.
TESTMODE	63	I	Factory test terminal. Connect to ground.
			Power/Ground
VCC_CORE	30,70		Connect to 3.3 V.
VCC	1, 14, 27, 40, 49, 57, 67		Connect to 3.3 V.
VDD_CAP	31,71		Mid-supply. Connect to ground through a 0.1-μF capacitor.

2 Detailed Description

2.1 1394 Interface

The 1394 interface is used to connect the camera to external devices using the IEEE 1394 serial bus. This bus is currently capable of speeds up to 400 Mbits/s and provides adequate bandwidth in which to transmit a quality uncompressed video signal. It is assumed that the reader has a moderate level of familiarity with the 1394 serial bus.

The TSB15LV01 serves as the application, transaction, and link layers of a 1394 node. This greatly simplifies implementation of the 1394 node, since only the physical layer remains to be implemented. This can be accomplished by placing a 1394 PHY, such as the TSB41LV01, between the TSB15LV01 and the 1394 connector. The 1394 interface on the TSB15LV01 provides a glueless interface to the PHY.

Note that while the device supports s400 1394 packets, the maximum bandwidth consumed by the device is 200 Mbits/s. This means that a TSB15LV01-based camera leaves at least 200 Mbits/s available to other functions, assuming all devices on the bus use s400 packets.

This section is not designed to be a tutorial on 1394. It is assumed that the reader has a basic knowledge of the 1394 serial bus. For more information on the 1394 bus, see the 1394 standard.

2.1.1 Isochronous Versus Asynchronous Protocols

There are two types of packets used in the 1394 link layer: isochronous and asynchronous. The TSB15LV01 uses *isochronous* packets to send video data to the bus and *asynchronous* packets to exchange control/status information with the bus.

An isochronous transaction delivers a consistent amount of data that is transferred at regular 125-µs intervals, with simplified addressing. Reception of an acknowledge packet is not required. Allocated flows of isochronous data are referred to as *channels.* Because the packets are assured to be delivered regularly, a constant data rate is achieved, making it ideal for video. In order to assure this bandwidth, a node must first request allocation of the bus resources from the node serving as the bus manager. The TSB15LV01 expects this to be performed by the node receiving the video data, referred to as the *host node.* The TSB15LV01 is capable of being an isochronous *talker.* However, it is not capable of listening to a channel of isochronous data. It is capable of transmitting isochronous data on channels 0 to 15 only.

An asynchronous transaction delivers a variable amount of data to a specific address. An acknowledge packet must be received from the designated target node, assuring delivery of the packet. This protocol allows packets to be sent without any prior permission or allocation. However, isochronous packets receive priority in order to maintain a consistent data rate. The TSB15LV01 is capable of sending and receiving asynchronous packets with a payload of up to 32 quadlets per packet. All request packets received by the device are answered with a response packet. If a request packet is received between a request and its corresponding response packet, the device acknowledges that packet with a *busy* acknowledge code.

2.1.2 Packet Format/Protocol

2.1.2.1 Isochronous Packet Format/Protocol

All video data sent from the camera is done so using isochronous communication. Before data can be sent, the node residing in the host must first request allocation of bus resources from the node serving as the bus manager. It must then configure the TSB15LV01's control and configuration registers. After the first CCD image integration cycle that follows completion of configuration, the camera will begin to send video data.

The full isochronous packet structure is shown in Table 2–1. This packet structure is defined by the 1394 standard.

Table 2–1. Isochronous Data Block Packet Format

0–7	8–15	16–23		24–31	
data_length		tg	channel	tCode	sy
header_CRC					
data payload quadlet 1 data payload quadlet 2 . . . last quadlet of data payload (padded with zeroes if necessary)					
data_CRC					

The fields are defined as:

- **data_length** The number of bytes in the data payload field
- **tg** The tag field is set to zero
- **channel** The isochronous channel number, as programmed in the ISO_CHANNEL_CNTL register
- **tCode** The transaction code. The code for an isochronous data block transaction is 1010b.
- **sy** Synchronization value. For the first isochronous packet of a frame, this is set to 0001b. For all other isochronous packets, this is set to zero.
- **data payload** Contains the digital video information

Isochronous data is formatted differently for each video transfer mode. Table 2–2 lists all supported transfer modes. For each mode, the table lists the total number of bits representing a single pixel. It also gives the data payload per packet for each mode, in terms of lines, pixels, and quadlets. The payload varies for each frame rate.

Every video component, Y, U, V, R, G, and B, has 8-bit data.

Table 2–2. Data Payload Per Isochronous Packet

MODE	VIDEO FORMAT	FRAME RATE (Frame per Second)			
		30	15	7.5	3.75
Mode_0	160 x 120 YUV(4:4:4) 24 bits/pixel	1/2 L 80 P 60 Q	1/4 L 40 P 30 Q	1/8 L 20 P 15 Q	
Mode_1	320 x 240 YUV(4:2:2) 16 bits/pixel	1 L 320 P 160 Q	1/2 L 160 P 80 Q	1/4 L 80 P 40 Q	1/8 L 40 P 20 Q
Mode_2	640 x 480 YUV(4:1:1) 12 bits/pixel	2 L† 1280 P 480 Q	1 L 640 P 240 Q	1/2 L 320 P 120 Q	1/4 L 160 P 60 Q
Mode_3	640 x 480 YUV(4:2:2) 16 bits/pixel		1 L† 640 P 320 Q	1/2 L 320 P 160 Q	1/4 L 160 P 80 Q
Mode_4	640 x 480 RGB 24 bits/pixel		1 L† 640 P 480 Q	1/2 L 320P 240Q	1/4 L 160P 120Q
Mode_5	640 x 480 Y (Mono) 8 bits/pixel	2 L† 1280P 320 Q	1 L 640 P 160 Q	1/2 L 320 P 80 Q	1/4 L 160 P 40 Q

† Requires s200 or faster packet speed, as programmed in the *ISO_CHANNEL/SPEED_CNTL* register. The others can use s100 as well.

Key: L: Lines/packet
P: Pixel/packet
Q: Quadlet/packet

2.1.2.2 Isochronous Video Payload

Each transfer mode requires a different data format structure, each defining how the pixels are combined to build 32-bit quadlets. Table 2–3 shows the payload structure for each mode, with the quadlets broken down into individual bytes. This data payload structure is slightly different for every video mode. In the table, *N* is the number of pixels/packet, as shown in Table 2–2.

Table 2–3. Video Data Payload Structure

0–7	8 –15	16–23	24–31
YUV (4:4:4) format (Mode_0)			
U_0	Y_0	V_0	U_1
Y_1	V_1	U_2	Y_2
V_2	U_3	Y_3	V_3
.	.	.	.
.	.	.	.
.	.	.	.
U_{N-4}	Y_{N-4}	V_{N-4}	U_{N-3}
Y_{N-3}	V_{N-3}	U_{N-2}	Y_{N-2}
V_{N-2}	U_{N-1}	Y_{N-1}	V_{N-1}
YUV (4:2:2) format (Mode_1, Mode_3)			
U_0	Y_0	V_0	Y_1
U_2	Y_2	V_2	Y_3
U_4	Y_4	V_4	Y_5
.	.	.	.
.	.	.	.
.	.	.	.
U_{N-6}	Y_{N-6}	V_{N-6}	Y_{N-5}
U_{N-4}	Y_{N-4}	V_{N-4}	Y_{N-3}
U_{N-2}	Y_{N-2}	V_{N-2}	Y_{N-1}
YUV (4:1:1) format (Mode_2)			
U_0	Y_0	Y_1	V_0
Y_2	Y_3	U_4	Y_4
Y_5	V_4	Y_6	Y_7
.	.	.	.
.	.	.	.
.	.	.	.
U_{N-8}	Y_{N-8}	Y_{N-7}	V_{N-8}
Y_{N-6}	Y_{N-5}	U_{N-4}	Y_{N-4}
Y_{N-3}	V_{N-4}	Y_{N-2}	Y_{N-1}
RGB format (Mode_4)			
R_0	G_0	B_0	R_1
G_1	B_1	R_2	G_2
B_2	R_3	G_3	B_3
.	.	.	.
.	.	.	.
.	.	.	.
R_{N-4}	G_{N-4}	B_{N-4}	R_{N-3}
G_{N-3}	B_{N-2}	R_{N-2}	G_{N-2}
B_{N-2}	R_{N-1}	G_{N-1}	B_{N-1}

Table 2–3. Video Data Payload Structure (Continued)

0–7	8–15	16–23	24–31
Y (Mono) format (Mode_5)			
Y_0	Y_1	U_2	Y_3
Y_4	V_5	Y_6	Y_7
.	.	.	.
.	.	.	.
.	.	.	.
Y_{N-8}	Y_{N-7}	U_{N-6}	Y_{N-5}
Y_{N-4}	V_{N-3}	Y_{N-2}	Y_{N-1}

Table 2–4 shows the data structure for Y, R, G, and B video data components. All components are unsigned 8-bit values.

Table 2–4. Data Structure for Y, R, G, and B Data Components

	SIGNAL LEVEL (Decimal)	DATA (Hexadecimal)
Highest	255	0xFF
	254	0xFE
	:	:
	1	0x01
Lowest	0	0x00

Table 2–5 shows the data structure for U and V video data components. Both components are signed 8-bit values.

Table 2–5. Data Structure for U and V Data Components

	SIGNAL LEVEL (Decimal)	DATA (Hexadecimal)
Highest(+)	127	0xFF
	126	0xFE
	:	:
	1	0x81
Lowest	0	0x80
	–1	0x7F
	:	:
	–127	0x01
Highest(–)	–128	0x00

2.1.2.3 Asynchronous Packet Format/Protocol

Asynchronous packets are used to read status information from the TSB15LV01 and write control information to it. These packets are formatted as defined by the 1394 standard. All reads and writes should correlate with the memory maps as shown in section 3, Address Space.

Asynchronous reads and writes can be performed either as quadlets or as blocks. Blocks can be read in sizes of up to 32 quadlets per packet. The structure of a quadlet write request packet is shown in Table 2–6, while the structure of a block write request packet is shown in Table 2–7.

Table 2–6. Asynchronous Quadlet Write Request Packet Format

0–7	8–15	16–23		24–31	
destination_ID		tl	rt	tCode	pri
source_ID		destination_offset			
destination_offset					
quadlet data					
header_CRC					

The fields are defined as:

- **destination_ID** 10-bit busID concatenated with 6-bit nodeID
- **tl** Transaction label, specified by the host that identifies this transaction. This optional value is returned in the response packet.
- **rt** Retry code. Indicates whether this packet is an attempted retry and defines retry protocol.
- **tCode** Transaction code. The code for an asynchronous write request for quadlet data is 0000b.
- **pri** Not used.
- **source_ID** Identifies host node by specifying its bus and physical ID
- **destination_offset** Address location within TSB15LV01 address space
- **quadlet_data** Contains the value being written to the addressed location
- **header_CRC** CRC value for the header

Table 2–7. Asynchronous Block Write Request Packet Format

0–7	8–15	16–23		24–31	
destination_ID		tl	rt	tCode	pri
source_ID		destination_offset			
destination_offset					
data_length		extended_tcode (0000)			
header_CRC					
data block . . . last quadlet of data block					

The fields are defined as:

- **destination_ID** 10 bit busID concatenated with 6-bit nodeID.
- **tl** Transaction label, specified by the host that identifies this transaction. This optional value is returned in the response packet.
- **rt** Retry code. Indicates whether this packet is an attempted retry and defines retry protocol.
- **tCode** Transaction code. The code for an asynchronous write request for block data is 0001b.
- **pri** Not used.
- **source_ID** Identifies host node by specifying its bus and physical ID
- **destination_offset** Address location within TSB15LV01 address space
- **data length** Specifies the amount of data being sent in the data field. Maximum size is 128 bytes.
- **extended_tcode** Reserved during write request packets
- **header_CRC** CRC value for the header
- **data_field** Contains the value being written to the addressed location
- **data_CRC** CRC value for the data field

The structure of a quadlet read request packet is shown in Table 2–8, while the structure of a block read request packet is shown in Table 2–9.

Table 2–8. Asynchronous Quadlet Read Request Packet Format

0–7	8–15	16–23		24–31	
destination_ID		tl	rt	tCode	pri
source_ID		destination_offset			
destination_offset					
header_CRC					

The fields are defined as:

- **destination_ID** 10-bit busID concatenated with 6-bit nodeID
- **tl** Transaction label is specified by the host that identifies this transaction. This optional value is returned in the response packet.
- **rt** Retry code. Indicates whether this packet is an attempted retry and defines retry protocol.
- **tCode** Transaction code. The code for an asynchronous read request for quadlet data is 0100b.
- **pri** Not used.
- **source_ID** Identifies host node by specifying its bus and physical ID
- **destination_offset** Address location within TSB15LV01 address space
- **header_CRC** CRC value for the header

Table 2–9. Asynchronous Block Read Request Packet Format

0–7	8–15	16–23		24–31	
destination_ID		tl	rt	tCode	pri
source_ID		destination_offset			
destination_offset					
data_length		extended_tcode (0000h)			
header_CRC					

The fields are defined as:

- **destination_ID** 10-bit busID concatenated with 6-bit nodeID.
- **tl** Transaction label is specified by the host that identifies this transaction. This value is reflected in the response packet that corresponds to this request packet.
- **rt.** Retry code. Indicates whether this packet is an attempted retry and defines retry protocol.
- **tCode** Transaction code. The code for an asynchronous read request for block data is 0101b.
- **pri** Not used
- **source_ID** Identifies host node by specifying its bus and physical ID
- **destination_offset** Address location within TSB15LV01 address space
- **data_length** Specifies the amount of data being sent in the data field. Maximum size is 128 bytes.
- **extended_transaction_code** Reserved during write request packets
- **header_CRC** CRC value for the header

2.1.3 1394 Serial Bus Management Capabilities

Nodes on the 1394 bus may be called on to serve in a number of bus management roles following a bus reset event. The TSB15LV01 is not designed to serve as the isochronous resource manager, a full bus manager, or the cycle master. The contents of the configuration ROM should reflect this level of capability.

2.1.4 PHY/Link Interface

The PHY/link interface consists of the signals that connect the TSB15LV01, which serves as the link layer of the 1394 node, to a physical layer device, or PHY. This interface carries all data, control, and status information that is transferred between the two layers.

To take full advantage of the TSB15LV01's capabilities, a 400-Mbits/s PHY device should be used, such as TI's TSB41LV01.

2.1.4.1 Principles of Operation

The TSB15LV01 PHY/link interface consists of the SCLK, CTL0-CTL1, D0-D7, LREQ, and RESET terminals. The PHY's SYSCLK terminal provides a 49.152-MHz interface clock to the TSB15LV01's SCLK terminal. All control and data signals are synchronized to, and sampled on, the rising edge of SYSCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the PHY and TSB15LV01.

The D0-D7 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the devices. In s100 operation only the D0 and D1 terminals are used; in s200 operation only the D0-D3 terminals are used; and in s400 operation all D0-D7 terminals are used for data transfer. When the PHY is in control of the D0-D7 bus, unused Dn terminals are driven low during s100 and s200 operations. When the TSB15LV01 is in control of the D0-D7 bus, unused Dn terminals are ignored by the PHY.

The LREQ terminal is used by the TSB15LV01 to send serial service requests to the PHY in order to request access to the serial-bus for packet transmission.

The PHY normally controls the CTL0-CTL1 and D0-D7 bidirectional buses. The TSB15LV01 is allowed to drive these buses only after it has been granted permission to do so by the PHY. There are three operations that may occur on the PHY-link interface: link service request, data transmit, and data receive. The TSB15LV01 issues a service request when it wants to request the PHY to gain control of the 1394 serial bus in order to transmit a packet.

The PHY may initiate a status transfer autonomously. The PHY initiates a receive operation whenever a packet is received from the 1394 serial bus. The PHY initiates a transmit operation after winning control of the serial bus following a bus request by the TSB15LV01. The transmit operation is initiated when the PHY grants control of the interface to the TSB15LV01.

For details on how the PHY/link interface operates, consult the 1394 specification.

2.1.5 Enabling the Transmission of Video

2.1.5.1 Enabling Isochronous Video Streaming

To enable the streaming of isochronous video data, the function control registers must be configured properly, as described in section 3.3.3.1.2. The last register to be written should be the *CAMERA_POWER_CNTL* register, which asserts the CAM_POWER terminal (activating the CCD circuitry, if the signal is utilized), begins processing data from the AFE interface, and begins transmitting isochronous data.

2.1.5.2 Enabling One-Shot Video Transmission

Alternatively to transmitting an isochronous stream of video data, the one-shot feature can be utilized. With this feature, a single frame is sent using the same isochronous packet structure. It is activated by asserting the *one_shot* field of the *ONE_SHOT_CNTL* register. Note that in order to use this feature, isochronous video streaming should be disabled via the *ISO_EN_CNTL* register.

When the feature is activated, the device automatically powers up the camera, activates isochronous transmission, sends a single image, then deactivates isochronous data and powers down the camera.

2.2 Sensor Interface

The TSB15LV01 obtains its raw video data from a charge-coupled device (CCD) sensor. This information is sent to an analog front end (AFE) that amplifies the analog video information provided by the CCD, performs correlated double sampling (CDS) and gain, and converts it to a digital format recognizable by the TSB15LV01.

Figure 2-1 shows the top-level signal flow in the sensor interface.

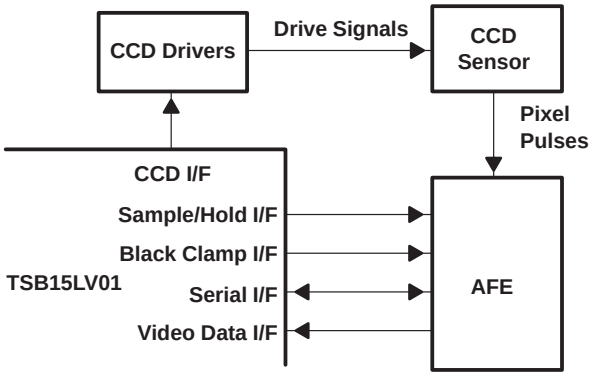


Figure 2–1. Top-Level Sensor Interface Signal Flow

2.2.1 CCD Interface

2.2.1.1 General Description

The video data is sourced by a CCD sensor. The TSB15LV01 contains a CCD timing generator for the approved sensors. Some of these signals must pass through a driver circuit to undergo voltage shifting.

Because the timing of the CCD interface is closely integrated with the timing of the analog front end, this topic is discussed jointly in section 2.2.3, *CCD/AFE Timing*.

2.2.1.2 Configuring for Different CCD Sensors

The TSB15LV01 is designed to be used with several different CCD sensors and contains the necessary logic to drive each of them. The *ccd_sel* field of the *AFE_SETUP_CNFG* register must be set to the correct value, identified in section 3.3.3.2, Configuration Registers. If this field selects the TC237 CCD, field *color_bw* of *VIDEO_OPTIONS_CNFG* register must also be set to *black and white*, since this is a black and white sensor. Otherwise, it should be set to *color*.

2.2.1.3 External Pulse Drivers

As with nearly all CCD applications, the TSB15LV01 requires use of a dedicated driver chip for the vertical drive pulses. This device performs level-shifting to high-voltage rails, as well as some logic functions. Table 2–10 shows the approved sensors with their recommended driver devices.

Table 2–10. Approved CCD Sensors and Recommended Drivers

SENSOR	DRIVER
Sony ICX084AK 1/3” color sensor	Sony CXD1267AN
Sony ICX098AK 1/4” color sensor	Sony CXD1267AN
Sharp LZ24BP 1/4” color sensor	Sony CXD1267AN or Sharp LR36685N
TI TC237 1/3” black and white sensor	TI TMC57253

In addition, an external driver for horizontal pulses is required in order to drive the capacitive load of the CCD sensor. A CMOS inverter device is recommended, such as the TI SN74LVCU04A.

2.2.2 Analog Front End Interface

Circuitry must be used in a TSB15LV01-based system that processes the pixel pulses received from the CCD and converts them to digital data readable by the TSB15LV01. This circuit is referred to as the analog front end (AFE). The TSB15LV01 is designed to be used with the TLV990 AFE device.

2.2.2.1 AFE Function

Figure 2-2 shows the block diagram of the TLV990.

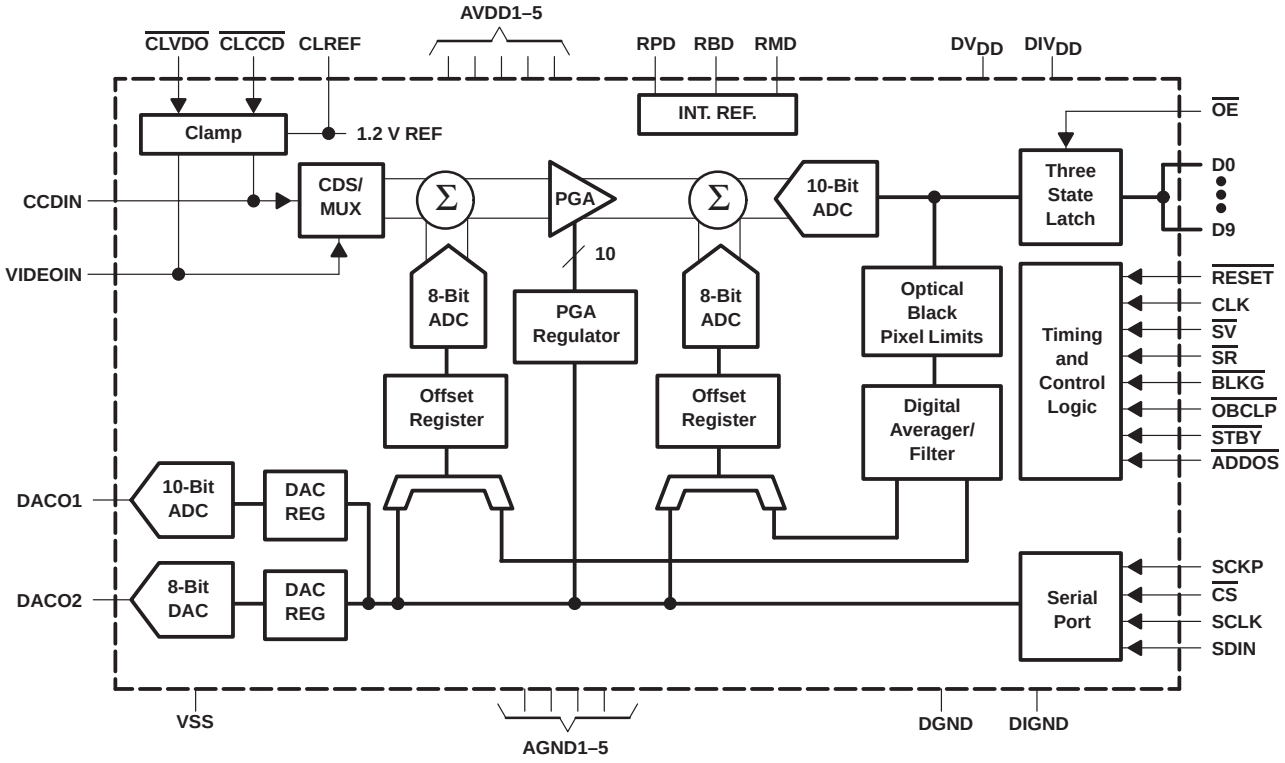


Figure 2–2. TLV990 Block Diagram

At the beginning of each image line, the AFE resets the dc bias of the incoming video data. It then performs correlated double sampling (CDS), which effectively extracts the video data from the pixel pulse and removes the most significant forms of noise. It then enters a programmable gain array (PGA) prior to conversion to digital form via a 10-bit analog/digital converter (ADC).

Before and after the PGA are offset correction circuits that maximize dynamic range of the video signal. The one prior to the PGA is considered the *coarse* adjustment offset, while the one after the PGA is considered the *fine* adjustment offset. These offset values are based either on the internal black clamping process or on values received from the TSB15LV01 via the serial interface, depending on the brightness mode. Digital/analog converters (DACs) in the AFE circuitry decode these values and apply them to the video signal flow. The TLV990 also contains a number of other registers that control operation of the device, which the TSB15LV01 is able to program.

The TSB15LV01 contains an interface to the AFE that is divided into four sections. The first is the sample/hold interface, which provides the timing signals necessary for sampling of the pixel pulses. The second is the black clamping interface. The third is the serial interface, which programs control values into the AFE. The fourth is the video data interface, which is a 10-bit parallel port that receives the video from the ADC after it has been converted.

2.2.2.2 Sample/Hold Interface

This interface provides the signals necessary for dc bias clamping and correlated double sampling (CDS) of the CCD pixel pulse.

The AFE should be capacitively coupled to the CCD output signal. At the beginning of each image line, the AFE must clamp this signal to a reference voltage, thereby properly setting the dc bias of the incoming video data. To accomplish this, the TSB15LV01 sends the CLAMP terminal low. This occurs during the CCD's dummy pixel output, prior to the active data pixels. CLAMP is held low only for a few pixels, but due to very low leakage current from this node, the clamped bias holds for the duration of the line.

During the active pixels portion of the line, reset pedestal and video data pedestal of the pixel pulses are sampled. The data pedestal is subtracted from the reset pedestal prior to amplification. The SR signal supplies the sampling pulse for the reset pedestal, while SV supplies the sampling pulse for the video data pedestal.

2.2.2.3 Black Clamping Interface

The dc offset is directly related to the brightness of the image. The dc offset can be controlled automatically or manually. When the TSB15LV01 is configured for autobrightness, it utilizes the black clamping feature of the TLV990.

In autobrightness mode, the AFE uses an internal feedback loop to adjust the offset. It adjusts the black pixels until they match a digital value received from the TSB15LV01 via the serial interface. When the TSB15LV01 sends the OBCLP terminal low, the AFE begins to acquire the digital pixel values produced by the ADC, average them, and compare them to the black reference value. If the values are not equal, the AFE attempts to make them equal by altering the *fine* adjustment offset value, which changes the offset that is summed with the signal prior to the ADC. If the necessary adjustment is out of range for the fine offset, the AFE can use the *coarse* adjustment. The adjustments are applied until the pixel data equals the black reference value.

The TSB15LV01 sends the OBCLP pulse during a time in which it knows the selected CCD is sending its *black* pixels. The number of lines per image and the number of pixels per line that should be sampled are stored in internal registers, programmed by the TSB15LV01 from the *lines_smpl* and *pix_smpl* fields, respectively, of the *VIDEO_OPTIONS_CNFG* register.

See section 2.6.6, *Brightness*, for more information on dc offset control.

2.2.2.4 Serial Interface

The TLV990 contains several control registers. The serial interface of the TSB15LV01 provides a means of programming these values. Table 2–11 shows the values that are transmitted from the TSB15LV01 to the TLV990.

Table 2–11. Values Transmitted to AFE via Serial Interface

Source Within the TSB15LV01	TLV990 Target Register	Covered in Section…
Gain/exposure control loop (auto mode)	PGA register	2.6.8, Gain and Exposure
GAIN_CNTL register (manual mode)		
Blooming_value field of *DAC_OFFSET_CNFG* register	User DAC1 register	2.6.7, Anti-Blooming
Brightness control loop (auto mode)	Coarse dc offset DAC register	2.6.6, Brightness
BRIGHTNESS_CNTL register (manual mode)		
Brightness control loop (auto mode)	Fine dc offset DAC register	
BRIGHTNESS_CNTL register (manual mode)		
Offset_level field of *DAC_OFFSET_CNFG* register	Optical black level register	
Lines_smpl field of *AFE_SETUP_CNFG* register	Optical black calibration register	
pixels_smpl field of *AFE_SETUP_CNFG* register		

Gain and offset (brightness) sources depend on whether the respective modes are manual or automatic.

The *lines_smpl* and *pix_smpl* fields of *AFE_SETUP_CNFG* register control the lines per image, and pixels per line, respectively, that are to be averaged (see section 2.2.2.3, *Black Clamping Interface*, for more information). The *offset_level* field of the *DAC_OFFSET_CNFG* register is the digital black reference value to which the dc offset is normalized.

The TLV990 contains two general purpose DACs with external outputs. One of these, DAC1, can be used to convert a digital code (sourced from the TSB15LV01's *DAC_OFFSET_CNFG* register) to an analog signal, which can be routed to the sensor for use in antiblooming. The second DAC, DAC2, is generally not utilized, but can be controlled from the TSB15LV01 as well.

See the TLV990 data sheet (literature number SLAS298) for more information about the target registers.

The timing of the AFE serial interface is shown in Figure 2–3. Table 2–12 shows the AFE interface timing parameters.

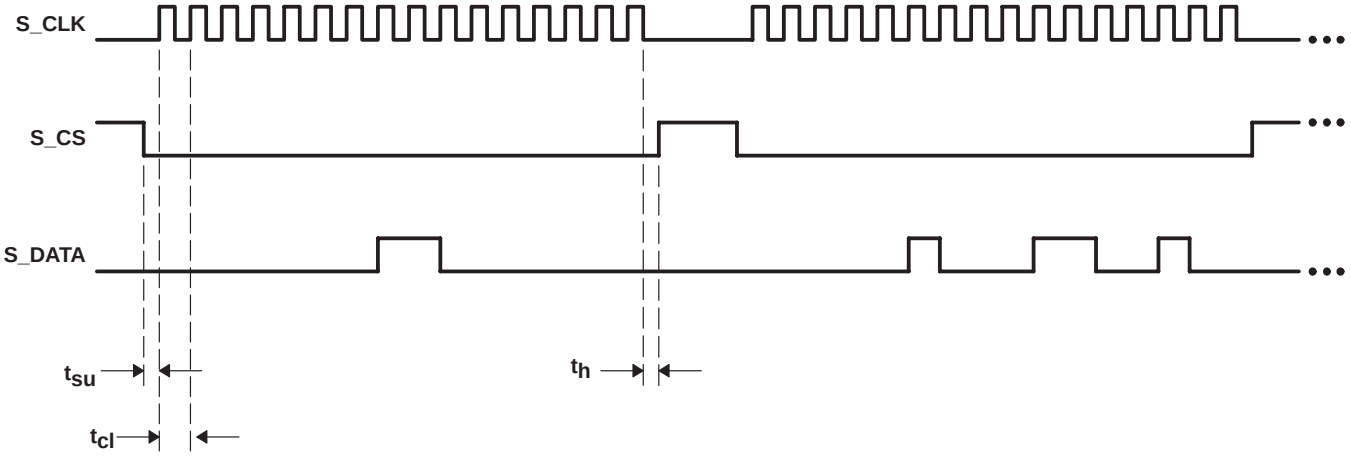


Figure 2–3. AFE Serial Interface Timing

Table 2–12. AFE Interface Timing Parameters

	MIN	TYP	MAX	UNIT
t_{su}		82		ns
t_{cl}		164		ns
t_h		82		ns

In Figure 2-3, two words are being written by the TSB15LV01 to the AFE. Each word represents a value being written to an AFE register address. The number of values written depends on the mode. For example, if autoexposure is being used, different parameters are being programmed to the AFE than if the mode is manual.

2.2.2.5 Video Data Interface

A 10-bit parallel interface is used to move the video data from the AFE ADC to the TSB15LV01. Data is clocked in with ADCLK.

2.2.3 CCD/AFE Timing

2.2.3.1 General Description

The timing of these interfaces takes into consideration two asynchronous, periodic events. The first event is the integration of light in the sensor, which occurs at a frequency dictated by the camera's frame rate. The second event is the beginning of a 1394 isochronous cycle, which determines when video data is transmitted from the TSB15LV01. The TSB15LV01 reconciles these two events in a way that produces optimal video quality while minimizing the amount of memory necessary to store the pixel data.

When the integration cycle is complete, the pixel charges are transferred out of the active region of the sensor. For the TC237, which is a full frame transfer CCD, this is the parallel transfer of charge from the image area to the storage area. For the other sensors, which are interline CCDs, this is the transfer of charge to the vertical shift registers. Several dummy/black lines are subsequently clocked and processed by the AFE.

At this point, timing waits for the next 1394 isochronous cycle. As data is clocked out onto the serial bus, more data is needed and therefore clocked out of the sensor and into the TSB15LV01. This method of processing reconciles the two asynchronous, periodic events. It also minimizes the size of the internal FIFO needed to buffer the data stream, since data is only taken from the CCD as it is needed.

The data is packetized on the bus such that there is a period of time between frames in which no data remains to be clocked out of the sensor, and no data is being transferred on the serial bus. During such periods of inactivity, the TSB15LV01 may clock pixels out of the serial register while ignoring the resulting processed data from the AFE. This results in lines of blank dummy pixels being clocked out of the CCD at regular intervals. This action is taken because extended idle periods can allow the CCD serial register to accumulate dark current. Clocking these pixels also keeps a constant dc level at the AFE ac-coupling capacitor.

Figures 2-4 through 2-12 show the sensor interface for each approved sensor. For each sensor, there are four views shown. The first view contains the timing for the acquisition and transfer of a full frame of video. The second view is a magnified portion of the start frame. The third view is a magnified portion of the start of a line, while the fourth view is a magnified portion of the horizontal drive pulses. In some cases, the pulses are identical for the different sensor options, so they are consolidated under a single figure. In all figures, the mode is YUV 4:1:1 640 x 480, at 30 frames per second, with minimum exposure time.

Note that these signals are intended to be processed by one of the recommended driver devices before reaching the CCD. In addition to level-shifting, these devices perform logic on the signals. Therefore, the signals at the sensor are different than the ones shown in Figures 2-4 through 2-12.

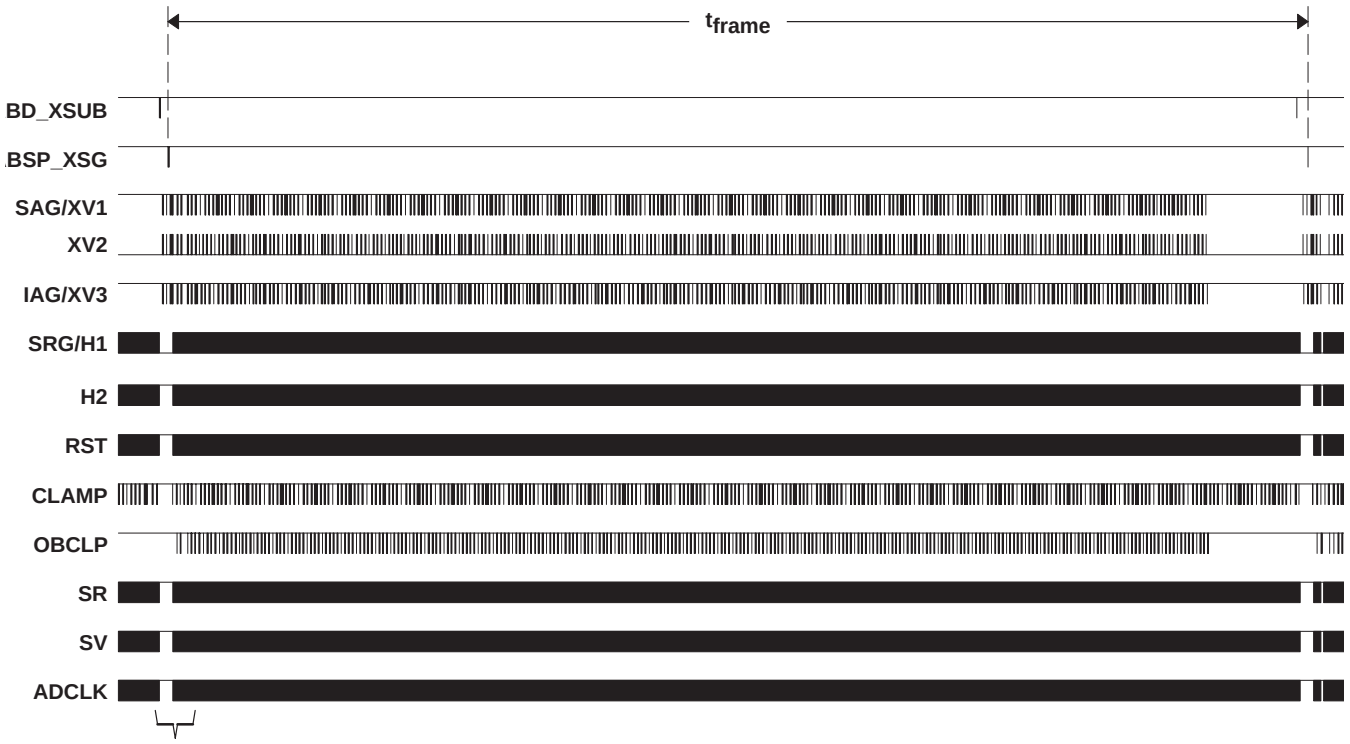


Figure 2–7

Figure 2–4. Sensor Interface Timing for ICX098/LZ24BP Sensor, Full Frame

Table 2–13. ICX098/LZ24BP Full Frame Timing Parameters

		MIN	TYP	MAX	UNIT
t_{frame}	Frame period (@ 30 frames per sec.)		33.3		ms

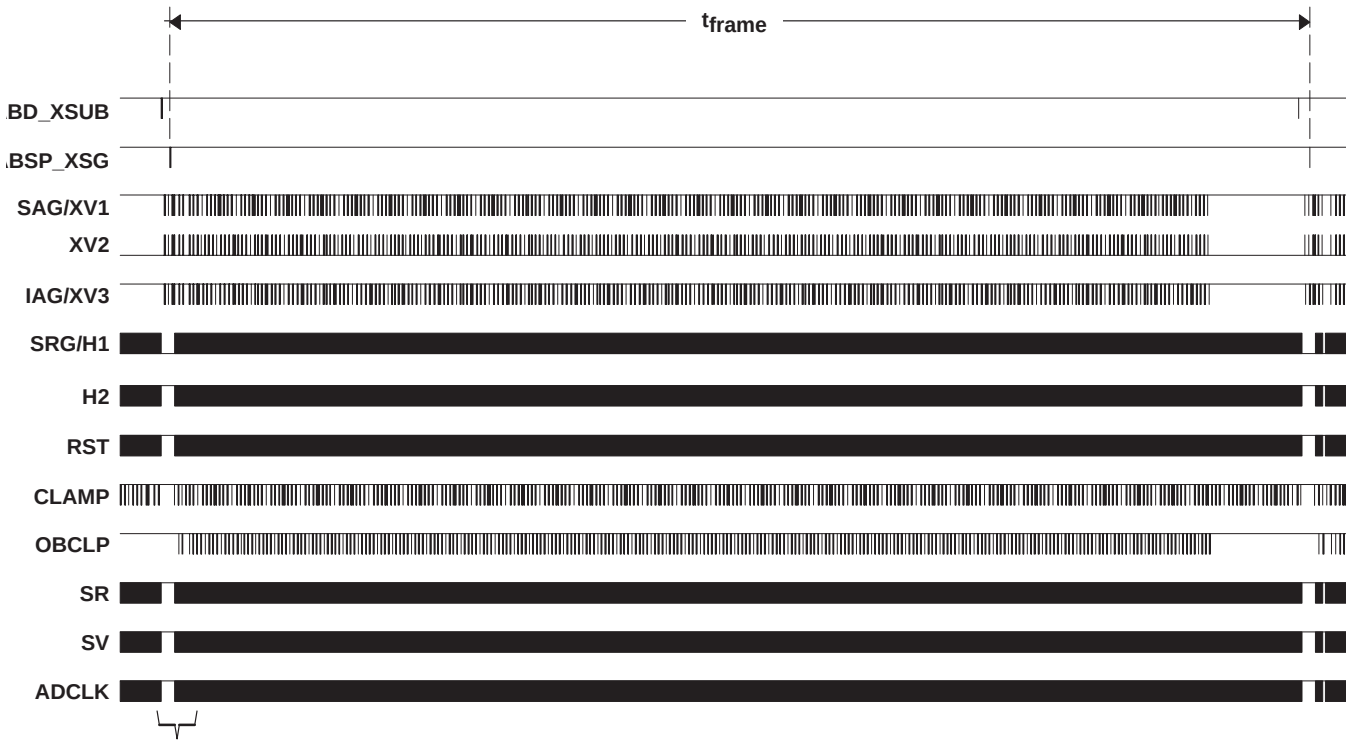


Figure 2–5. Sensor Interface Timing for ICX084 Sensor, Full Frame

Table 2–14. ICX084 Full Frame Timing Parameters

		MIN	TYP	MAX	UNIT
t_{frame}	Frame period (@ 30 frames per second)		33.3		ms

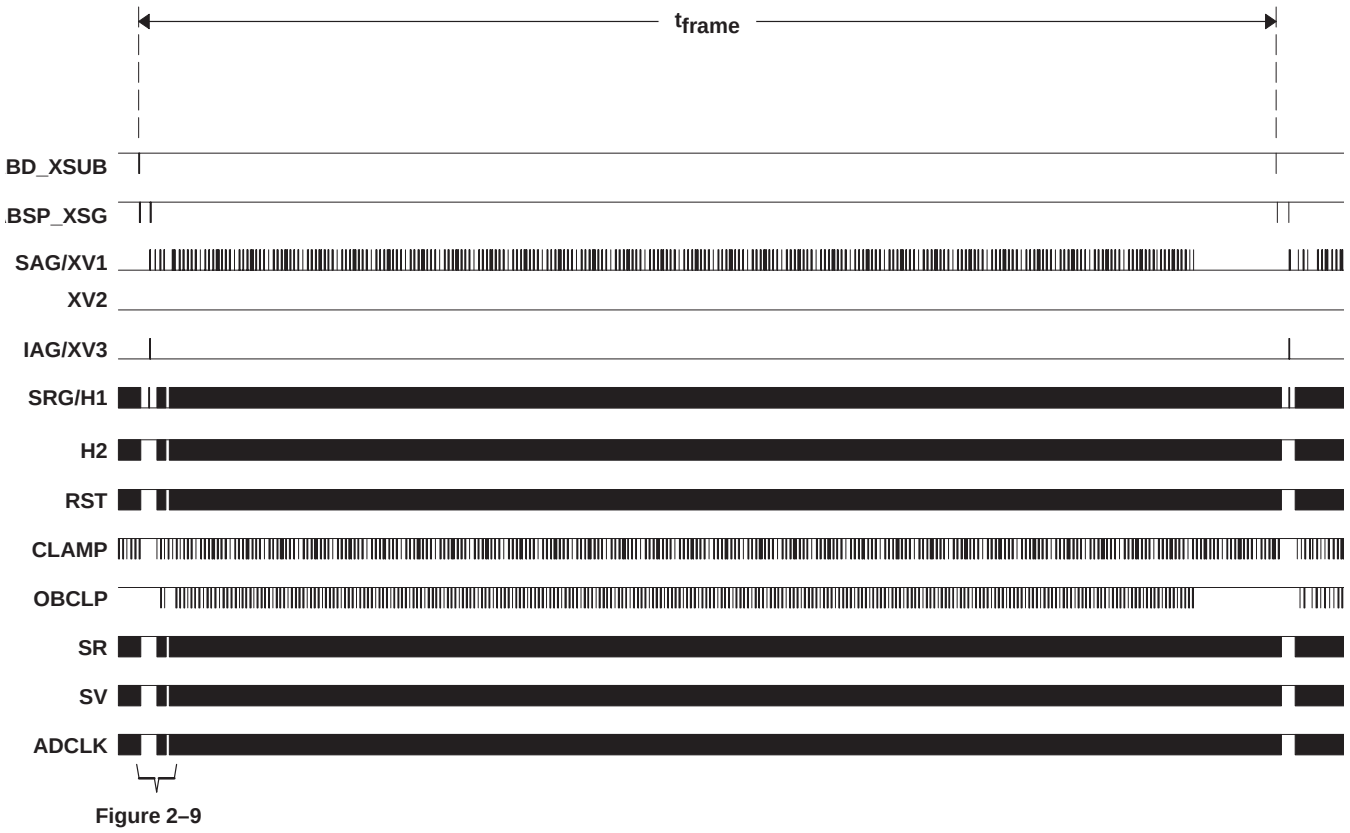


Figure 2–6. Sensor Interface Timing for TC237 Sensor, Full Frame

Table 2–15. TC237 Full Frame Timing Parameters

		MIN	TYP	MAX	UNIT
t_{frame}	Frame period (@ 30 frames per second)		33.3		ms

Figures 2-7 through 2-9 depict the start of a frame. Each block of pulses on the horizontal drive signals following the pulse on ABSP_XSG represents a line of video data. The gap between the fourth and fifth lines is the waiting period for the next 1394 isochronous cycle. Because the integration cycle is asynchronous with the 1394 isochronous cycle, this gap continually changes in length.

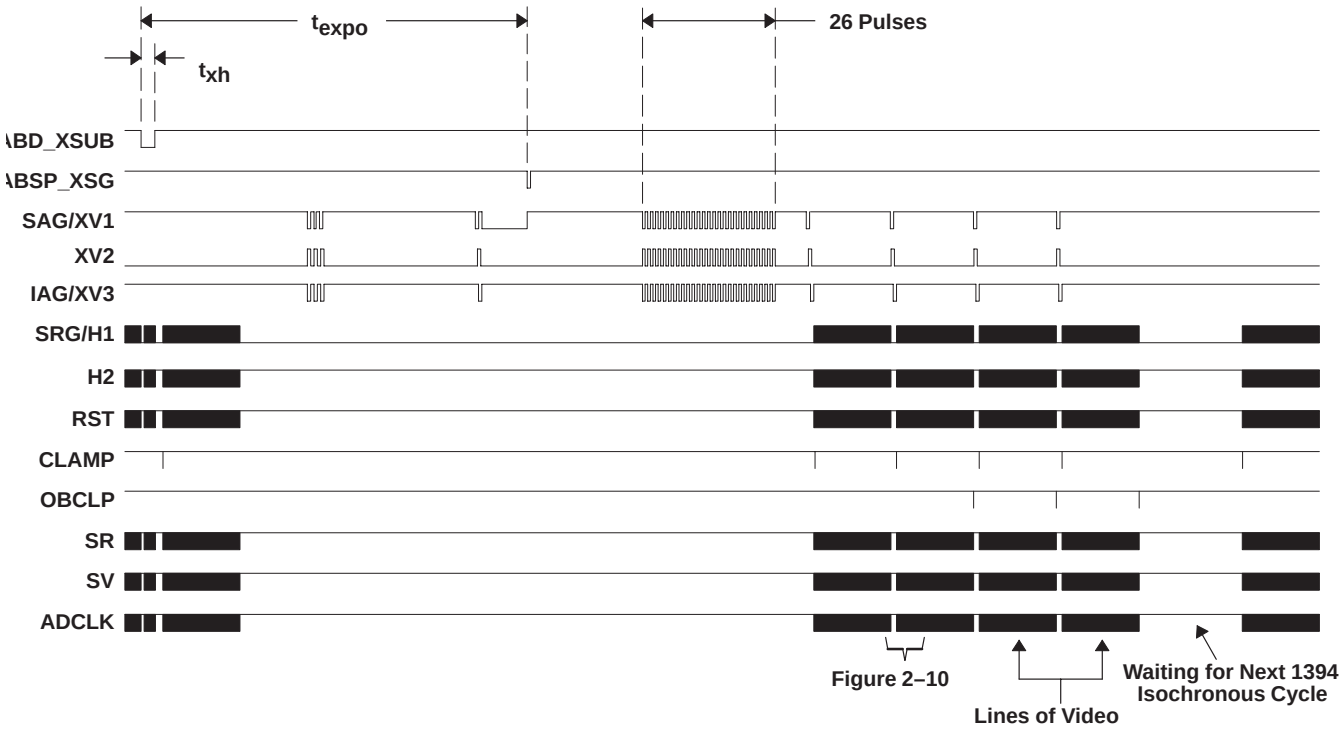


Figure 2–7. Sensor Interface Timing for ICX098/LZ24BP Sensor, Start of Frame Data

Table 2–16. ICX098/LZ24BP Frame Start Timing Parameters

		MIN	TYP	MAX	UNIT
t_{xh}	ABD_XSUB hold		11		µs
t_{expo}	Exposure time	292			µs

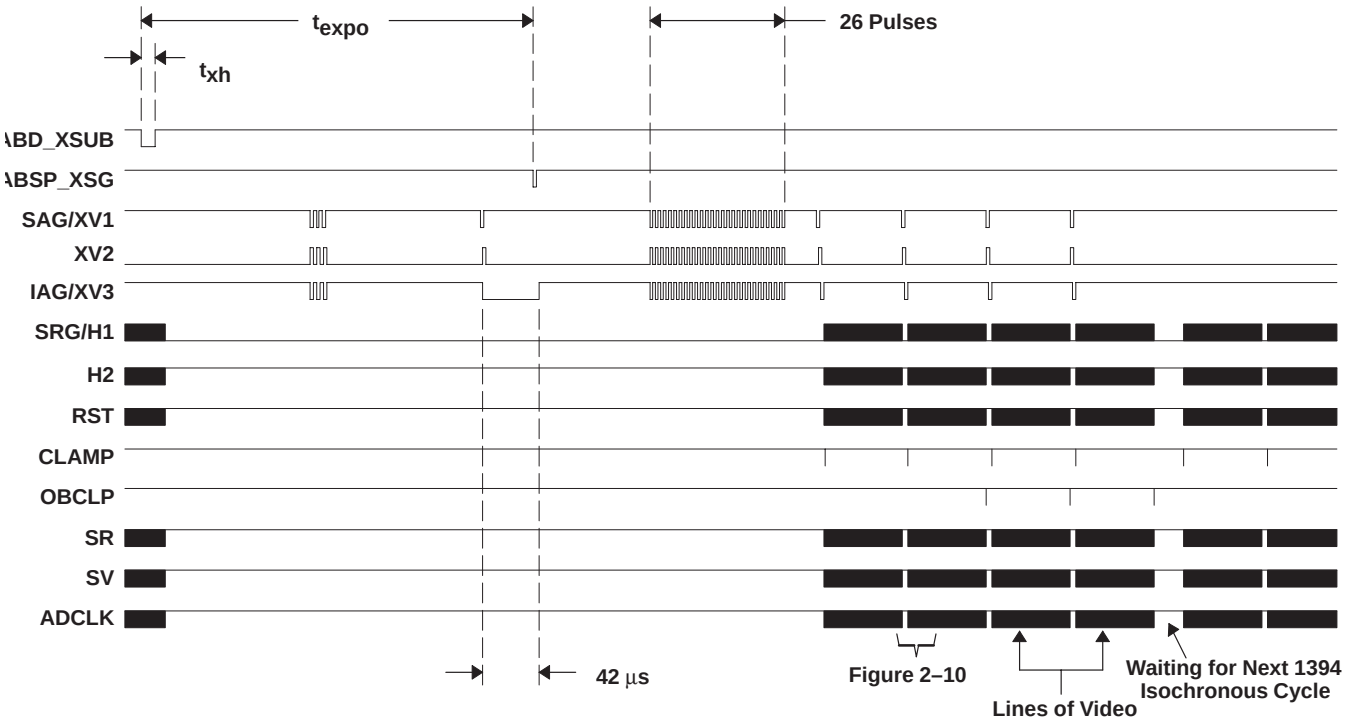


Figure 2–8. Sensor Interface Timing for ICX084 Sensor, Start of Frame

Table 2–17. ICX084 Frame Start Timing Parameters

		MIN	TYP	MAX	UNIT
t_{xh}	ABD_XSUB hold		11		µs
t_{expo}	Exposure time	292			µs

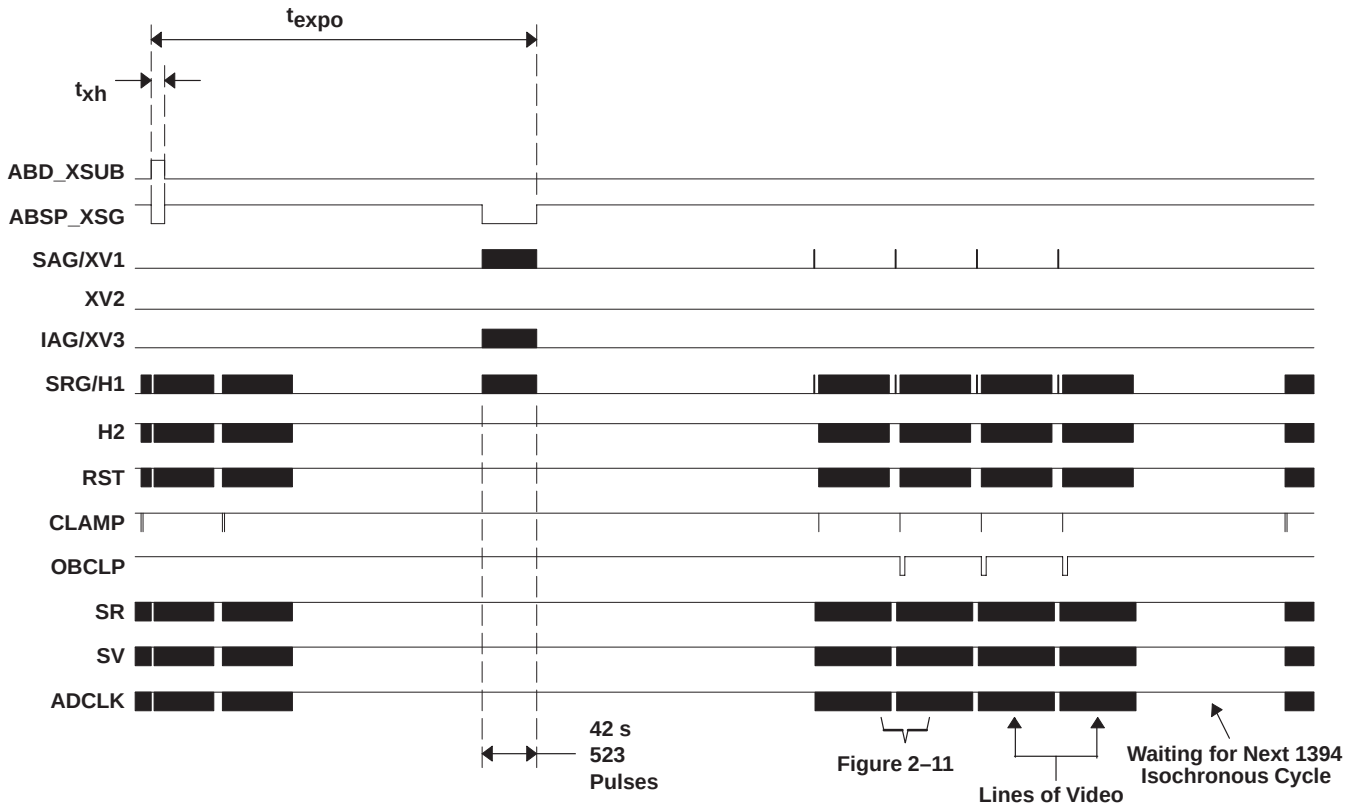


Figure 2–9. Sensor Interface Timing for TC237 Sensor, Start of Frame

Table 2–18. TC237 Frame Start Timing Parameters

		MIN	TYP	MAX	UNIT
t_{xh}	ABD_XSUB/ABSP_XSG hold		11		µs
t_{expo}	Exposure time	294			µs
t_{ptd}	Parallel transfer duration		42		µs

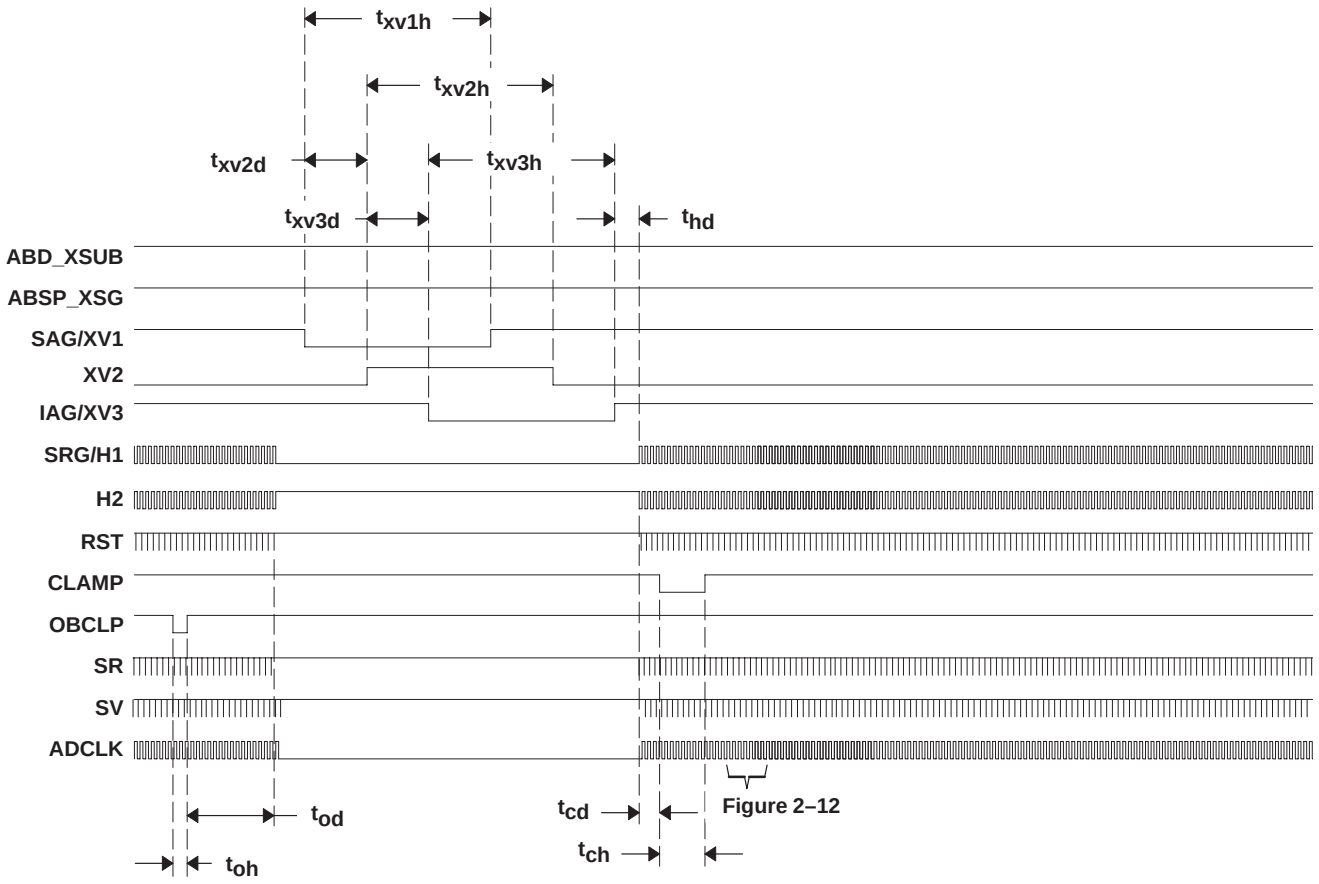


Figure 2–10. Sensor Interface Timing for ICX098/LZ24BP/ICX084 Sensor, Start of Line

Table 2–19. ICX098/LZ24BP/ICX084 Line Start Timing Parameters

		MIN	TYP	MAX	UNIT
t_{xv1h}	SAG/XV1 hold time		2.7		µs
t_{xv2h}	XV2 hold time		2.7		µs
t_{xv3h}	IAG/XV3 hold time		2.7		µs
t_{xv2d}	XV2 delay time		900		ns
t_{xv3d}	IAG/XV3 delay time		900		ns
t_{hd}	Horizontal drive delay following line transfer		350		ns
t_{cd}	CLAMP delay following start of horizontal drive		280		ns
t_{ch}	CLAMP hold time		652		ns
t_{od}	Time between OBCLP and end of line		1.3		µs
t_{oh}	OBCLP hold time		160		ns

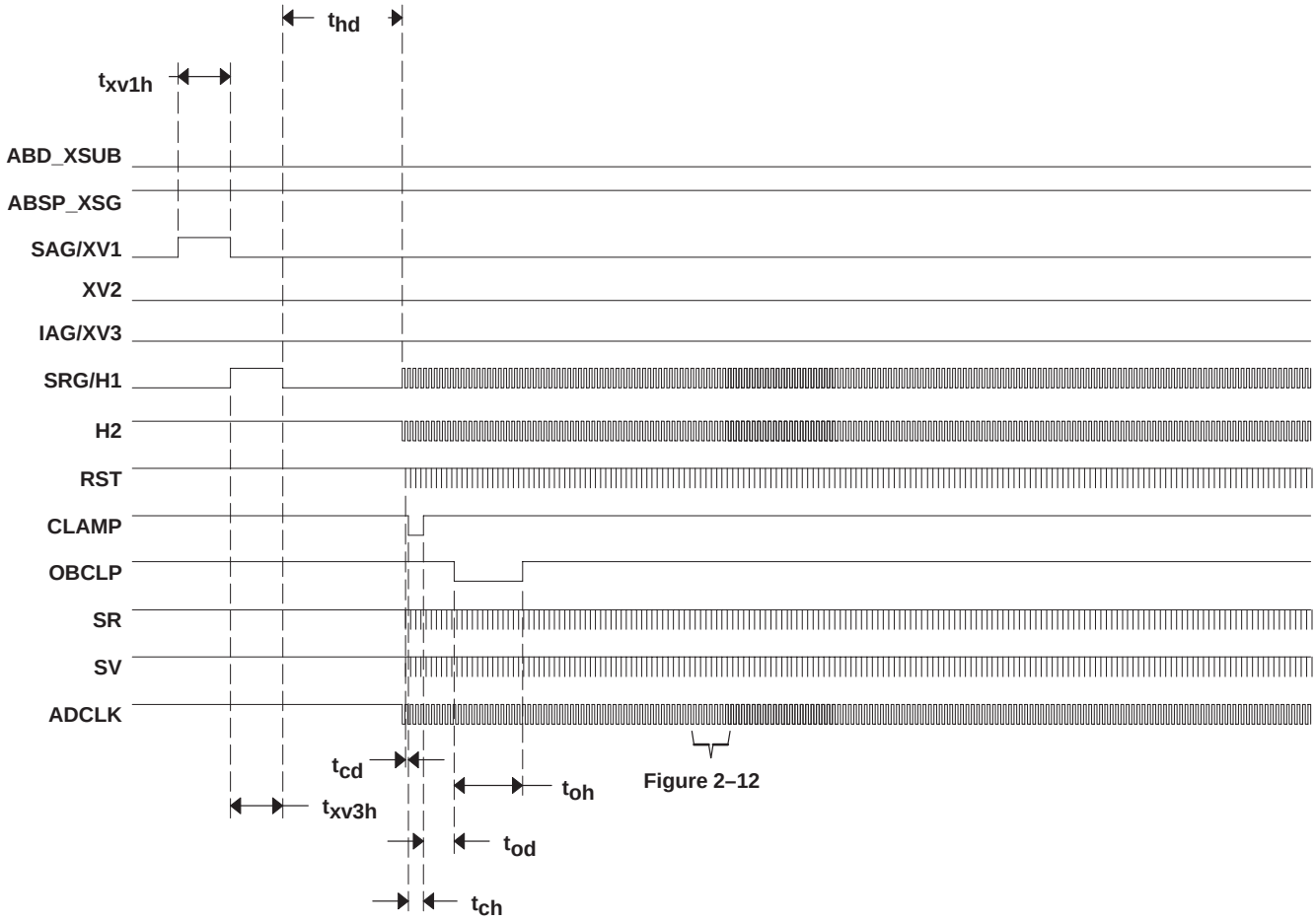


Figure 2–11. Sensor Interface Timing for TC237 Sensor, Start of Line

Table 2–20. TC237 Line Start Timing Parameters

		MIN	TYP	MAX	UNIT
t_{xv1h}	SAG/XV1 hold time		820		ns
t_{xv3h}	IAG/XV3 hold time		810		ns
t_{hd}	Horizontal drive delay following line transfer		1.8		µs
t_{cd}	CLAMP delay following start of horizontal drive		40		ns
t_{ch}	CLAMP hold time		244		ns
t_{od}	Time between clamp and OBCLP		488		ns
t_{oh}	OBCLP hold time		1.056		µs

Figure 2–12 depicts the horizontal drive pulses. Note that this diagram reflects the timing when all fields in the *CCD_PULSE_CNFG* and *CCD_PULSE_CNFG* registers are set to 00. This is the nominal position. Table 2–21 shows the horizontal drive timing parameters.

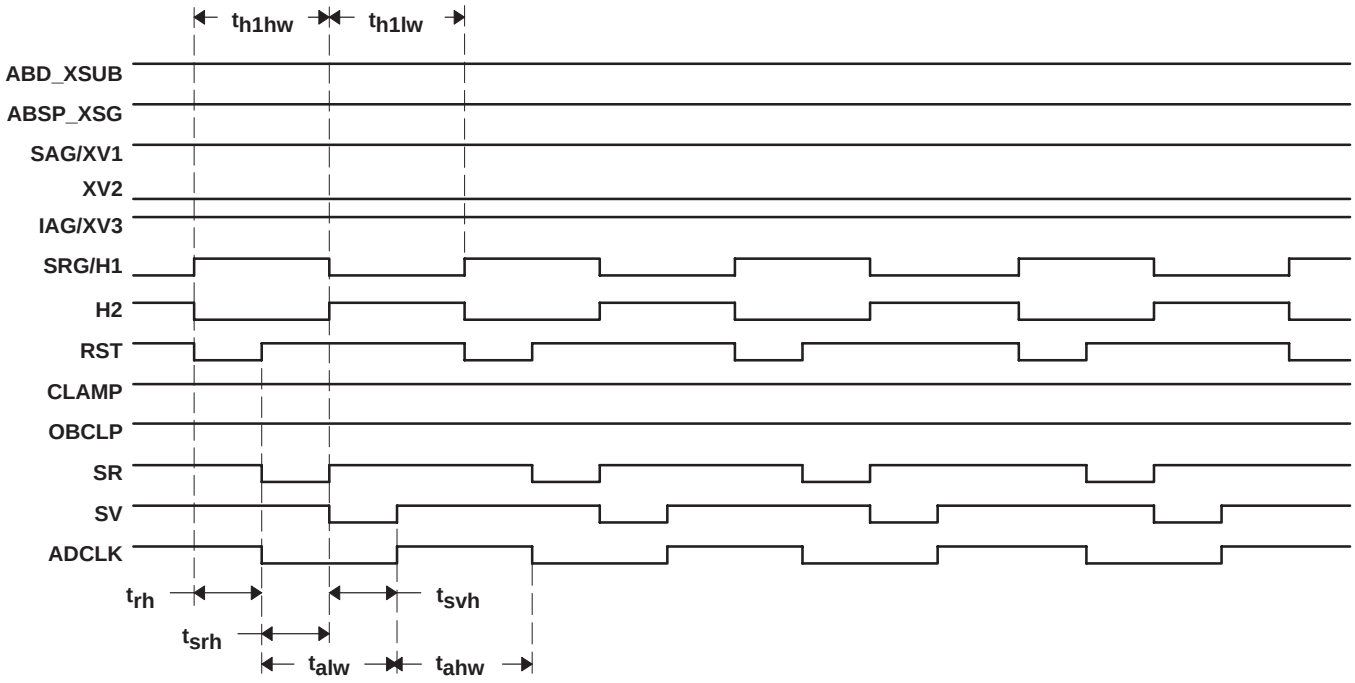


Figure 2–12. Sensor Interface Timing for All Sensors, Horizontal Drive

Table 2–21. Horizontal Drive Timing Parameters

		MIN	TYP	MAX	UNIT
t_{h1hw}	SRG/H1 high width		40		ns
t_{h1lw}	SRG/H1 low width		40		ns
t_{rh}	RST hold time		20		ns
t_{srh}	SR hold time		20		ns
t_{svh}	SV hold time		20		ns
t_{ahw}	ADCLK high width		40		ns
t_{alw}	ADCLK low width		40		ns

2.2.3.2 Pulse Tuning

Maintaining maximum dynamic range of the CCD image requires that the AFE's CDS clamp and sample pulses correspond perfectly to the analog output of the CCD, and thus to the CCD clock pulses as well. This means that after a camera has been built, the CCD/AFE drive pulses need to be tuned into their proper positions.

Signals that need to be adjusted include RST, H2, SRG/H1, SR, SV, and ADCLK. For each of these signals, a field exists in the *CCD_PULSE_CNFG* and *CDS_PULSE_CNFG* registers. These 6-bit fields contain values that represent the amount of delay relative to the nominal position. Each field has a maximum value of 3 F, which corresponds to approximately 16 to 18 ns.

2.3 STAT Interface

Three status terminals are provided: STAT0, STAT1, and STAT2. These terminals can be configured to provide different functions. The function of a STATn terminal is changed by writing a new signal code into the corresponding field of the *STATUS_CNFG* register.

When one or more of the terminals is configured as a signal input, the host can read the input value by reading the *st_stat* field of the *STATUS_CNFG* register. Similarly, when one or more of the terminals is configured as a signal output, the host can change its value by writing to the *st_stat* field.

The functions provided by the STAT interface are shown in Table 2–22.

Table 2–22. Status Terminal Functions Determined by STATn Register Fields

SIGNAL CODE	I/O	SIGNAL
		STAT0
0	I	Signal input. Configures this terminal as an input that can be read from the host via the 1394 serial bus. The input value can be found in bit 0 of the *st_stat* field of the *STATUS_CNFG* register.
1	O	Signal output. Configures this terminal such that it outputs the value of bit 0 in the *st_stat* field of the *STATUS_CNFG* register, which can be written to by the host.
2	O	Cycle_out. This is the link's cycle clock. It is based on the timer controls and the cycle-start messages received from the 1394 bus cyclemaster.
3	O	ITF_Empty. This signal is high when the ITF (isochronous transfer FIFO) is empty.
4	O	Line sync pulse. Pulses at the start of every horizontal line
5	O	Clamping pulse
6	O	Active region pulse. Vertical sync signal that pulses once per image frame.
7	O	Focus motor select. Writing this value to the *STAT0* register tells the TSB15LV01 that a motor is present that will derive its control from the *FOCUS_CNTL* register.
		STAT1
0	I	Signal input. Configures this terminal as an input that can be read from the host via the 1394 serial bus. The input value can be found in bit 1 of the *st_stat* field of the *STATUS_CNFG* register.
1	O	Signal output. Configures this terminal such that it outputs the value of bit 1 in the *st_stat* field of the *STATUS_CNFG* Register, which can be written to by the host.
2	O	Cycle_start. Isochronous cycle start indicator. Signals the beginning of an isochronous cycle by pulsing for one clock period.
3	O	Cycle_Done. When high, an arbitration gap has been detected on the 1394 bus after the reception of a cycle-start packet. This indicates that the isochronous cycle is over.
4	O	Line sync pulse. Pulses at the start of every horizontal line.
5	O	Iso_Enable. Indicates that isochronous 1394 packet transmission has been activated.
6	O	Active region pulse. Vertical sync signal that pulses once per image frame.
7	O	Zoom motor select. Writing this value to the *STAT1* register tells the TSB15LV01 that a motor is present that will derive its control from the *ZOOM_CNTL* register.
		STAT2
0	I	Signal input. Configures this terminal as an input that can be read from the host via the 1394 serial bus. The input value can be found in bit 2 of the *st_stat* field of the *STATUS_CNFG* register.
1	O	Signal output. Configures this terminal such that it outputs the value of bit 2 in the *st_stat* field of the *STATUS_CNFG* register, which can be written to by the host.
2	O	Dm_Rdy. Indicates that a 1394 isochronous stream is ready to be sent on the next iso cycle.
3	O	While high, indicates that a valid video line is being clocked out of the CCD. If low, indicates that dummy lines are being clocked out.
4	O	Line sync pulse. Pulses at the start of every horizontal line
5	O	6-MHz clock
6	O	Active region pulse. Vertical sync signal that pulses once per image frame
7	O	Iris motor select. Writing this value to the *STAT2* register tells the TSB15LV01 that a motor is present that will derive its control from the *IRIS_CNTL* register.

2.4 Motor Control Interface

The TSB15LV01 provides control for three stepper motors that can be used for focus, zoom, and iris functions. Steppers provide exact, high-tolerance control.

Note also that while the interface provides for focus, zoom, and iris motors, any motor with a similar function can be attached to those interfaces, such as pan or tilt.

2.4.1 Motor Driver Timing

Only one set of drivers is provided, and control of the motors is multiplexed. The STAT0, STAT1, and STAT2 terminals, when configured for stepper motors as discussed in section 2.3 STAT Interface, select which motor is being controlled. When a STATn terminal goes low, all motor terminal signals (PHASEx_n, IR_SIG, MOTOR_PLUS/MINUS) are intended for the motor corresponding to the STATn terminal in question.

If only one STATn terminal is configured as a motor select, that terminal is held low continually, while the others perform the function for which they were programmed. If more than one STATn terminal is configured as a motor select, their outputs alternately pulse low. For example, if two motors are being used, each STATn terminal is active half the time. If three motors are being used, each STATn terminal is active one third the time. This is shown in Figure 2–13.

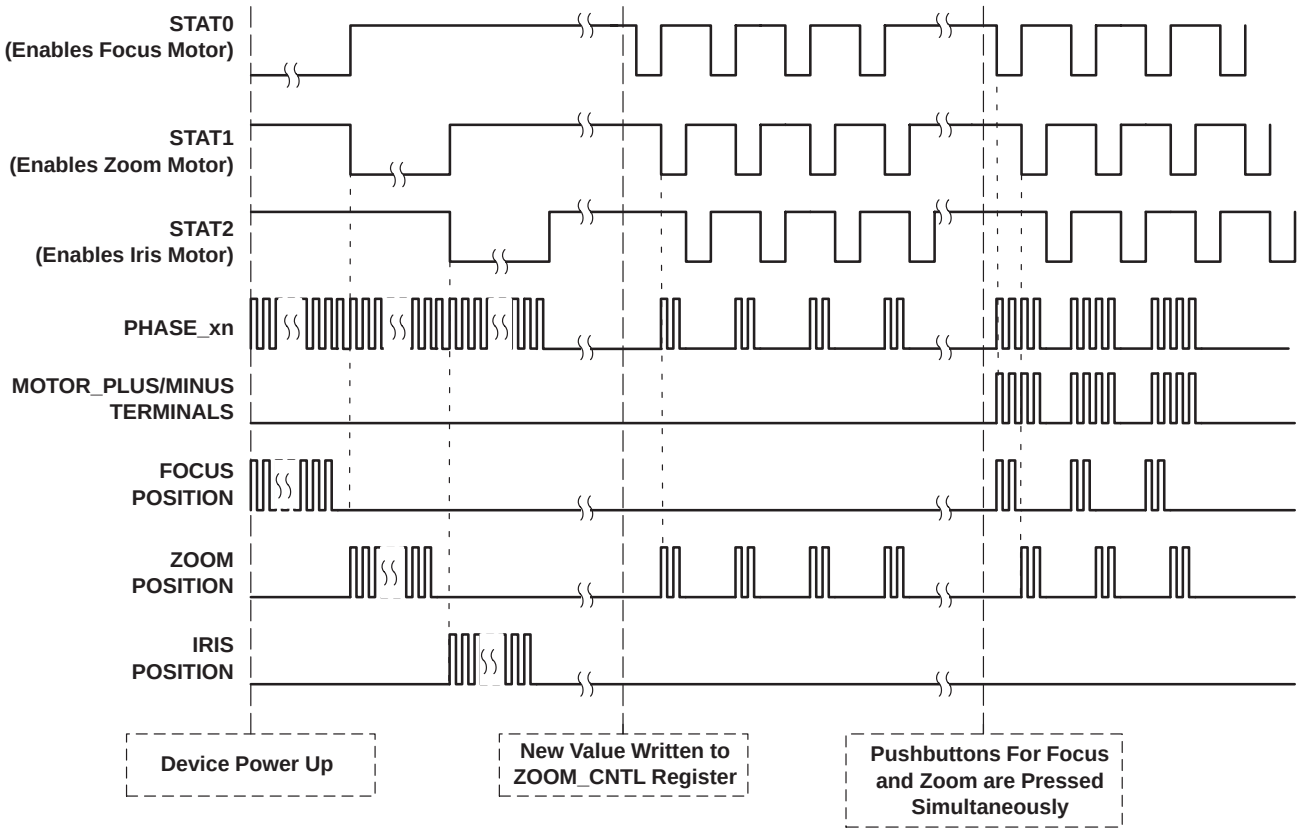


Figure 2–13. STATn Motor Select Pulses

In Figure 2-13, each pulse in the last three lines does not indicate a signal pulse, but rather a movement in the position of the motors. Also, the pulses for *phase_xn* are not literal. The pulses actually driven are as defined by the stepper drive table used by the TSB15LV01, shown in Table 2–23.

Table 2–23. Stepper Drive Table

	MOTOR DRIVE TERMINAL			
	PHASE1_A	PHASE1_B	PHASE2_A	PHASE2_B
STEP 1	1	0	1	0
STEP 2	0	1	1	0
STEP 3	0	1	0	1
STEP 4	1	0	0	1

The table shows values for the forward direction. The values are driven in a cyclical pattern when the motor is to be driven forward. The values are driven cyclically in reverse when the motor is to be moved backwards.

The default state for the drive terminals is high, resulting in the outgoing value of 1111. It is intended that the outputs will be used as inputs to an inverting drive circuit; therefore, the default state of the stepper drive windings is that both ends are grounded. As a result, the motor and driver assembly only draw current when actively stepping in one direction or another.

Note that only one STATn terminal is needed per motor, such that if less than three motors are being used, the remaining STATn terminals can be used for other functions.

2.4.2 Positioning System

Positioning for the steppers is based on a linear scale from 000h to 3FFh (10 bit). Upon power up of the device, it seeks to align the physical motor position with the initial starting value stored in the corresponding field of the *MOTOR_POS_CNFG* register (*ir_zoom, ir_focus*, or *ir_iris* fields). To do this, the device first moves the stepper to a physical reference point indicated by the IR_SIG terminal. IR_SIG is assumed to have a position feedback signal attached to it, such as an infrared sensor. This point is likely near the beginning or end of the mechanism's motion.

If the IR_SIG terminal is high when the device powers up, it indicates that the mechanism is in a position beyond the position reference. The TSB15LV01 steps the mechanism down until the terminal goes low. If the terminal is already low at power up, the motor steps the mechanism up until the terminal goes high, and then steps it back one.

After each motor has been positioned at its reference, the TSB15LV01 associates those positions with the values in the corresponding fields of the MOTOR_POS_CNFG register. Using these values as starting points, it moves each motor to the position indicated in the *value* field of the feature control register corresponding to that motor (ZOOM_CNTL, FOCUS_CNTL, or IRIS_CNTL). For example, a camera can be preset to focus at a certain distance. After the TSB15LV01 has realigned the motor at the beginning or end of the focus mechanism movement, it moves the motor to the predetermined focus setting.

Subsequently, any value written to the feature control registers that is not equal to the current position will cause the motor to step toward that value. Each incremental value written to the register represents one step the motor moves. When the motor position matches the value in the feature control register, the stepper shuts off, and the windings are grounded. Power up and movement of the motor can be seen in Figure 2–13.

Initial positioning of the motors following power up occurs in sequential order, with the first motor pulling itself into position, then the second motor, and then the third. After this, all motor step sequences are multiplexed, which effectively causes the motors to move simultaneously.

2.4.3 Pushbutton Interface

The MOTOR_PLUS and MOTOR_MINUS terminals are designed as pushbutton inputs. Driving one of these terminals high causes the *value* field of the current motor's feature control register to increment or decrement accordingly. In response, the corresponding motor moves forward or backward. Holding one of these inputs high will cause the motor to step continuously.

The motor to which activity on MOTOR_PLUS/MINUS is applied is determined by which motor select (STATn terminal) is currently low. If only one motor is used, only one motor select is present, allowing pushbuttons to be attached directly to the terminals.

If more than one motor is being used, it is necessary to multiplex them. As a result of the alternating STATn pulses, the switches are scanned on a periodic basis. There is no need for a debounce circuit, because the buttons are scanned at a fixed rate of approximately 30 Hz.

2.5 EEPROM Interface

An external EEPROM with serial port interface (SPI) interface is required for TSB15LV01 operation. The entire address space of the TSB15LV01 accessible from the 1394 bus is stored there. The EEPROM must provide 4096 bits of memory, such as a 512×8 configuration. The interface is designed to be used with the Atmel AT25040 or Xicor X25040. It utilizes a four-wire interface consisting of a chip select, an input, an output, and a clock.

The 1394 bus uses 48-bit addresses. Since this is too large of a contiguous address space for most conventional EEPROMs, the TSB15LV01 converts these addresses into an 8-bit form called the *internal address*. The conversion is shown in section 3, Address Space.

All registers are stored in the external EEPROM device. However, upon power up of the TSB15LV01, the feature control registers and the configuration registers are copied from the EEPROM into registers resident in the TSB15LV01 device. This includes all address space between F0F00800h and F0F00F24h. From that moment on, 1394 bus accesses to this address space apply to the registers in the TSB15LV01. For address space outside this range, bus accesses are executed on the EEPROM device. As a result, the role of the EEPROM with respect to these registers is to store default values, these values are saved when power is removed from the device. The values in the TSB15LV01 registers are never written back to the EEPROM by the TSB15LV01 device, and the bus is not capable of changing them since all normal run-time bus accesses to this memory space operate on the TSB15LV01. This allows for the loading of power up initialization values into the EEPROM.

However, it is possible to write values to the EEPROM for any address location once a value of 12345678h has been written to the *write_protect_control* field of the *EEPROM_CNFG* register. This value is known as the *write-protect control code*. Once this control code has been written to the device, all register space accesses will operate upon the EEPROM. *Writes* operate on both the EEPROM and the TSB15LV01. *Reads* operate on the EEPROM only. This mechanism provides a way to program new initialization values.

Figures 2–14 and 2–15 show the read and write timing (Table 2-24) associated with the TSB15LV01 EEPROM interface.

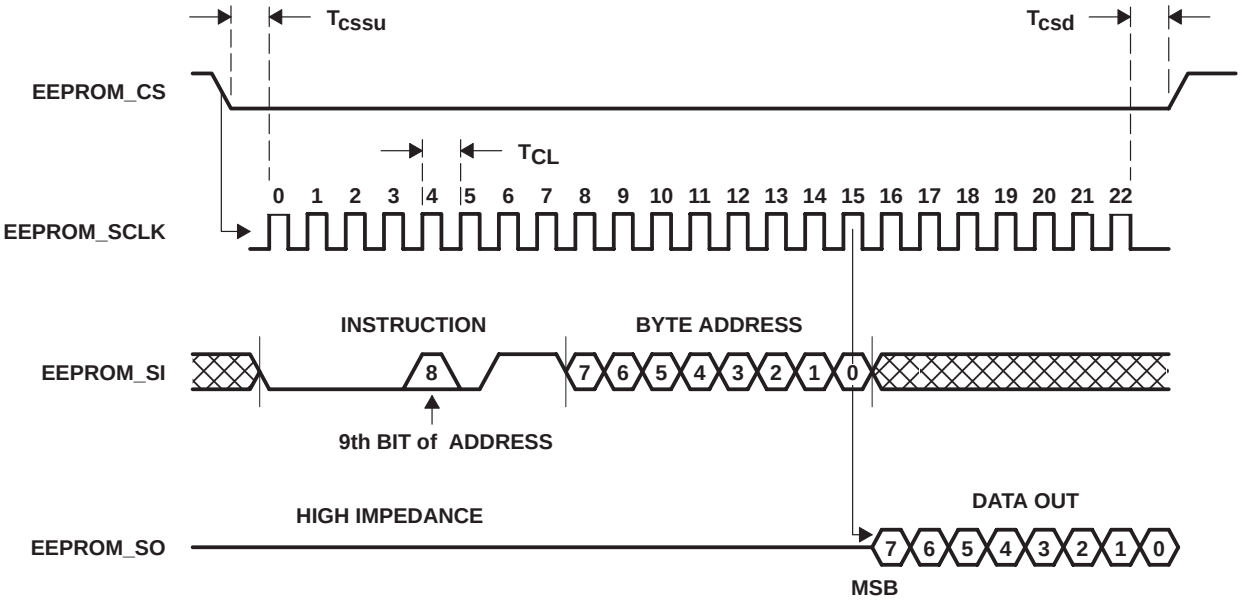


Figure 2–14. Read Timing

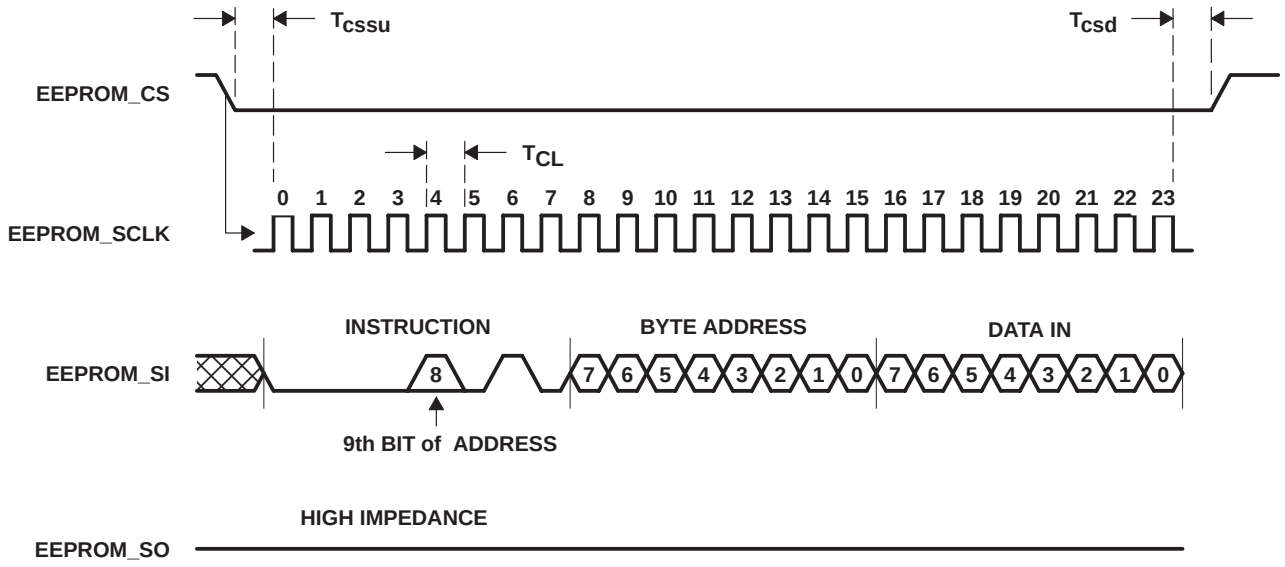


Figure 2–15. Write Timing

Table 2–24. EEPROM Interface Timing Parameters

		MIN	TYP	MAX	UNIT
t_{cssu}	EEPROM CS setup time		652		ns
t_{csd}	EEPROM CS delay time		652		ns
t_{cl}	Clock period		1.304		µs

2.6 Video Signal Processor

After the CCD image data is received from the AFE, it is processed by the video signal processor (VSP). The core of the VSP is a digital signal processor (DSP) that conducts numerous essential algorithms, discussed in the sections below.

Most of the video processing features present in the TSB15LV01 are included as part of the digital camera specification. As such, they are controllable via the feature control registers (see section 3.3.3.1.3, Feature Control Registers). A few others are specific to the TSB15LV01 and can be controlled with the TSB15LV01 configuration registers.

2.6.1 De-Mosaicing

The CCD image data is comprised of individual component pixels, each of which is pure red, green, or blue. The VSP *de-mosaics* them, a process in which they are grouped to form composite pixels that fit the RGB standard.

Several adjustments can be made in the configuration registers that affect how the sensor data is compiled into the RGB image frame. These are shown in Table 2–25.

Table 2–25. CCD Sensor Processing Adjustments

ADJUSTMENT	COMMENT
H-Center and V-Center fields of CCD_OPTICS_CNFG register	The TSB15LV01 receives an image size greater than 640 x 480 pixels from the CCD. These fields determine which 640 x 480 rectangle is processed and transmitted to the host.
pix_shp fields of VIDEO_OPTIONS_CNFG register	Determines whether component pixels are grouped as squares or as L-shaped pieces. L-shaped pixels give a higher resolution image than square pixels but can create a jagged edge effect.

Additional information for each of these adjustments can be found in section 3.3.3.2, Configuration Registers.

2.6.2 Brightness

The brightness of the image is directly related to the DC offset of the image data in the AFE. This feature can be controlled automatically or manually.

When brightness is configured for automatic control via the *BRIGHTNESS_CNTL* register, the TSB15LV01 utilizes the TLV990's black clamping feature. This feature sets the offset at the beginning of every image frame, adjusting it so that the black pedestal is equal to the value stored in the *offset_level* field of the *DAC_OFFSET_CNFG* register. (See section 2.2.2.3, Black Clamping Interface, for more information.)

Brightness can also be controlled by setting the offset manually. If the TSB15LV01's auto-brightness feature is disabled, it divides the *value* field of the *BRIGHTNESS_CNTL* register into coarse (most significant eight bits) and fine (least significant eight bits) and sends those values directly to the AFE.

If autobrightness is used, there are two parameters sent to TLV990 that affect how black clamping is performed. Both are found in the *AFE_SETUP_CNFG* register. The first, found in the *lines_smpl* field, informs the TLV990 how many lines per image should be included in the black clamp averaging. The second, found in the *pix_smpl* field, informs the TLV990 how many samples per line should be included in the averaging. The TLV990 datasheet can provide more information on the use of these values.

2.6.3 Gain and Exposure

Gain refers to the gain stage of the AFE, while exposure refers to the CCD image integration time. These parameters can be configured manually using their corresponding feature control registers, *GAIN_CNTL* and *EXPOSURE_CNTL* (Figure 2-16).

Alternatively, they can be controlled automatically using an internal feedback loop. This loop samples 4048 pixels within an image and calculates the average pixel luminance. It compares this value with the value stored in the *auto-expo* field of the *AUTO_ADJ_CNFG* register, adjusting the gain and exposure time accordingly.

A control input to this block, stored in the *expo_delta* field of the *AUTO_ADJ_CNFG* register, regulates the speed at which adjustments are made to the algorithmic filter. This value must be adjusted to provide adequate damping for the feedback loop.

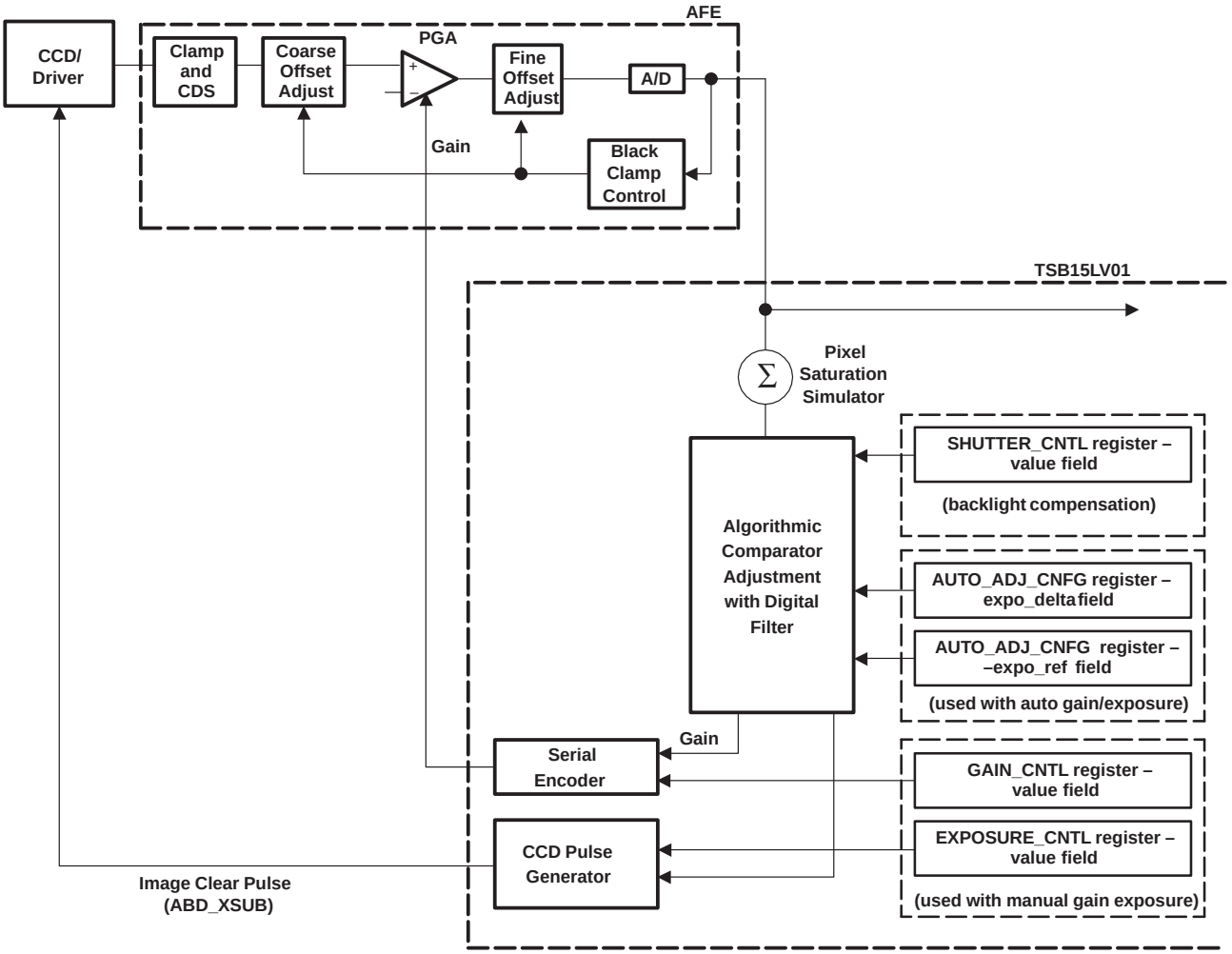


Figure 2–16. Gain and Exposure Automatic and Manual Controls

The location of the sampled pixels is dictated by the backlight compensation feature, described in section 2.6.9.

Gain and exposure have a similar effect on the image. In other words, the effect of a reduction in gain can be countered by a proportional increase in exposure, and vice versa. Therefore, there are many combinations of gain and exposure settings that produce a similar image.

High gain settings can amplify any noise that may have been introduced to the analog signal, prior to or during its conversion to digital. Because of this, the autogain/exposure loop generally seeks to keep gain as low as possible, adjusting the exposure parameter to properly expose the image. Gain is increased when the exposure parameter alone is not sufficient to produce a proper exposure.

2.6.4 Sharpness and Saturation

Processing on the sharpness and saturation parameters is performed by the VSP. They are adjustable within reasonable boundaries by altering values in their corresponding feature control registers.

The sharpness control utilizes a continuous extrapolation filter, providing smooth sharpness control. Saturation refers to color saturation, as opposed to saturation of a CCD charge.

2.6.5 White Balance

This feature alters the degree to which red and blue CCD component pixels are weighted to form composite pixels. Green is considered constant. White balance often needs to be adjusted when image lighting changes. For example, when white balance has been configured for incandescent lighting, it will need adjustment if taken to an area with fluorescent or natural lighting. This is because the spectral content of these light sources differs from incandescent light.

White balance can be adjusted manually or automatically, selectable in the *WHITE_BALANCE_CNTL* register. If the feature is set as manual, it corresponds directly with the value in that register. The host can then alter the white balance value as it wishes. For example, it could implement its own autobalance feature.

If the feature is set as automatic, an internal adjustment is used. This algorithm assumes that all incoming colors have a relatively equal amount of red, green, and blue, and makes small, iterative adjustments to the white balance. This provides very good white balance in most situations without necessitating manual adjustments. However, if red or blue is dominant in the image for a moderate period of time, the assumption is incorrect, and the image will begin to noticeably discolor.

2.6.6 Gamma

Gamma correction can be implemented to compensate for nonlinearities in cathode ray tubes, which in most cases is the device that is used to display the image. It is possible to turn this feature off, since some high-end CRTs are capable of providing their own gamma correction.

The gamma correction implemented by the TSB15LV01 incorporates a correction factor equivalent to the 0.45 analog gamma standard.

2.6.7 YUV Conversion

If the transfer mode is one that uses the YUV color space, the VSP converts the RGB pixels into YUV.

RGB to YUV color space conversion for gamma-corrected, fully-saturated RGB video is:

$$Y = 0.257\,R + 0.504\,G + 0.098\,B + 16$$

$$Cb = -0.148\,R - 0.291\,G + 0.439\,B + 128$$

$$Cr = 0.439\,R - 0.368\,G - 0.071\,B + 128$$

This matrix is approximated in the TSB15LV01, which processes video data as 8-bit digital values, by fractionalizing the coefficients with respect to 8 bits:

$$Y = (66/256)\,R + (129/256)\,G + (25/256)\,B + 16$$

$$Cb = -(38/256)\,R - (74/256)\,G + (112/256)\,B + 128$$

$$Cr = (112/256)\,R - (94/256)\,G - (18/256)\,B + 128$$

This approximation introduces less than one least significant bit of error.

2.6.8 Antiblooming

Blooming occurs when a CCD pixel becomes saturated and overflows into surrounding pixels. This can appear on the image display as discoloration or bright speckles. CCD sensors usually have a means of allowing a *cutoff* level to be set, above which charge is not allowed to exceed. Setting this antiblooming level just below the saturation level prevents charge overflow.

The Sony ICX084, Sony ICX098, and the Sharp LZ24BP perform this function internally. The TI TC237, however, requires the level to be set externally. To provide this voltage reference, one of the general-purpose DACs on the AFE can be utilized. The TSB15LV01 designates DAC1 as the antiblooming DAC. The DAC output can be used to set the TC237 antiblooming level.

The antiblooming feature must be activated by setting the *bloom_en* field of the *DAC_OFFSET_CNFG* register. Once this has been done, the value of the *blooming_value* field of the *DAC_OFFSET_CNFG* register will be sent to the TLV990. This will set the antiblooming voltage level for the CCD sensor. The value of the other general-purpose DAC, DAC2, can be set as well via the *DAC2_en* and *DAC2_value* fields of the same corresponding registers.

2.6.9 Backlight Compensation

The TSB15LV01 provides a way to compensate for situations in which a forefront object appears dark due to excessive light in the background. This is accomplished by extracting more gain/exposure samples from image regions in which the intended object resides (see 2.6.3, Gain and Exposure). Hot regions for which this feature can be activated include those shown in Table 2–26.

Table 2–26. Backlight Compensation Hot Regions

VALUES OF *SHUTTER_CNTL* REGISTER	HOT REGION
0	Matrix (No compensation). Pixel samples are evenly spaced.
1	Circle. All the pixel samples are taken from a circle in the center of the image. The region is 128 pixels wide.
2	Circle, averaged. Half the samples are taken inside the same circle as circle mode, half the samples are taken outside the circle.
3	Head and Shoulders. All the pixel samples are taken from a region that would be occupied by a person sitting in front of the camera.
4	Top third. All the pixel samples are taken from the top third of the image.
5	Bottom third. All the pixel samples are taken from the bottom third of the image.
6	Middle third. All the pixel samples are taken from the middle third of the image.

The hot region for backlight compensation is selected by the *SHUTTER_CNTL* register. As shown in Table 2–26, the feature can be disabled, causing the gain/exposure loop samples to be evenly distributed throughout the image.

2.6.10 White Spot Compensation

CCD sensors occasionally have nonuniformities that cause some pixels to build a charge significantly greater than the light that is activating them, due to leakage current in the pixel. In a black and white sensor, this causes white spots that appear out of place. In a color sensor, it can result in discoloration or speckles.

The TSB15LV01 can be configured to compensate for this error using one of two built-in filters. The first filter is a median filter. For every pixel, the median filter considers its value and the pixels on either side and replaces the original pixel with the median of the three. This removes any single-pixel abnormalities from the pixel stream. The other filter is the nonlinear interpolation filter. It compares a pixel to the ones before and after it. If it is significantly different, such that it exceeds a preset threshold, it is thrown out and replaced by the average of the two surrounding pixels. Alternatively, white spot compensation can be disabled.

The white spot compensation filter is chosen by the *filter* field of the *CCD_OPTICS_CNFG* register. The threshold for how deviant a pixel is allowed to be before it is discarded by the nonlinear interpolation filter is determined by the value of the *filter_limit* field, also in the *CCD_OPTICS_CNFG* register.

The tradeoff in using one of these filters lies in the fact that the filters are indiscriminate in discarding single-pixel abnormalities. Single-pixel abnormalities may be noise, or they may be a valid part of the image. As a result, the filters remove white spots but also result in some degradation of the image due to some loss of spacial high-frequency response. The median filter is more extreme in this regard. The nonlinear interpolation filter has an amplitude threshold that defines how extreme the abnormality must be before it is discarded, giving the user more control of the tradeoff.

The median filter is more effective in removing white spots, but if it has an adverse effect on the sharpness of the image, it may be desirable to use the nonlinear interpolation filter and adjust the filter limit, or disable the filter altogether.

2.6.11 Test Pattern

The TSB15LV01 can send a continuous image consisting of color bars and linear ramps. The test pattern is activated using the *test_en* field of the *TEST_CNFG* register. It is shown in Figure 2–17.

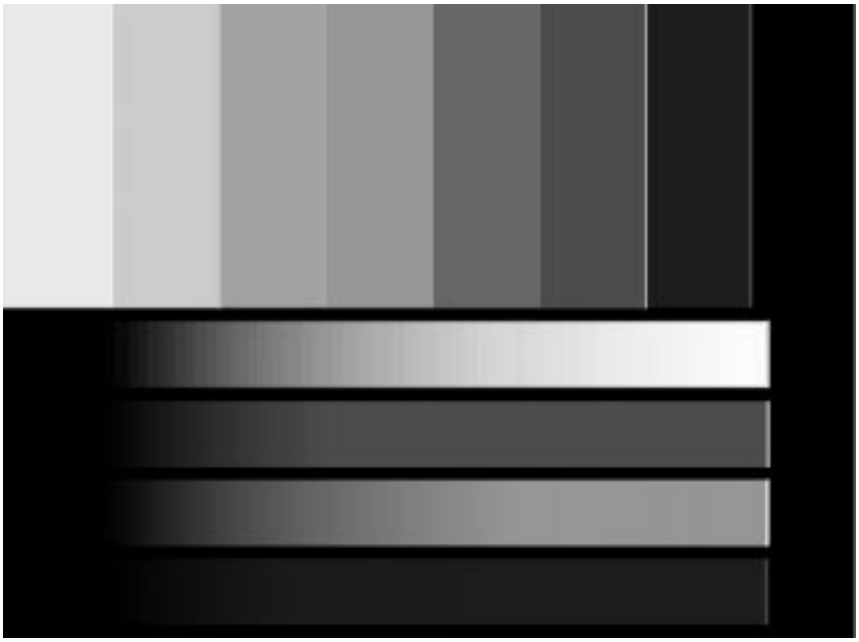


Figure 2–17. TSB15LV01 Built-In Test Pattern

The upper portion of the test pattern consists of solid vertical bars of white, yellow, cyan, green, magenta, red, blue, and black (in order, as shown in Figure 2–17). The bottom portion consists of horizontal bars of white, red, green, and blue, with luminance increasing from left to right. The luminance value increases by one every two pixels (RGB 640 x 480 mode).

The test pattern image is subject to changes in saturation, white balance, sharpness, and gamma control. It is not affected by changes in gain, brightness, exposure, or backlight compensation.

The test pattern is useful during camera development for determining whether image problems are originating *after* the VSP (1394 interface) or *before* it (sensor interface). That is, it can verify functionality between the host and the TSB15LV01 device, isolating image problems to the CCD or AFE interface.

3 Address Space

The address space for the TSB15LV01 is divided into four areas. The first consists of registers and ROM required for any 1394 node, called *1394 memory*. The second area consists of registers that reflect the level of capability of the digital camera, known as the *inquiry registers.* These registers are required by the Digital Camera Specification. Both 1394 memory and the inquiry registers are considered read-only. The third and fourth areas consist of registers that can be read for camera status or written to for camera control. These are called the *control registers* and *configuration registers.* The control registers are dictated by the Digital Camera Specification, while the configuration registers are unique to the TSB15LV01.

Table 3–1 gives a summary of the various register groupings referred to throughout this document.

Table 3–1. TSB15LV01 Register Groupings

REGISTER GROUP NAME	DESCRIPTION	REQUIRED BY	DOCUMENTATION
1394 registers	Registers required for 1394 nodes.	1394 Standard	Section 3.3.1
Inquiry registers	Registers that describe the capability of the digital camera, allowing host to determine availability of features provided for by the Digital Camera Specification.	Digital Camera Specification	Section 3.3.2
Control registers	Registers that control basic camera features, such as frame rate, output format, and video parameters.	Digital Camera Specification	Section 3.3.3.1
Configuration registers	Registers that control unique TSB15LV01 features and functions.	TSB15LV01-specific	Section 3.3.3.2

The TSB15LV01 provides a memory map consistent with v1.04 of the 1394 Digital Camera Specification, and implements most of the features provided for by that document. There are a few features that are not implemented.

This functionality should always be indicated in the inquiry registers. Recommended values are provided in Section 3.3.2. The inquiry registers themselves are always valid, since their function is to tell the host which features are valid and which are not, and since they are read-only by definition. The only registers that are disabled for nonsupported features are control registers.

3.1 1394 Node Memory Architecture

To understand the memory allocation of the TSB15LV01, it is useful to first understand the addressing structure for 1394 nodes in general. 1394 addresses consist of the components shown in Table 3–2.

Table 3–2. 1394 Address Components

COMPONENT	LENGTH	COMMENT
Bus ID	10 bits	Identifies the 1394 bus
Node ID	6 bits	Identifies the node within the bus
Destination offset	48 bits	Identifies the address within the node

The values of the first two components are environment-dependent. Note that address values shown throughout section 3 consist only of the 48-bit destination offset. In the case of the TSB15LV01, locations in “1394 memory” have a base destination offset of FFFF F000 0000h. In contrast, the inquiry, control, and configuration registers have a base destination offset of FFFF F0F0 0000h. Various registers are determined by adding an additional offset value to the destination offset.

The memory space of a typical 1394 node consists of a small collection of registers that exist at fixed addresses, called *initial register space,* and a number of dynamic memory structures called *directories* and *leaves*. Directories contain information and pointers to more directories and leaves. Leaves are blocks of memory that contain information but do not point to other directories or leaves.

These elements form a tree structure. A certain amount of freedom is granted to the developer of the 1394 node, allowing a variety of structures within the architecture guidelines. The root node for this structure exists in part of the initial register space, called the *root directory*. The *root directory tree* allotted in the TSB15LV01 is shown in Figure 3–1.

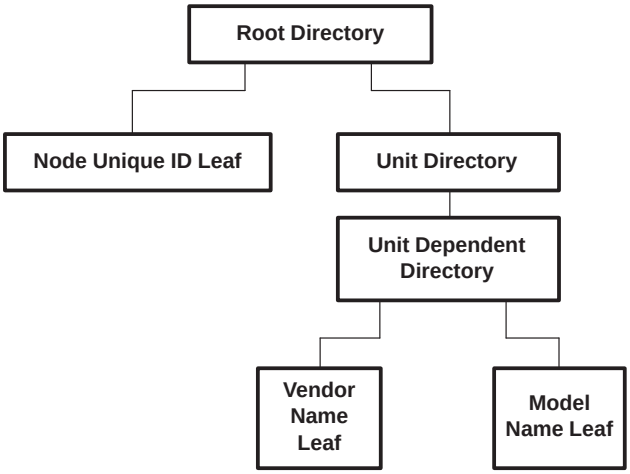


Figure 3–1. TSB15LV01 Root Directory Tree

The TSB15LV01 memory structure is based on this dynamic concept but assumes that all memory locations are fixed. Although all the components are present, including initial register space, root directory tree, and the appropriate pointers, these structures are assigned a fixed memory location. All memory locations can be legally addressed by their fixed addresses without needing to derive them from the corresponding base address and offset. (The exceptions to this rule are the vendor and model name leaves, discussed in section 3.3.1.2, Configuration ROM). This scheme provides efficient usage of EEPROM memory.

Because this memory structure is implemented in EEPROM, it is the responsibility of the system designer to ensure that it exists according to the maps shown in section 3. See section 2.5, EEPROM Interface, for more information.

3.2 Top-Level Memory Maps

The tables below give a top-level map of the TSB15LV01 address space. Along with the 1394 bus address, an *internal address* is given. This is the address scheme used inside the TSB15LV01 and also in interfacing with the EEPROM (see sections entitled Physical Location of Register Data and EEPROM Interface for more information).

Table 3–3. Top-Level Memory Map: 1394 Memory (Core CSRs)

1394 BUS ADDRESS	INTERNAL ADDRESS
FFFF F000 0000	
FFFF F000 0004	
FFFF F000 0008	0
FFFF F000 000C	1
FFFF F000 0010	2
FFFF F000 0014	3
FFFF F000 0018	5
FFFF F000 001C	6
FFFF F000 0200	8
FFFF F000 0204	9
FFFF F000 0208	10
FFFF F000 020C	11
FFFF F000 0210	12

Table 3–4. Top-Level Memory Map: 1394 Memory (Device Configuration ROM)

1394 BUS ADDRESS	INTERNAL ADDRESS	REGISTER NAME
FFFF F000 0400	13	BUS INFO BLOCK
FFFF F000 0404	14	
FFFF F000 0408	15	
FFFF F000 040C	16	
FFFF F000 0410	17	
FFFF F000 0414	18	ROOT DIRECTORY
FFFF F000 0418	19	
FFFF F000 041C	20	
FFFF F000 0420	21	
FFFF F000 0424	22	
FFFF F000 0428	23	NODE UNIQUE
FFFF F000 042C	24	
FFFF F000 0430	25	
FFFF F000 0434	26	UNIT DIRECTORY
FFFF F000 0438	27	
FFFF F000 043C	28	
FFFF F000 0440	29	
FFFF F000 0444	30	UNIT DEPENDENT DIRECTORY
FFFF F000 0448	31	
FFFF F000 044C	32	
FFFF F000 0450	33	
FFFF F000 0454	34	VENDOR NAME LEAF
FFFF F000 0458	35	
FFFF F000 045C	36	
FFFF F000 0460	37	
FFFF F000 0464	38	MODEL NAME LEAVES
FFFF F000 0468	39	
FFFF F000 046C	40	
FFFF F000 0470	41	
FFFF F000 0474	42	
FFFF F000 0478	43	
FFFF F000 047C	44	
FFFF F000 0480	45	
FFFF F000 0484	46	

Table 3–5. Top-Level Memory Map: Inquiry Registers

1394 BUS ADDRESS	INTERNAL ADDRESS	REGISTER NAME
FFFF F0F0 0000	64	CAMERA INITIALIZATION
FFFF F0F0 0100	65	FORMAT_INQ
FFFF F0F0 0180	66	VIDEO_MODE_INQ
FFFF F0F0 0200	67	RATE_INQ
FFFF F0F0 0204	68	
FFFF F0F0 0208	69	
FFFF F0F0 020C	70	
FFFF F0F0 0210	71	
FFFF F0F0 0214	72	
FFFF F0F0 0400	73	BASIC_FUNC_INQ
FFFF F0F0 0404	74	FEATURE_HI_INQ
FFFF F0F0 0408	75	FEATURE_LO_INQ
FFFF F0F0 0500	76	BRIGHTNESS_INQ
FFFF F0F0 0504	77	EXPOSURE_INQ
FFFF F0F0 0508	78	SHARPNESS_INQ
FFFF F0F0 050C	79	WHITE_BAL_INQ
FFFF F0F0 0510	80	HUE_INQ
FFFF F0F0 0514	81	SATURATION_INQ
FFFF F0F0 0518	82	GAMMA_INQ
FFFF F0F0 051C	83	SHUTTER_INQ
FFFF F0F0 0520	84	GAIN_INQ
FFFF F0F0 0524	85	IRIS_INQ
FFFF F0F0 0528	111	FOCUS_INQ
FFFF F0F0 0580	87	ZOOM_INQ
FFFF F0F0 0584	88	PAN_INQ
FFFF F0F0 0588	89	TILT_INQ

Table 3–6. Top-Level Memory Map: Control Registers

1394 BUS ADDRESS	INTERNAL ADDRESS	REGISTER NAME
FFFF F0F0 0600	90	CUR_V_FRM_RATE_CNTL
FFFF F0F0 0604	91	CUR_V_MODE_CNTL
FFFF F0F0 0608	92	CUR_V_FORMAT_CNTL
FFFF F0F0 060C	93	ISO_CHANNEL/SPEED_CNTL
FFFF F0F0 0610	94	CAMERA_POWER_CNTL
FFFF F0F0 0614	95	ISO_EN_CNTL
FFFF F0F0 0618	96	RESERVED
FFFF F0F0 061C	97	ONE_SHOT_CNTL
FFFF F0F0 0620	98	RESERVED
FFFF F0F0 0624	99	RESERVED
FFFF F0F0 0800	100	BRIGHTNESS_CNTL
FFFF F0F0 0804	101	EXPOSURE_CNTL
FFFF F0F0 0808	102	SHARPNESS_CNTL
FFFF F0F0 080C	103	WHITE_BAL_CNTL
FFFF F0F0 0810	104	RESERVED
FFFF F0F0 0814	105	SATURATION_CNTL
FFFF F0F0 0818	106	GAMMA_CNTL
FFFF F0F0 081C	107	SHUTTER_CNTL (BACKLIGHT COMPENSATION)
FFFF F0F0 0820	108	GAIN_CNTL
FFFF F0F0 0824	109	IRIS_CNTL
FFFF F0F0 0828	110	FOCUS_CNTL
FFFF F0F0 0880	112	ZOOM_CNTL
FFFF F0F0 0884	113	RESERVED
FFFF F0F0 0888	114	RESERVED

Table 3–7. Top-Level Memory Map: Configuration Registers

1394 BUS ADDRESS	INTERNAL ADDRESS	REGISTER NAME
FFFF F0F0 0F00	127	EEPROM_CNFG
FFFF F0F0 0F04	116	TEST_CNFG
FFFF F0F0 0F08	117	CCD_PULSE_CNFG
FFFF F0F0 0F0C	118	CDS_PULSE_CNFG
FFFF F0F0 0F10	119	AUTO_ADJ_CNFG
FFFF F0F0 0F14	120	DAC_OFFSET_CNFG
FFFF F0F0 0F18	121	CCD_OPTICS_CNFG
FFFF F0F0 0F1C	122	STATUS_CNFG
FFFF F0F0 0F20	123	VIDEO_OPTIONS_CNFG
FFFF F0F0 0F24	124	MOTOR_POSITION_CNFG

3.3 Register Detail

3.3.1 1394 Memory

The following sections define the CSR (Command and Status register) and ROM locations implemented in the TSB15LV01. For more information on the way 1394 CSR architectures are implemented, see section 3.1, 1394 Node Memory Architecture, and the 1394a specification.

3.3.1.1 Implemented Core CSRs

The TSB15LV01 implements the following core CSRs, defined in the IEEE 1212-1991 standard (upon which the 1394 standard is based). These are shown in Table 3–8.

Table 3–8. Implemented Core CSRs

Offset	0-7	8-15	16-23	24-31
FFFF F000 0000h	STATE_CLEAR			
FFFF F000 0004h	STATE_SET			
FFFF F000 0008h	NODE_IDS			
FFFF F000 000Ch	RESET_START			
FFFF F000 0010h				
FFFF F000 0014h				
FFFF F000 0018h	SPLIT_TIMEOUT_HI			
FFFF F000 001Ch	SPLIT_TIMEOUT_LO			

The TSB15LV01 implements the following serial-bus-dependent CSRs, defined by the 1394 standard. These are shown in Table 3–9.

Table 3–9. Serial-Bus-Dependent CSRs

Offset	0-7	8-15	16-23	24-31
FFFF F000 0200h	CYCLE_TIME			
FFFF F000 0204h				
FFFF F000 0208h				
FFFF F000 020Ch				
FFFF F000 0210h	BUSY_TIMEOUT			

3.3.1.2 Configuration ROM

The TSB15LV01 implements Configuration ROM defined in the IEEE 1212-1991 standard, shown in Table 3–10.

Table 3–10. Base Configuration ROM

NAME	Offset	0-7	8-15	16-23	24-31
Bus info block	FFFF F000 0400h	04h	crc_length	rom_crc_value	
	FFFF F000 0404h	31h (1)	33h (3)	39h (9)	34h (4)
	FFFF F000 0408h	0 0 1 0 rsv	FFh	max_rec	rsrv
	FFFF F000 040Ch	node_vendor_id			chip_id_hi
	FFFF F000 0410h	chip_id_lo			
Root directory	FFFF F000 0414h	0004h		CRC	
	FFFF F000 0418h	03h	module_vendor_ID value		
	FFFF F000 041Ch	06h	module_sw_version (070198h)		
	FFFF F000 0420h	0Dh	Node_Unique_ID indirect_offset (000002h)		
	FFFF F000 0424h	11h	unit_directory offset (000004h)		

Note that the last two quadlets of Table 3–10 are entries that point to a leaf and a directory, respectively. The leaves are shown in Table 3–11 and Table 3–12.

Table 3–11. Node_Unique_ID Leaf

NAME	Offset	0-7	8-15	16-23	24-31
Node_ Unique_ID leaf	FFFF F000 0428h	0002h		CRC	
	FFFF F000 042Ch	node_vendor_ID			chip_id_hi
	FFFF F000 0430h	chip_id_lo			

Table 3–12. Unit Directory

NAME	Offset	0-7	8-15	16-23	24-31
Unit directory	FFFF F000 0434h	0003h		CRC	
	FFFF F000 0438h	12h	unit_spec_ID (=0x00A02D)		
	FFFF F000 043Ch	13h	unit_sw_version (=0x000100)		
	FFFF F000 0440h	D4h	unit_dependent_directory offset		

The last quadlet of the unit directory in Table 3–12 contains an offset to another directory, shown below in Table 3–13.

Table 3–13. Unit-Dependent Directory

NAME	Offset	0-7	8-15	16-23	24-31
Unit-dependent directory	FFFF F000 0444h	unit_dep_info_length		CRC	
	FFFF F000 0448h	40h	command_regs_base		
	FFFF F000 044Ch	81h	vendor_name_leaf		
	FFFF F000 0450h	82h	model_name_leaf		

In the unit-dependent directory, *command_regs_base* points to the base address of the inquiry, control, and configuration registers (FFFF F0F0 0000h). It is expressed in terms of quadlets, relative to the base address of initial register space (FFFF F000 0000h).

Two leaves are provided that should contain ASCII strings representing the camera vendor and model names. These are referred to as the *vendor name leaf* and *model name leaf.* The unit-dependent directory also contains pointers to these leaves. *Vendor_name_leaf* specifies the number of quadlets from the address of the *vendor_name_leaf* entry (FFFF F000 044Ch) to the address of the vendor name leaf. *Model_name_leaf* specifies the number of quadlets from the address of the *model_name_leaf* entry (FFFF F000 0450h) to the address of the model name leaf.

The format of the vendor and model name leaves is shown in Table 3–14 and Table 3–15.

Table 3–14. Vendor Name Leaf

NAME	Offset	0-7	8-15	16-23	24-31
Vendor name leaf	FFFF F000 0454h	leaf_length		CRC	
	FFFF F000 0458h	00h	00 0000h		
	FFFF F000 045Ch	0000 0000h			
	FFFF F000 0460h	char_0	char_1	char_2	char_3

Table 3–15. Model Name Leaf

NAME	Offset	0-7	8-15	16-23	24-31
Model name leaf	FFFF F000 0464h	leaf_length		CRC	
	FFFF F000 0468h	00h	00 0000h		
	FFFF F000 046Ch	0000 0000h			
	FFFF F000 0470h	char_0	char_1	char_2	char_3
Model name leaf	FFFF F000 0474h	char_4	char_5	char_6	char_7
	FFFF F000 047Ch	char_8	…		
	FFFF F000 0480h	…			char + n – 3
	FFFF F000 0480h	char_n – 2	char_n – 1	NUL	NUL

Notice that these leaves have length that varies according to the length of the ASCII strings. A total of 13 quadlets is provided for these two leaves. Because each leaf contains a three-quadlet header, seven quadlets are available for ASCII characters. These seven quadlets can be appropriated in any way between the two name leaves, providing that the *directory length* field in each leaf reflects the appropriation. Also, the *vendor_name_leaf* and *model_name_leaf* fields in the unit-dependent directory leaf must point to their appropriate leaves. This is especially important for the model name leaf, since its address can move depending on the length of the vendor name leaf.

3.3.2 Inquiry Registers

The Digital Camera Specification provides for a wide variety of features a vendor can choose to implement. However, a compliant camera must include a series of registers that indicate exactly which of the standard features are supported. These *inquiry registers* also provide some basic information about the way in which the camera supports these features, such as whether an automatic control exists.

These values are determined during camera system development and must be written to the EEPROM when cameras are built. The TSB15LV01 supports the majority of features provided under the Digital Camera Specification.

Note that setting these values does not change any camera functionality. It only changes what the host perceives the capability of the camera to be.

The inquiry registers have a base destination offset of FFFF F0F0 0000h. In the tables that follow, all listed offsets are specified in bytes, relative to this base address. Most fields serve as Boolean flags that indicate availability of the feature, with a 1 indicating availability. Other types of fields are marked accordingly.

3.3.2.1 Video Format Inquiry Register

The video format describes the format of the video information being transmitted by the TSB15LV01 across the 1394 serial bus. The only format supported by v1.04 of the digital camera specification is VGA non-compressed data, which has a maximum of 640 x 480 resolution. Space is reserved for future expansion to other formats.

Table 3–16. Video Format Memory Map

NAME	OFFSET	0–7		8–15	16–23	24–31
FORMAT_INQ	100h	Format_0	Format_x	Rsrv		

Table 3–17. Video Format Register Proper Values for TSB15LV01

NAME	OFFSET	0–7		8–15	16–23	24–31
FORMAT_INQ	100h	1	XXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Table 3–18. Video Format Field Descriptions

FIELD NAME	BITS	DESCRIPTION
Format_0	0	VGA noncompressed format. (Maximum 640 x 480)
Format_x	1..7	Reserved for other formats
Reserved	8..31	Reserved (all zero)

3.3.2.2 Video Mode Inquiry Registers

The video mode describes the type of data output by the digital camera. These modes correspond with those described in section 2.1.2.1, Isochronous Packet Format/Protocol.

The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address. All fields are Boolean flags; a 1 indicates availability.

Table 3–19. Video Mode Memory Map

NAME	OFFSET	0–7							8–15	16–23	24–31
VIDEO_MODE_INQ_0 (640 × 480 VGA Format)	100h	Mode_0	Mode_1	Mode_2	Mode_3	Mode_4	Mode_5	Mode_x	Rsrv		
VIDEO_MODE_INQ_0	184h..19Fh	Reserved for other formats									

Table 3–20. Video Mode Proper Values for TSB15LV01

NAME	OFFSET	0–7							8–15	16–23	24–31
VIDEO_MODE_INQ_0 (640 × 480 VGA Format)	100h	1	1	1	1	1	1	XX	XXXXXXXX	XXXXXXXX	XXXXXXXX
VIDEO_MODE_INQ_0	184h..19Fh	XXXXXXXX							XXXXXXXX	XXXXXXXX	XXXXXXXX

Table 3–21. Video Mode Field Descriptions

FIELD NAME	BITS	DESCRIPTION
Mode_0	0	160 × 120 YUV(4:4:4) Mode (24 bit/pixel)
Mode_1	1	320 × 240 YUV(4:2:2) Mode (16 bit/pixel)
Mode_2	2	640 × 480 YUV(4:1:1) Mode (12 bit/pixel)
Mode_3	3	640 × 480 YUV(4:2:2) Mode (16 bit/pixel)
Mode_4	4	640 × 480 RGB Mode (24 bit/pixel)
Mode_5	5	640 × 480 Y (Mono) Mode (8 bit/pixel)
Mode_x	6..7	Reserved for other modes
Reserved	8..31	Reserved (all zero)

3.3.2.3 Video Frame Rate Inquiry Registers

These registers describe the availability of the various frame rates for the digital camera. A separate register is provided for each combination of format and mode, and this relationship is shown in Table 3–22.

The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address. All fields are Boolean flags; a 1 indicates availability.

Table 3–22. Video Frame Rate Memory Map

NAME	OFFSET	0–7						8–15	16–23	24–31
RATE_INQ_0 (160 × 120 YUV (4:4:4))	200h	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_x	Rsrv		
RATE_INQ_1 (320 × 240 YUV (4:2:2))	204h	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_x	Rsrv		
RATE_INQ_2 (320 × 240 YUV (4:1:1))	208h	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_x	Rsrv		
RATE_INQ_3 (640 × 480 YUV (4:2:2))	20Ch	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_x	Rsrv		
RATE_INQ_4 (640 × 480 RGB)	210h	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_x	Rsrv		
RATE_INQ_5 (640 × 480 Mono)	214h	Frame Rate_0	Frame Rate_1	Frame Rate_2	Frame Rate_3	Frame Rate_4	Frame Rate_5 | Frame Rate_x	Rsrv		

Table 3–23. Video Frame Rate Proper Values for TSB15LV01

NAME	OFFSET	0-7							8-15	16-23	24-31
RATE_INQ_0	200h	X	0	1	1	1	XXX		XXXXXXXX	XXXXXXXX	XXXXXXXX
RATE_INQ_1	204h	X	1	1	1	1	XXX		XXXXXXXX	XXXXXXXX	XXXXXXXX
RATE_INQ_2	208h	X	1	1	1	1	XXX		XXXXXXXX	XXXXXXXX	XXXXXXXX
RATE_INQ_3	20Ch	X	1	1	1	0	XXX		XXXXXXXX	XXXXXXXX	XXXXXXXX
RATE_INQ_4	210h	X	1	1	1	0	XXX		XXXXXXXX	XXXXXXXX	XXXXXXXX
RATE_INQ_5	214h	X	1	1	1	1	0	XX	XXXXXXXX	XXXXXXXX	XXXXXXXX

Table 3–24. Video Frame Rate Field Descriptions

FIELD NAME	BITS	DESCRIPTION
FrameRate_0	0	Reserved
FrameRate_1	1	3.75 fps
FrameRate_2	2	7.5 fps
FrameRate_3	3	15 fps
FrameRate_4	4	30 fps
FrameRate_5	5	60 fps
FrameRate_x	5..7	Reserved for another frame rate
FrameRate_y	6..7	Reserved for another frame rate
Reserved	6..31	Reserved (all zero)

3.3.2.4 Basic Function Inquiry Register

This register describes the availability of some top-level features.

The base address is FFFF F0F0 0000h. The listed offset is specified in bytes, relative to this base address. All fields are Boolean flags; a 1 indicates availability.

Table 3–25. Memory Map for Basic Function Register

NAME	OFFSET	0–7	8–15	16–23				24–31
BASIC_FUNC_INQ	400h	Rsrv		cam_power_inq		one_shot_inq	Rsrv	Memory_ Channel

Table 3–26. Basic Function Register Proper Values for TSB15LV01

NAME	OFFSET	0–7	8–15	16–23					24–31	
BASIC_FUNC_INQ	400h	XXXXXXXX	XXXXXXXX	1	X	X	1	XXXX	XXXX	0000

Table 3–27. Field Descriptions for Basic Function Register

FIELD NAME	BITS	DESCRIPTION
Reserved	0..15	Reserved
cam_power_inq	16	Camera process power on/off capability
Reserved	17..18	Reserved
one_shot_inq	19	One shot transmission capability
Reserved	20..27	Reserved
memory_channel	28..31	Maximum memory channel number (N) Memory channel number 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N = Memory Ch N If 0000, user memory is not available.

3.3.2.5 Feature Presence Inquiry Registers

These registers indicate the availability of some low level features.

The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address. All fields are Boolean flags; a 1 indicates availability.

Table 3–28. Memory Map for Feature Presence Registers

NAME	OFFSET	0–7								8–15				16–23	24–31
FEATURE_HI_INQ	404h	Brightness	Exposure	Sharpness	White_Balance	Hue	Saturation	Gamma	Shutter	Gain	Iris	Focus	Rsrv		
FEATURE_LO_INQ	408h	Zoom	Pan	Tilt	Rsrv										

Table 3–29. Feature Presence Registers Proper Values for TSB15LV01

NAME	OFFSET	0–7								8–15				16–23	24–31
FEATURE_HI_INQ	404h	1	1	1	1	0	1	1	1	1	?	?	XXXXX	XXXXXXXX	XXXXXXXX
FEATURE_LO_INQ	408h	?	0	0	XXXXX					XXXXXXX				XXXXXXXX	XXXXXXXX

Table 3–30. Field Descriptions for Feature Presence Registers

FIELD NAME	BITS	DESCRIPTION
Brightness	0	Brightness control
Exposure	1	Exposure control
Sharpness	2	Sharpness control
White_Balance	3	White Balance control
Hue	4	Hue control
Saturation	5	Saturation control
Gamma	6	Gamma control
Shutter	7	Shutter control†
Gain	8	Gain control
Iris	9	Iris control‡
Focus	10	Focus control‡
	11..31	Reserved
Zoom	0	Zoom control‡
Pan	1	Pan control
Tilt	2	Tilt control
	3..31	Reserved

† On the TSB15LV01, the shutter register controls the backlight compensation feature.

‡ The proper setting of these bits depends on whether the designer has implemented focus, zoom, and iris motorized controls on the camera.

3.3.2.6 Feature Elements Inquiry Registers

These registers indicate the availability of features provided in the Digital Camera Specification. All registers are supported except hue, pan, and tilt, and this is reflected in the proper values in Table 3–31. (Note that pan and tilt features can still be supported, as described in section 2.4, Motor Control Interface).

The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address. All fields are Boolean flags; a 1 indicates availability.

Table 3–31. Memory Map for Feature Elements Inquiry Registers

NAME	OFFSET	0–7								8–15	16–23	24–31
BRIGHTNESS_INQ	500h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
EXPOSURE_INQ	504h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
SHARPNESS_INQ	508h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
WHITE_BAL_INQ	50Ch	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
HUE_INQ	510h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
SATURATION_INQ	514h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
GAMMA_INQ	518h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
SHUTTER_INQ†	51Ch	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
GAIN_INQ	520h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
IRIS_INQ‡	524h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
FOCUS_INQ‡	528h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
ZOOM_INQ‡	580h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
PAN_INQ	584h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	
TILT_INQ	588h	Presence				Readout	On/Off	Auto	Manual	min_value	max_value	

† On the TSB15LV01, the shutter register controls the backlight compensation feature

‡ The proper setting of these bits depends on whether the designer has implemented focus, zoom, and iris motorized mechanisms on the camera, and the individual characteristics of those mechanisms.

Table 3–32. Feature Elements Registers Proper Values for TSB15LV01

NAME	OFFSET	0-7						8-15	16-23	24-31
BRIGHTNESS_INQ	500h	1	XXX	1	0	1	1	000		1FF
EXPOSURE_INQ	504h	1	XXX	1	0	1	1	000		1FF
SHARPNESS_INQ	508h	1	XXX	1	0	0	1	000		0FF
WHITE_BAL_INQ	50Ch	1	XXX	1	0	1	1	000		0FF
HUE_INQ	510h	0	XXX	X	X	X	X	XXX		XXX
SATURATION_INQ	514h	1	XXX	1	0	0	1	000		0FF
GAMMA_INQ	518h	1	XXX	1	0	0	1	000		001
SHUTTER_INQ†	51Ch	1	XXX	1	0	0	1	000		007
GAIN_INQ	520h	1	XXX	1	0	0	1	000		0FF
IRIS_INQ‡	524h	?	XXX	1	0	0	1	???		???
FOCUS_INQ‡	528h	?	XXX	1	0	0	1	???		???
ZOOM_INQ‡	580h	?	XXX	1	0	0	1	???		???
PAN_INQ	584h	0	XXX	X	X	X	X	XXX		XXX
TILT_INQ	588h	0	XXX	X	X	X	X	XXX		XXX

† On the TSB15LV01, the shutter register controls the backlight compensation feature

‡ The proper setting of these bits depends on whether the designer has implemented focus, zoom, and iris motorized mechanisms on the camera, and the individual characteristics of those mechanisms.

Table 3–33. Field Descriptions for Feature Elements Registers

FIELD NAME	BITS	DESCRIPTION
Presence	0	Presence of this feature
	1..3	Reserved
ReadOut	4	Capability of reading the value of this feature§
On/Off	5	Capability of switching this feature on and off
Auto	6	Auto mode (in which the feature is controlled automatically by camera)
Manual	7	Manual mode (in which the feature is controlled directly by user)
MIN_Value	8..19	MIN Value for this feature control
MAX_Value	20..31	MAX Value for this feature control

§ All control values in manual mode can be read. Values cannot be read during auto modes.

3.3.3 Control and Configuration Registers

These registers are used to control the digital camera, as well as allowing the host to read camera status. The control registers are required by the Digital Camera Specification. They control some of the basic camera operations, such as frame rate, output format, and video parameters. The configuration registers are unique to the TSB15LV01. They allow the user to configure features unique to the TSB15LV01 and fine-tune its interface with supporting components.

As with the inquiry registers, the control and configuration registers have a base destination offset of FFFF F0F0 0000h. In the tables that follow, all listed offsets are specified in bytes, relative to this base address.

3.3.3.1 Control Registers

As stated earlier, all features provided for by the digital camera specification are listed.

3.3.3.1.1 Camera Initialize Register

This register is not used on the TSB15LV01.

Table 3–34. Camera Initialize Register Memory Map

NAME	OFFSET	0–7	8–15	16–23	24–31
INITIALIZE	000h	Rsrv			

Table 3–35. Camera Initialize Register Field Descriptions

FIELD CODE	BITS	DESCRIPTION
Rsrv	0..31	Reserved (all zero)

3.3.3.1.2 Function Control Registers

These registers control the basic functionality of the camera. The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address.

Table 3–36. Memory Map for Camera Registers

NAME	OFFSET	0–7	8–15	16–23	24–31
CUR_V_FRM_RATE_CNTL	600h	Frame_Rate	Rsrv		
CUR_V_MODE_CNTL	604h	Video_Mode	Rsrv		
CUR_V_FORMAT_CNTL	608h	Video_Format	Rsrv		
ISO_CHANNEL/SPEED_CNTL	60Ch	Iso_Chnl	Iso_Speed	Rsrv	
CAMERA_POWER_CNTL	610h	Cam_Power	Rsrv		
ISO_EN_CNTL	614h	Iso_Enable	Rsrv		
RSRV	618h	Rsrv			
ONE_SHOT_CNTL	61Ch	One_Shot	Rsrv		
RSRV	620h.. 624h	Rsrv			

Table 3–37. Field Descriptions for Camera Registers

FIELD NAME	BITS	DESCRIPTION
Frame_rate	0..2	Current frame rate (FrameRate_0 .. FrameRate_7)
Video_mode	0..2	Current video mode (Mode_0 .. Mode_7)
Video_format	0..2	Current video format (Format_0 .. Format_7)
Iso_chnl	0..3	1394 isochronous channel number for video data transmission (0-15)
	4..5	Reserved
Iso_speed	6..7	1394 isochronous transmit speed code 0 = s100 1 = s200 2 = s400
Cam_power	0	This register determines the on/off status of the TSB15LV01. It also directly controls the CAM_POWER terminal of the device, which can be used to control power to the CCD. 1 = power up camera 0 = power down camera.
Iso_Enable	0	1 = start isochronous transmission of video data 0 = stop isochronous transmission of video data
One_shot	0	1 = only one frame of video data is transmitted. Self-cleared after transmission. Ignored if *ISO_EN_CNTL* (field *iso_en*) = 1.

3.3.3.1.3 Feature Control Registers

These registers control features pertaining to video processing and motor control.

The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address.

Table 3–38. Memory Map for Feature Control Registers

NAME	OFFSET	0–7				8–15	16–23	24–31
BRIGHTNESS_CNTL	800h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
EXPOSURE_CNTL	804h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
SHARPNESS_CNTL	508h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
WHITE_BAL_CNTL	80Ch	Presence		On/Off	Manual	U_Value		V_Value
RSRV	510h	Rsrv						
SATURATION_CNTL	814h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
GAMMA_CNTL	818h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
SHUTTER_CNTL†	81Ch	Presence	Rsrv	On/Off	Manual	Rsrv		Value
GAIN_CNTL	820h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
IRIS_CNTL	824h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
FOCUS_CNTL	828h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
RSRV	82Ch.. 87CH	Rsrv						
ZOOM_CNTL	580h	Presence	Rsrv	On/Off	Manual	Rsrv		Value
RSRV	884h.. 8FCH	Rsrv						

† On the TSB15LV01, the shutter register controls the backlight compensation feature.

Table 3–39. Field Descriptions for Feature Registers

FIELD NAME	BITS	DESCRIPTION
Presence	0	Presence of this feature should match the value in the corresponding feature control inquiry register. 0 : Not available 1 : Available
Reserved	1..5	Reserved
ON_OFF	6	If this field is written to, it turns the feature on or off (1 or 0, respectively). If this field is read, it indicates the on/off status of the feature. (As the inquiry registers indicate, this feature is not enabled for any of the controls in the TSB15LV01.)
A_M_Mode	7	Indicates whether an automatic mode is active for this feature. Writing to this field changes the mode status. Reading from it indicates the mode status. 0 : Manual 1 : Auto
	8..19	Reserved.
Value	20..31	Value associated with the feature. If a value is written to this field while A_M_Mode indicates auto mode, this field is ignored. If readout capability for this feature is not available as indicated by the corresponding feature elements inquiry register, the value read from this address has no meaning.
U_Value	8..19	U-Value. Target U-value for white balance. If a value is written when A_M_Mode indicates auto mode, this field is ignored. If readout capability for this feature is not available (see Feature Elements Inquiry Register), the value read from this address has no meaning.
V_Value	20..31	V-Value. Target U-value for white balance. If a value is written when A_M_Mode indicates auto mode, this field is ignored. If readout capability for this feature is not available (see Feature Elements Inquiry Register), the value read from this address has no meaning.

3.3.3.1.2 Configuration Registers

These registers control features and enhancements that are unique to the TSB15LV01. Most of these features have been addressed in prior sections of this document when applicable.

Table 3–40 shows a memory map of the configuration registers. The base address is FFFF F0F0 0000h. All listed offsets are specified in bytes, relative to this base address.

Table 3–40. Configuration Register Memory Map

NAME	OFFSET	0	1	2	3	4	5	6	7
EEPROM_CNFG	0F00h	write_protect_control							
TEST_CNFG	0F04h	test_en	RSRV						
CCD_PULSE_CNFG	0F08h	RSRV							
		RSRV		h2					
		RSRV		rst_rg					
		RSRV		srg_h1					
CDS_PULSE_CNFG	0F0Ch	RSRV		adclk					
		RSRV							
		RSRV		sv					
		RSRV		sr					
AUTO_ADJ_CNFG	0F10h	stable							
		min_gain							
		expo_delta_high					expo_delta_low		
		expo_ref							
DAC_OFFSET_CNFG	0F14h	dac2_en	bloom_en	RSRV					
		dac2_value							
		blooming_value							
		offset_level							
CCD_OPTICS_CNFG	0F18h	filter_limit							
		RSRV						filter	
		RSRV				h-center			
		RSRV				v-center			
STATUS_CNFG	0F1Ch	RSRV					stat_input		
		RSRV					stat2		
		RSRV					stat1		
		RSRV					stat0		
AFE_SETUP_CNFG	0F20h	lines_smpl				pixels_smpl			
		internal_bias				ccd_sel			afe_sel
VIDEO_OPTIONS_CNFG	0F22h	RSRV				h_inv	v_inv	rb_shift	ad_inv
		Hz	RSRV					color_bw	pix_shp

Table 3–40. Configuration Register Memory Map (Continued)

NAME	OFFSET	0	1	2	3	4	5	6	7
MOTOR_POS_CNFG	0F24h	ir_en	RSRV	ir_zoom (msb)					
		ir_zoom (lsb)				ir_focus (msb)			
		ir_focus (lsb)						ir_iris (msb)	
		ir_iris (lsb)							

Table 3–41. Field Descriptions for Configuration Registers

REGISTER	FIELD CODE	BITS	DESCRIPTION
EEPROM_CNFG	write_protect_ control	0..31	Write protect control code. Allows write access to EEPROM. Writing 12345678h unlocks, all other values lock.
TEST_CNFG	test_en	0	Color bar test pattern. Setting this bit high enables color bar test pattern
CCD_PULSE_CNFG	h2	10..15	H2 pulse position. H2 pulse placement register. 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
	rst	18..23	RST pulse position. RST pulse placement register. 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
	srg/h1	26..31	SRG/H1 pulse position. SRG/H1 pulse placement register 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
CDS_PULSE_CNFG	adclk	2..7	ADCLK pulse position. ADCLK pulse placement register. 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
	sv	18..23	SV pulse position. SV pulse placement register. 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
	sr	26..31	SR pulse position. SR pulse placement register. 00h : places it at the nominal value for the chosen CCD 3Fh : places it at maximum delay
AUTO_ADJ_CNFG	stable	0..7	Number of frames before enabling auto exposure. Gives the image time to stabilize at start-up to prevent oscillation.
	min_gain	8..15	Minimum gain to saturate CCD
	expo_delta_ high	16..20	Speed control adjustment for auto exposure loop. Applies to frames in which the average luminance is very far away from the level specified in expo_ref. As this value is increased, adjustments are made to gain/exposure more quickly, but setting higher than 11011b can lead to instability. Recommended value is 10011b.
	expo_delta_ medium	21..23	Speed control adjustment for auto exposure loop. Applies to frames in which the average luminance is deviant from the level specified in expo_ref, but not to the extent as those to which expo_delta_high applies. As this value is increased, adjustments are made to gain/ exposure more quickly. Recommended value is 010b.
	expo_ref	24..31	Autoexposure reference. Target value used in the auto-gain and -exposure feedback loop. This value is the average luminance of the hot region sampled for the autoexposure loop.

Table 3–41. Field Descriptions for Configuration Registers (Continued)

REGISTER	FIELD CODE	BITS	DESCRIPTION
DAC_OFFSET_CNFG	dac2_en	0	DAC-2 enable. Enables output to general purpose DAC in AFE 0 : Disabled 1 : Enabled
	bloom_en	1	Blooming DAC enable. Enables output to general purpose DAC in AFE, configured to supply blooming reference values to the CCD. 0 : Disabled 1 : Enabled
	dac2_value	8..15	DAC-2 value. Output value for DAC-2 (see DAC-2 Enable, above)
	blooming_value	16..23	Blooming DAC value. Output value for Blooming DAC (see Blooming DAC Enable, above)
	offset_ level	24..31	Black offset reference. Black reference value for digital black clamping. Recommended value is 40h.
CCD_OPTICS_CNFG	filter_limit	0..7	Filter limit. Specifies the maximum amount of error allowed when the non-linear interpolation white spot compensation filter is used (see *filter* field).
	filter	8..15	White spot compensation filter select. Selects between two white-spot compensation filters implemented in the TSB15LV01, or de-activates the filter. 0 : Off 1 : Median Filter 2 : Non-linear Interpolation (requires limit value in *filter_limit* field, above)
	h-center	20..23	Lens horizontal center. Indicates the horizontal position of the CCD image's upper left corner, with respect to the left-most active pixels (does not include dummy and black pixels)
	v-center	28..31	Lens vertical center. Indicates the vertical position of the CCD image's upper left corner, with respect to the top-most pixels (does not include dummy and black pixels)
STATUS_CNFG	st_stat	5..7	Status terminal input/output. Indicates the value being read from or written to the STAT2, STAT1, and STAT0 terminals, in order from MSB to LSB. If STAT2, STAT1, or STAT0 is configured as an output, writing to this register changes the output of that terminal.
	stat2	13..15	STAT2 configuration. Indicates which STAT input/output is tied to the STAT2 terminal. See Table 2-3-1 for corresponding values.
	stat1	21..23	STAT1 configuration. Indicates which STAT input/output is tied to the STAT1 terminal. See Table 2-3-1 for corresponding values.
	stat0	29..31	STAT0 configuration. Indicates which STAT input/output is tied to the STAT0 terminal. See Table 2-3-1 for corresponding values.
AFE_SETUP_CNFG	lines_smpl	0..3	Lines per image. This value is sent to the AFE to tell it the number of lines per image that should be sampled for black clamping.
	pixels_smpl	4..7	Black clamp sampling. This value is sent to the AFE to tell it the number of pixels per line that should be sampled for black clamping.
	internal_bias	8..11	AFE bias current. Set to 0110b.
	ccd_sel	12..14	CCD Select. Indicates the CCD being used with this device. 0 : TI TC237 1/3 B&W sensor (if this is selected, *color_bw* field in *VIDEO_OPTIONS_CNFG* must be cleared also. 1 : Sony ICX084AK 1/3 color sensor 2 : Sony ICX098AK ¼ color sensor; Sharp LZ24BP 1/3 color sensor
	afe_sel	15	Always set to 1.

Table 3–41. Field Descriptions for Configuration Registers (Continued)

REGISTER	FIELD CODE	BITS	DESCRIPTION
VIDEO_OPTIONS_CNFG	h_inv	20	Horizontal CCD pulse inversion. Inverts all horizontal drive pulses. Recommended value is 0. 0 : No inversion 1 : Inversion
	v_inv	21	Vertical CCD pulse inversion. Inverts all vertical drive pulses. Recommended value is 0. 0 : No inversion 1 : Inversion
	rb_shft	22	Red/Blue pixel shift. Indicates whether one-color pixel shift is implemented. Recommended value is 1. 0 : No pixel shift 1 : Pixel shift
	ad_inv	23	ADCLK Inversion. Inverts pulses from the ADCLK terminal. Recommended value is 0. 0 : No inversion 1 : Inversion
	Hz	24	Integration Hz. Reduces the actual frame rate to approximately 83.3% of the one indicated in the *CUR_V_FRM_RATE _CNTL* register. For example, 30 fps becomes 25 fps. This can be used to reduce flicker in countries using 50-Hz lighting. 0 : No reduction 1 : Reduction
	color_bw	30	Color/BW. Indicates the type of CCD being used. 0 : Black and white CCD (TC237 only) 1 : Color CCD (all others)
	pix_shp	31	Pixel shape. Indicates the way CCD pixel data are interpreted. 0 : L-Shaped pixels 1 : Square pixels
MOTOR_POS_CNFG	ir_enable	0	IR_Enable. Used internally.
	ir_zoom	2..11	IR_Zoom. Starting position (IR sensor location) of the zoom stepper motor.
	ir_focus	12..21	IR_Focus. Starting position (IR sensor location) of the focus stepper motor.
	ir_iris	22..31	IR_Iris. Starting position (IR sensor location) of the iris stepper motor.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$ (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$ (see Note 2) . . . . . ±20 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Virtual junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies to external input and bidirectional buffers.
2. This applies to external output and bidirectional buffers.

4.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Input voltage, V_I	0		V_{CC}	V
Output voltage, V_O (see Note 3)	0		V_{CC}	V
High-level input voltage, V_{IH}	$0.7V_{CC}$		V_{CC}	V
Low-level input voltage, V_{IL}	0		$0.3V_{CC}$	V
Input transition time, t_f and t_r (10% to 90%)	0		25	ns
Operating free-air temperature, T_A	0	25	70	°C
Virtual junction temperature, T_{JC} (see Note 4)	0	25	115	°C

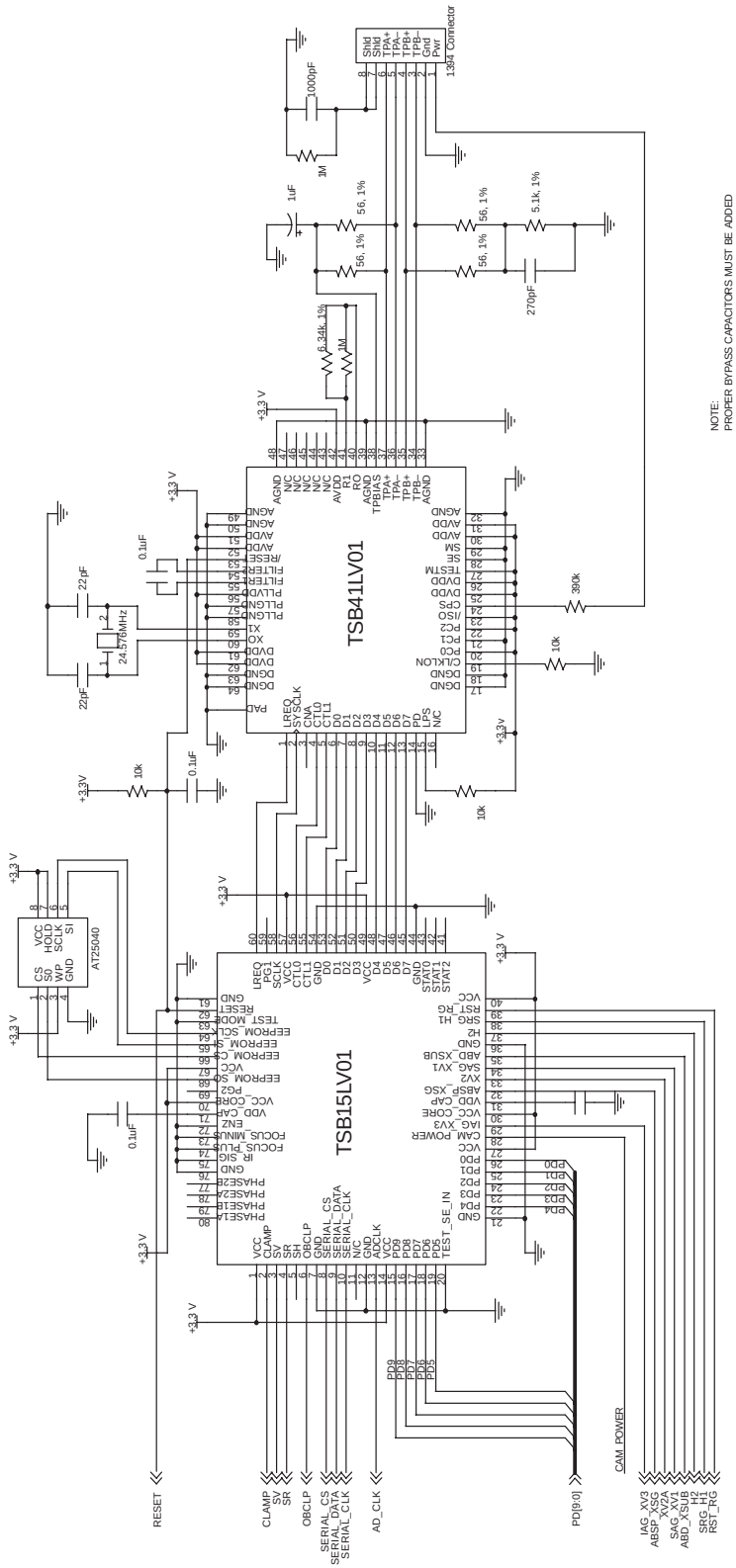
NOTES: 3. This applies to external output buffers.
4. The junction temperatures listed reflect simulation conditions. The customer is responsible for verifying the junction temperature.

4.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

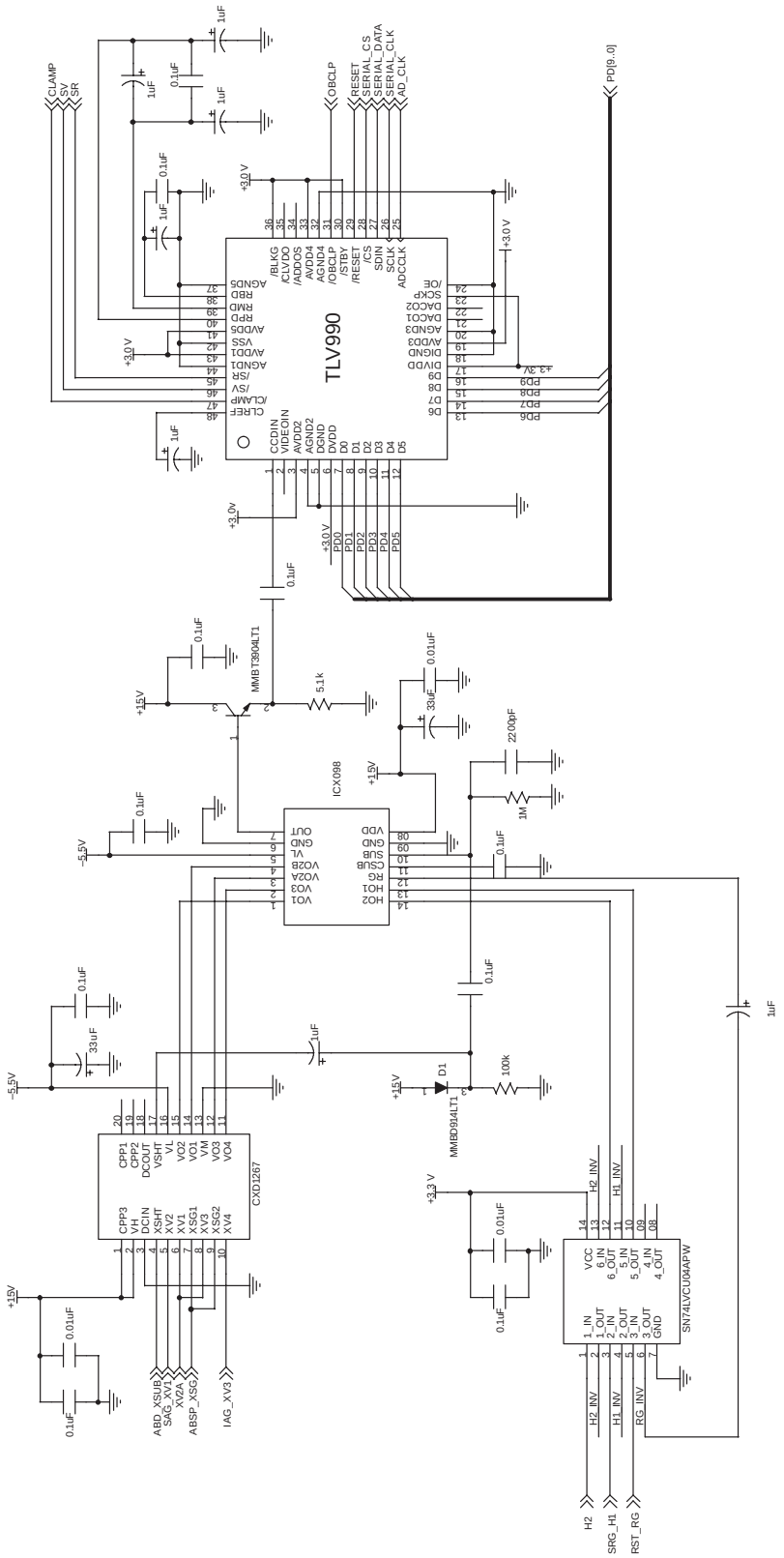
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –12 mA‡		$0.8V_{CC}$			V
		I_{OH} = –8 mA§		$0.8V_{CC}$			
V_{OL}	Low-level output voltage	I_{OL} = 24 mA‡				$0.22V_{CC}$	V
		I_{OL} = 8 mA§				$0.22V_{CC}$	
I_{IL}	Low-level input current	$V_I = V_{IL}$				–1	µA
I_{IH}	High-level input current	$V_I = V_{IH}$				1	µA
I_{OZ}	High-impedance output current	$V_O = V_{CC}$ or GND				±20	µA
$I_{CC(Q)}$	Static supply current	All V_{CC} and $V_{CC_}$CORE terminals	CAMERA_POWER_CNTL and ISO_EN_CNTL activated		22		mA
			CAMERA_POWER_CNTL and ISO_EN_CNTL deactivated		27		

† All typical characteristics are measured at V_{CC} = 3.3 V and T_A = 25°C.
‡ For ABSP_XSG, IAG_XV3, SAG_XV1, ABD_XSUB, SRG_H1, RST_RG
§ For all other outputs.

5 Application Information



Sheet 2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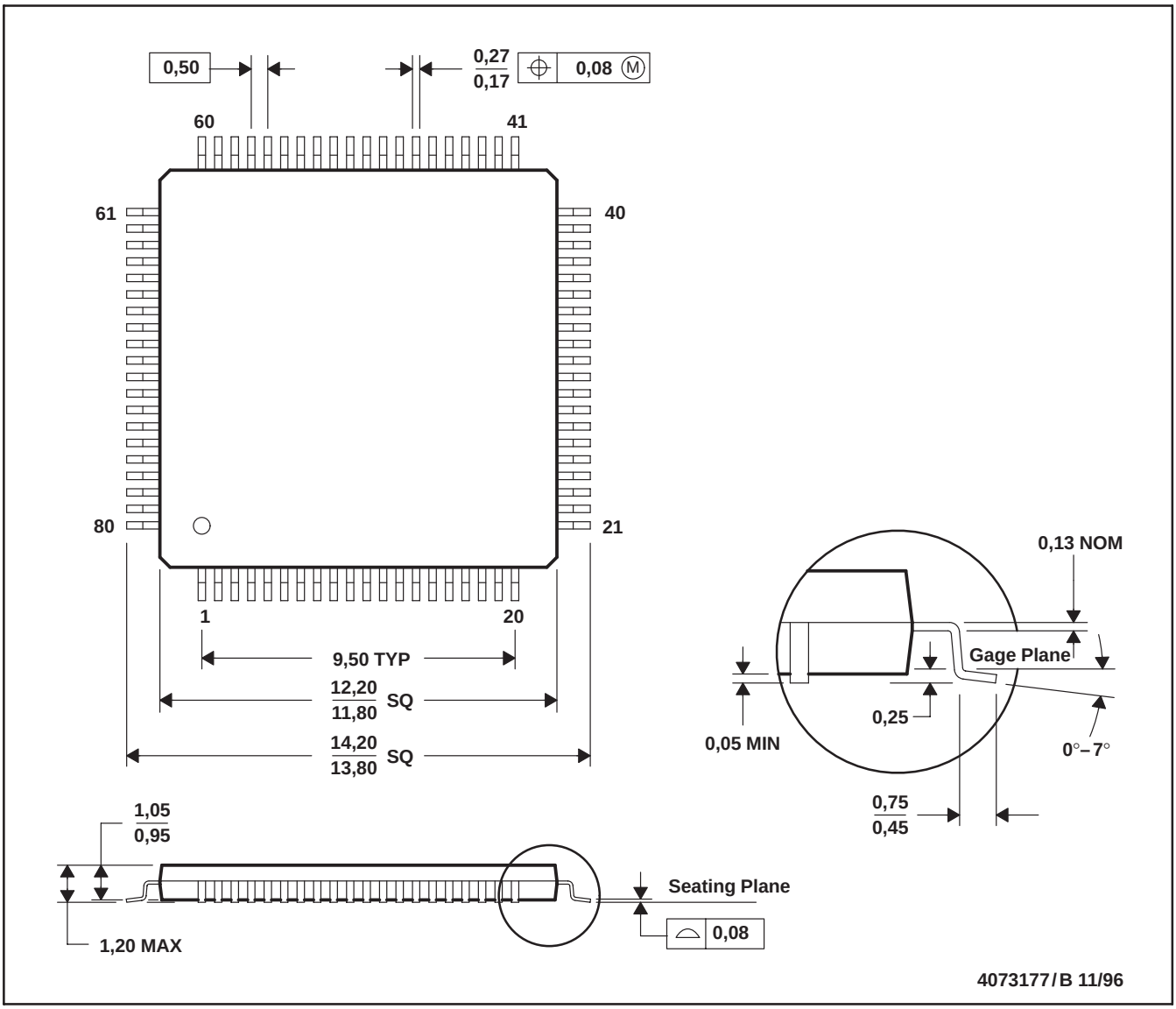
ICX098
CXD1267
SN74LVCU04APW
MMBT3904LT1
MMBD914LT1
CLAMP
SV
SR
OBCLP
RESET
SERIAL_CS
SERIAL_DATA
SERIAL_CLK
AD_CLK
PD[9..0]
+3.0 V
+15V
−5.5V
+3.3 V
0.1uF
0.01uF
1uF
33uF
5.1k
100k
1M
220pF
H2
SRG_H1
RST_RG
H2_INV
H1_INV
RG_INV
ABD_XSUB
SAG_XV1
ABSP_XSG1
IAG_XV3

6 Mechanical Information

The TSB15LV01 is packaged in a high-performance 80-pin PFC package. The following shows the mechanical dimensions of the PFC package.

PFC (S-PQFP-G80)
PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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