ERRATA TO THE DVLynx (TSB12LV42) DATA MANUAL

(TEXAS INSTRUMENTS LITERATURE NO. SLLS293, November 1998)

This document contains corrections and additions to information in the TSB12LV42 data manual (TI Literature Number SLLS293)

1. On asynchronous transmit automatic retries from the Bulky Asynchronous FIFO, the retry code is not incremented correctly. All retries should have a retry code (rt code) of 01 which indicates retry_X. However, retries on DVLynx all have a retry code of 00 which indicates retry_1.

SOLUTION: None

2. When transmitting asynchronous data from the BATX FIFO, the AsyncTXFIFO-Struck interrupt (bit 14 at register 10h) is falsely generated.

SOLUTION: The ATSTK interrupt (bit 14 at register 10h) should be disabled if supporting asynchronous transmit.

 If the ARHS bit (register ECh, bit 27) is set to 1, during a bus reset, then part of the Self-IDs collected into the BARX FIFO will be lost. This is because DVLynx assumes part of the Self-IDs being written into the FIFO are asynchronous headers and strips them.

SOLUTION: Clear ARHS prior to bus reset.

4. Extended Interrupt Register (address 18h) bit 20 is set when a Cycle Start packet is flushed from the Broadcast Write Receive FIFO. Since cycle start packets are continuously being sent if there is a Cycle Master present on the 1394 network, this interrupt can unnecessarily bog down the host processor. Similarly, the Extended Interrupt Register bit 12 is set whenever a Cycle Start packet is flushed from the Bulky Asynchronous FIFO.

SOLUTION: This interrupt should be disabled if the DVLynx must support Isochronous capability in the desired application.

- 5. If a node transmitting DV data is turned OFF and back ON again, the receiving DVLynx may only receive part of the first frame. This is because the last frame of some DV transmitters are truncated when the transmitting source is turned off. When turned back on (transmit), the DVLynx internal DV counter is out of synch and will truncate the first packet. The DVLynx is able to recover on the second and all subsequent DV packets.
 - SOLUTION: The receiving node CODEC should be able to discard the first partial frame received by the DVLynx. It should resume receiving for the second and all subsequent frames. If this is not possible, then a software reset will reset the DVLynx DV counter. The receiving node would have to detect when the other node had turned OFF, and then perform the software reset. We suggest Busying Off all asynchronous packets until the software reset and reprogramming is complete. This can be selected by programming register Ch bit 02 immediately after the software reset.
- 6. The DVLynx receive state machine will get stuck in DV receive mode it is receiving DV packets addressed to the node. The result is that the DVLynx may miss self-ids or ack_busy asynchronous packets if they occur while the DVLynx is receiving DV packets (or has data in the FIFO.) One symptom of this problem is never receiving the Self-Id ready interrupt after a bus reset. The DVLynx receive state machine will get back into idle (able to receive self-ids, asynchronous, or DV FIFO) whenever an empty packet is received, or the DV FIFO is emptied.



- SOLUTION: This should not present a problem with asynchronous data. Transmitting nodes should retry asynchronous packets if it receives an ack_busy. For self-ids, the receiving node should turn off the *receive self id* bit in register Ch after the bus reset interrupt. Then the node should wait for the sub-action gap interrupt. This will tell them when the self-id period is over. The node will not capture the self-ids, but the bus info register (register 44h) will contain the correct information about the node.
- 7. When using DVLynx in 68000 or 8051 mode with a 1394.a PHY (for example TSB41LV03), the LPS pin can not be used to indicate link power status to the PHY. As documented by the 1394.a standard, a 1394.a compliant PHY will not generate SCLK to the link layer until it receives the link power status (LPS) status from the link. However, the DVLynx uses SCLK from the PHY to generate the LPS signals in 68000 and 8051 modes. The result is a standoff between the PHY needing LPS and the link layer needing SCLK. In the TMSAV7100 ARM mode, the DVLynx has no problem since it uses an external BCLK to generate LPS.

To work around this problem, the LPS pin on the PHY should be tied high to PHY power.



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated