ERRATA TO THE TSB21LV03 DATA SHEETS

(TEXAS INSTRUMENTS LITERATURE NO. SLLS230, ALL RevisionS)

This document contains corrections and additions to information in the TSB21LV03 data sheets (TI Literature Numbers SLLS230, SLLS230A, and SLLS230B), also included in *IEEE 1394 Circuits Data Book*, 1997 (TI Literature Number SLLD004), including circuit changes required when changing from the TSB21LV03 device to the production release Revision A device (TSB21LV03A) in applications.

TSB21LV03

The following items apply only to the initial production Revision of the TSB21LV03 device.

a. There has been a problem with corrupted packets when the phy supply voltage is at the high end of the specification range and the temperature is also at the high end of the specification range. It is recommended that the supply voltage be maintained at the low end of the range, approximately 2.9 volts ±5% to avoid this problem. This will be corrected in production release Revision A — TSB21LV03A.

b. The arbitration comparators have a wide threshold switching range. Although there have been no reported problems in applications, it is possible that problems could be caused in a noisy environment. If the problem were to appear, the symptom would most likely be corrupted packets. This will be corrected in production release Revision A — TSB21LV03A.

c. The speed comparators have a wide threshold range near the threshold region and delays through the speed comparators are approximately 50 ns. Although there have been no reported problems in applications, it is possible that problems could be caused in a noisy environment. If the problem were to appear, the symptom would most likely be corrupted packets. This will be corrected in production release Revision A — TSB21LV03A.

d. The twisted pair drivers have headroom problems under low V_{DD} and high common mode conditions. Although there have been no reported problems in applications, if the problem were to occur, it would typically appear in situations where the node was a power provider and maximum voltage drops occurred in the cable power leads. This will be corrected in production release Revision A — TSB21LV03A.

e. TPBias is not well regulated. Although there have been no reported problems in applications, if the problem were to occur, it would typically appear in situations where the node was a power provider and maximum voltage drops occurred in the cable power leads. This will be corrected in production release Revision A — TSB21LV03A.

f. A pull-down transistor on the $\overline{\text{RESET}}$ terminal activated by PWRDWN was not implemented on the initial production design. This will be corrected in production release Revision A — TSB21LV03A.

g. The D2 and D3 lines do not comply with informative Annex J of the 1394 specification, which specifies that unused data terminals shall be driven to a logic 0 during packet reception. Currently, these terminals are placed in a high-impedance state. This will be corrected in production release Revision A — TSB21LV03A.

h. The TPBias output voltage limits have been relaxed to 1.165 volts minimum and 2.065 volts maximum. These limits should not be a problem in actual systems implementations. The limits are generally only exceeded at the minimum or maximum supply voltage levels and there is enough guardband in the standard that it should not be a problem. This will be corrected in production release Revision A — TSB21LV03A.

i. If transmitting data at 200 Mbps between nodes 5 or more hops apart, the TSB21LV03 may cause occasional spurious bus resets. As the number of hops increases, the frequency of spurious bus resets will also increase. Simulations predict that 4 hops may cause the problem but lab testing could only produce the problem with 5 or more hops with several minutes (5 to 20 minutes) between spurious resets. Having 5 hops in the network does not cause the problem, having 5 or more hops in the transmit path between the transmitting node and the furthest end of bus may cause the problem. The most critical path is the asynchronous acknowledge transmit path. This will be corrected in production release Revision A — TSB21LV03A.

j. When connected to a network with 3 or more hops between the root node and the furthest node on the network, upon bus reset the TSB21LV03 network may not initially issue the correct number of self–ID packets. If this occurs, the TSB21LV03s that did not issue a self–ID packet will cause another bus reset. This bus reset process will continue until the correct number of self–ID packets are issued unless the process is interrupted by receipt of a non–self–ID packet. The frequency of occurrence (number of resets before multiple self–ID packages occur) averages:

   3 hops ≅ 1018 resets

   4 hops ≅ 133 resets

   5 hops ≅ 23 resets

   6 hops ≅ 14 resets

   7+ hops ≅ 7 resets

Workaround:

Optimize the bus topology to place the root close to the center of the network. To allow the bus reset sequence described above to complete, it must not be interrupted by cycle start packets or asynchronous packets. It is recommended that upon bus reset, the isochronous resource manager node should wait for 450 μs after the start of the initial bus reset then check to see if another bus reset indication has been sent to the link.

If another bus reset has been indicated, repeat the wait. If another bus reset has ***not*** been indicated, then resume cycle start packets and asynchronous packets. The bus manager should use the final package of self–IDs received.

k. Lab tests have shown that there is a possibility of a glitch at the end of data transmission (transition from *data-strobe encoded data* to *data end arbitration line state* at the end of a packet). This glitch may cause an extra data bit to be “received” by the phy, which is then transmitted to the link. This can cause data CRC error acknowledges when asynchronous data is transmitted. It can also cause parity errors on the received acknowledge.

   This glitch will not necessarily cause a problem. It is very narrow, so it is very sensitive and dependent on the application. The problem is sensitive to supply voltage, cable, layout, and ports. It may be seen on the phy–link interface as an extra 4 bits (at S200 speed) being sent to the link by the phy, which causes the CRC and parity errors. This will be corrected in production release Revision A — TSB21LV03A.

TSB21LV03 data sheet changes (TI Literature Number SLLS230)

l. In the original and Revision A versions of the data sheet (SLLS230 and SLLS230A) on page 3 (page 9–5 in the *IEEE 1394 Circuits Data Book*, 1997), paragraph 3 states that when the power supply is removed, the twisted-pair drivers will go into a high impedance state.

This is incorrect. When power is removed, the twisted-pair ports could load down the TPBias of the ports connected to it. If connected to another TSB21LV03, this will only disable the port connected to the unpowered TSB21LV03. If connected to a TSB11C01, this could incapacitate all three ports on the TSB11C01 because the TSB11C01 has only a single TPBias shared between the 3 ports.

This problem will **NOT** occur if the TSB21LV03 is ***powered down*** using the PD terminal because power is still being supplied to the device.

If a multi-port system is designed in accordance with the 1394 standard, this problem will not occur because when a node is unpowered, its phy is still powered using the 1394 cable power.

Revision B of the data sheet, SLLS230B, is correct.

m. In the original and Revision A versions of the data sheet (SLLS230 and SLLS230A), there is an error in the PACKAGE OUTLINE drawing on page 5 (page 9–7 in the *IEEE 1394 Circuits Data Book*, 1997) and in the APPLICATION INFORMATION drawing, Figure 4 on page 15 (page 9–17 in the *IEEE 1394 Circuits Data Book*, 1997). Pins 28, 29, and 30 should be corrected as shown below:

– pin 28 is PC2

– pin 29 is PC1

– pin 30 is PC0

The PACKAGE OUTLINE drawing and APPLICATION INFORMATION drawing in data sheet Revision B (SLLS230B) are correct.

n. In the Terminal Functions table of all Revisions of the data sheet on page 7 (page 9–9 in the *IEEE 1394 Circuits Data Book*, 1997), the tolerance specified for the resistor in the R0 and R1 row (terminals 59 and 60) is incorrect.

– The correct tolerance is 0.5%.

This will be corrected in the data sheet released for the production Revision A (TSB21LV03A).

Application notes for both the original device and device production Revision A (TSB21LV03A):

aa. The line A/B status (returned by a read of register 3) will be given as *b0000* if the read is performed immediately following a packet transfer between the phy and link (either transmitted or received). This is because the line A/B status is set to b0000 during packet transmission/reception, including during the DATA_END time following the actual data transfer of the packet.

The link interface will enter the idle state after the data is transferred, but the phy will still be transmitting/receiving the DATA_END for the packet (for approximately another 240 ns). If a read–register–3 request is performed at this time, the phy will return b0000 as the line A/B status. This is likely to occur if there is a lot of traffic on the line, since the link will queue up the read–register request until any packet data transfers have completed (as indicated by the phy–link interface going idle), then immediately perform the read–register request. The line A/B status returned by a read of register 3 is invalid if there is any packet traffic on the line. Because of this, the line A/B status is not very useful for real-time monitoring of the line. Generally, the status will be either b0000 (packet traffic is on the line), or b1111 (the line is IDLE), though other line states are possible if the read is performed at just the right time (for example, during ARBITRATION, tree–ID, or self–ID).

bb. On hardware reset only, during the bus reset process, the TSB21LV03 will send two status transfers. The first is *invalid* and reports that the local node is root, with a node number of *0*, and no other phys are connected. Later during the same bus reset, the correct root, node number and connection status are reported. This double status transfer only occurs during hardware reset, not during initiated software bus reset or from bus reset received over the bus. For the hardware reset condition only, the micro must make sure that it does not read the *new* node number, root, and connection information too soon before the second, correct status transfer has taken place.

cc. To avoid potential bus hanging problems, it is very important that the TSB21LV03's gap count setting should never be done directly from the link by writing to the phy register directly. The gap count should only be set with phy config packets. This is a standards issue. TI devices meet the IEEE 1394–1995 standard.

Application changes for device production Revision A (TSB21LV03*A*):

When replacing TSB21LV03 devices with production Revision A devices (TSB21LV03A) in applications, the following items are applicable:

a1. Bus holder functionality was added to:

- phy/link interface data terminals D0 – D3 (pins 13, 14, 15, and 16)
- phy/link interface control terminals CTL0 and CTL1 (pins 11 and 12)
- phy/link interface link power status terminal LPS (pin 2)
- phy/link interface link request terminal LREQ (pin 3)
- phy/link interface power down terminal PD (pin 7)

Consequently:

- If any of these pins are to be tied to a fixed state through a resistor, the resistor must be sized to provide enough current to overcome the bus hold function. The recommended value is 1 kΩ.
- If pulldown resistors are used on the control 0 and control 1 pins (CTL0 and CTL1), these resistors should also be 1 kΩ.
- The LPS pin (pin 2) is a special case. If the LPS pin is tied to the link power plane directly, it must be connected through a 1-kΩ resistor to avoid problems in the case of the phy being powered down and the link being powered up. The 1-kΩ resistor prevents the link power plane from supplying power via the LPS connection to the phy when the phy is powered down.

b1. The TSB21LV03**A** SYSCLK output is active when chip reset is active (low).

The TSB21LV03 SYSCLK output was *NOT* active when chip reset was low.

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